



**Submission to JTRS JPO from SDR Forum
regarding DSP and FPGA portability
standardization effort**

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The SDR Forum submits the following points for consideration by the JTRS JPO.

1. The SDRF regards standardization of the software environment for high speed signal processing (including DSP and FPGA) to improve software portability as critical to the growth and long-term success of the SDR industry. Development of separate military and commercial standards would be detrimental to both JPO program goals and to the non-military industry and users.
2. Commercial requirements and best practices should be considered in the JPO standardization process. In its role as the consensus organization for the SDR industry, the SDRF would like to peer-review the developing standard and provide comments to the writing teams.
3. The Hardware Abstraction Layer Working Group (HALWG) of the SDRF Technical Committee has carried out an RFI process to study industry best-practices, available technologies, and architectures for portability of high speed signal processing software. The RFI received 14 responses. This indicates the high level of industry interest in this area of standardization. Also, the HALWG recommendations developed from the RFI responses should be considered by the JPO writing teams when developing standards.
4. The SDR market is international. For example, the European Union has funded a significant program called E2R, for end to end reconfigurability, which includes as one of its work areas reconfiguration of radio functions in a portable fashion. Many of the 14 HALWG RFI responses came from European organizations.
5. To avoid a detrimental split between military and commercial standards, any extension of the SCA should preserve the current non-ITAR unlimited-download status of the SCA.
6. The JPO sponsored military standard should be an open standard.
7. The SDRF submitted a document to the JPO dated June, 2003 titled "API Position Paper SDRF-03-I-0030" which made general recommendations for waveform portability. The recommendations made in that submission also apply to DSP and FPGA software environments. The points stated here are consistent with the general principles articulated earlier.

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