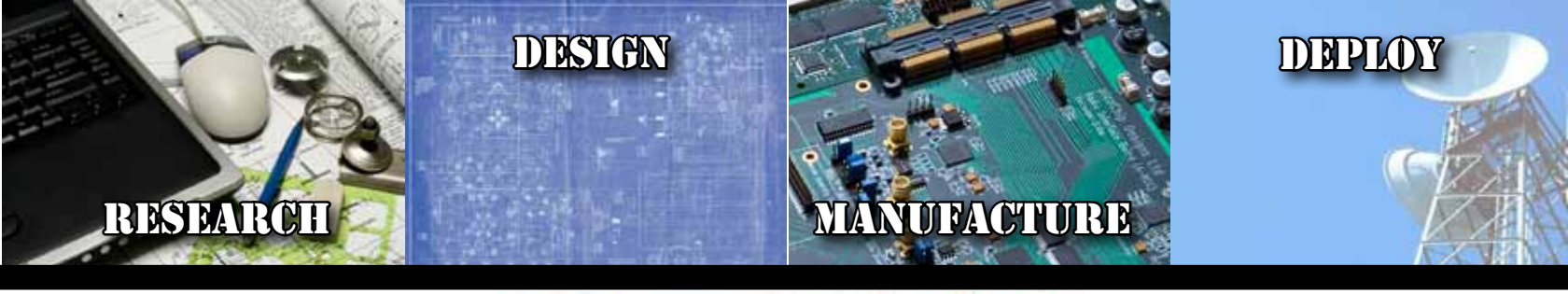

SDR'10

Technical Conference and Product Exposition

30 November - 3 December 2010 • Washington, DC

The premier event for bringing next generation radio technologies to life.

Attracting attendees from all aspects of the reconfigurable radio value chain, SDR'10 is the ideal place to network and make an impact on the reconfigurable radio community. This is the only event devoted to the advancement of reconfigurable radio technologies from research through deployment. This year's event features technical presentations, demonstrations, tutorials, and workshops from some of the leading experts from all positions in the reconfigurable radio value chain.

Featuring Keynotes from Recognized Industry Leaders:

Dr. Masayuki Ariyoshi
Principal Researcher and Cognitive Radio Research Project Leader, System Platforms Research Laboratories, Central Research Laboratories,
NEC Corporation

Vern Fotheringham
Chairman, *CBT Group*

Madan Jagernauth
Vice President, Wireless Marketing and Product Management, *Huawei Technologies*

Jörgen Lantto
Executive Vice President, Chief Technology Officer and Strategy
ST Ericsson

Richard J. Lynch
Executive Vice President and Chief Technology Officer,
Verizon Communications

Dr. Richard North
Technical Director,
Joint Program Executive Office Joint Tactical Radio System (JPEO JTRS)

Thomas Stroup
CEO, *Shared Spectrum Company*

Presented by:

Established in 1996, The Wireless Innovation Forum (SDR Forum Version 2.0) is a non-profit mutual benefit corporation dedicated to driving technology innovation in commercial, civil, and defense communications worldwide. Members bring a broad base of experience in Software Defined Radio (SDR), Cognitive Radio(CR) and Dynamic Spectrum Access (DSA) technologies in diverse markets and at all levels of the wireless value chain to address emerging wireless communications requirements. To learn more about The Wireless Innovation Forum, its meetings and membership benefits, visit www.WirelessInnovation.org.

WIRELESS INNOVATION FORUM

#SDR10

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Program at a Glance

General Program Chair, Dr. John Glossner

CTO, *Sandbridge Technologies*

Technical Program Committee

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Cosimo Berlingeri, *Selex Communications*
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Benjamin Egg, *fred harris & associates* **(Tutorial Track Chair)**
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Kees Goosens , *TU Eindhoven*
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Friedrich Jondral, *Karlsruhe Institute of Technology (KIT)*
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Vince Kovarik, *Harris Corporation* **(Workshops Chair)**
Fahdi Kurdahi, *UC Irvine*
Sébastien Le Nours, *University of Nantes*
Dake Liu, *Institute of Tech Linkoping Univ*
Joe Mitola, *Stevens Institute of Technology*
Fanny Mlinarsky, *OctoScope* **(Demonstrations Track Co-chair)**
Klaus Moessner, *Univ of Surrey*
Jakub Moskal, *Northeastern University*
Mayan Moudgill, *Sandbridge Technologies*
Christophe Moy, *SUPELEC*
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Najam ul Islam Muhammad, *Eurecom*
R Muralidharan, *Tata Power SED*
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Robert Normoyle, *DRS*
Dale Parson, *Kutztown University*
Antti Piipponen, *Nokia*
Nikos Pitsianis, *Aristotle University and Duke*
Kim Rounioja, *Nokia*
Magdalena Sanchez, *Univ Ireland, Maynooth*
Mike Schulte, *UW Madison*
Bob Schutz, *ViaSAT*
William Scott, *GDC4S*
Murugappan Senthilvelan, *Optimum Semiconductor Technologies* **(Demonstrations Track Co-chair)**
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Mihai Sima, *University of Victoria, Canada*
Sarvpreet Singh, *Fraunhofer FKIE*
Dean Skuldt, *Motorola*
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Mark Turner, *Harris Corporation*
Manuel Uhm, *Xilinx*
Ben Vigoda, *Lyric Semiconductor*
Kees Vissers, *Xilinx*
Marilyn Wolf, *Georgia Tech*
Stephan Wong, *TU Delft*

Program at a Glance

Monday, 29 November

18:00-20:00 **Early Registration, sponsored by Green Hills Software, Inc.** (*Regency Foyer*)

19:00-21:00 **Technical Program Committee Appreciation Dinner** *(Arlington Room)*

Tuesday, 30 November

08:00 **Breakfast** (*Regency Foyer*), **Speakers' Breakfast** *(Potomac II)*

	Regency C	*Regency D*	*Regency E*	*Regency F*	*Potomac III & IV*	*Potomac V & VI*
	Workshop 1A	**Tutorial 1B**	**Tutorial 1C**	**Tutorial 1D**	**Tutorial 1E**	**Workshop 1F**
10:00 (p. 9)	Understanding the Rules for TV Band Devices **BEGINS at 09:00** ***(Overview on page 9)***	Radio-In-The-Loop: Design Tools for Software Radios ***John Irza***	ETSI Reconfigurable Radio Systems (RRS) ***Markus Mueck***	Migrating Legacy Radios to the SCA ***Toby McClean, Mike Williams***	Open Component Portability Infrastructure (Open CPI) ***Michael Pepe***	Public Safety Communications ***(Overview on page 10)***

12:00 **Lunch**

13:30 **Conference Welcome: John Glossner**, *Sandbridge Technologies* and Conference Chair

13:40 **Keynote: Masiyuki Ariyoshi**, Principal Researcher and Cognitive Radio Research Project Leader, System Platforms Research Laboratories, Central Research Laboratories, *NEC Corporation*

14:20 **Keynote: Tom Stroup**, CEO, *Shared Spectrum Company*, with **Vern Farthingham**, Chairman, *CTB Group*

15:00 **Coffee Break**

	Regency C	*Regency D*	*Regency E*	*Regency F*	*Potomac III & IV*	*Potomac V & VI*
	Session 2A	**Session 2B**	**Session 2C**	**Expert Lecture 2D**	**Workshop 2E**	**Workshop 2F**
15:15 (p. 10)	SCA ***Chair: Eric Christensen***	Cognitive Radio I ***Chair: James Neel***	Education & Radio Challenge ***Chair: Peter Farkas***	Air Interface Innovations Applicable to Cognitive Radio Systems ***Donald Steinbrecher***	Open Source in Military and Commercial Wireless Applications ***(Overview on page 11)***	Public Safety Communications ***(Overview on page 11)***

18:00 - 21:00 **Welcome Reception and Forum Awards**, Sponsored by General Dynamics, held at the **International Spy Museum**

GENERAL DYNAMICS
C4 Systems

Want the complete story behind some of the most intriguing espionage cases in history? What about spies and spying in the world right now? Join us for tapas and drinks at the Spy Museum and get the latest intel on all things spy. The International Spy Museum opened in Washington, DC on July 19, 2002. It is the only public museum in the United States solely dedicated to espionage and the only one in the world to provide a global perspective on an all-but-invisible profession that has shaped history and continues to have a significant impact on world events. The Museum features the largest collection of international espionage artifacts ever placed on public display. Many of these objects are being seen by the public for the first time. These artifacts illuminate the work of famous spies and pivotal espionage actions as well as help bring to life the strategies and techniques of the men and women behind some of the most secretive espionage missions in world history. **Directions available at the registration desk.**

Proceedings and Presentations submitted by 15 Oct 2010 can be found on your complimentary USB drive.
Updates are available at http://Conference.WirelessInnovation.org/page/2010Proceedings

Program at a Glance

Wednesday, 1 December

08:00 **Breakfast** (*Regency Foyer*), **Speakers' Breakfast** *(Potomac II)*

08:30 **Introduction to Day 2 and Announcements: John Glossner**, *Sandbridge Technologies* and Conference Chair

08:40 **Regulatory Keynote: Peter Tenhula**, *Shared Spectrum Company* and Chair, *Wireless Innovation Forum Regulatory Committee*

09:20 Break

	Regency C	*Regency D*	*Regency E*	*Regency F*	*Potomac III & IV*	*Potomac V*	*Potomac VI*
09:50 (p. 12)	**Session 3A**	**Session 3B**	**Session 3C**	**Workshop 3D**	**Tutorial 3E**	**Tutorial 3F**	**Tutorial 3G**
	Security ***Chair: Mark Turner***	Cognitive Radio II ***Chair: Sherin Kamal***	Communica-tions Signal Processing I ***Chair: Kamran Arshad***	Regulatory I *(Overview on page 13)*	IPA ***Peter G. Cook, James Neel***	Two-Thirds of SDR is SD ***Bruce Trask***	A Graphical Approach to FPGA Programming ***Christian Amadasun***

11:50 Lunch and Exhibits (*Independence A&B*, please see pages 27-28 for a list of Exhibitors)

	Regency C	*Regency D*	*Regency E*	*Regency F*	*Potomac III & IV*	*Potomac V*	*Potomac VI*
13:45 (p.14)	**Session 4A**	**Session 4B**	**Session 4C**	**Workshop 4D**	Expert Lecture 4E	**Tutorial 4F**	**Tutorial 4G**
	System Implementation and Test I ***Chair: Fanny Mlinarsky***	Cognitive Radio III ***Chair: S.M. Hasan***	Communica-tions Signal Processing II ***Chair: fred harris***	Regulatory II *(Overview on page 14)*	Multipath Interference Characterization in Wireless Communication Systems ***Michael Rice***	Rapid Prototyping Digital SCA-Based SDR Waveforms with OSSIE: Hands-On ***Carl B. Dietrich, Frank Kragh, Donna Miller***	Extending the SCA to Meet Interna-tional Security Needs ***Scott Leubner and Chuck Linn,*** Harris Corp.

15:45 **Coffee Break**

16:00 **Panel - The Future of Radio Technologies**

Cognitive radio technologies are enabling dynamic spectrum access and interference suppression, and they will soon be transitioning into a wide range of commercial and defense wireless products and services. The FCC's TV "white spaces" decision and the DARPA WNaN and EPLRS-XF efforts are just a few examples. Standards are beginning to emerge in 3GPP and IEEE that are integrating these technologies into "4G" and beyond. Although these near-term prospects are very promising, there remain many more exciting areas in which advanced radio and networking technology will have a profound impact. The impact will be felt in areas such as radio network robustness, spectrum efficiency, regulations and enforcement, dynamic spectrum access to additional "white spaces", device and network performance, improved broadband user experiences and applications, etc. This panel of expert "radio futurists" will discuss the new vistas for smarter and smarter radio technologies, the impact of these technologies on regulatory frameworks and business models, and the challenges that remain in moving forward at Internet speed.

MODERATOR: Dr. Douglas Sicker, Chief Technologist, *Federal Communications Commission*
PARTICIPANTS:

- The Honorable Meredith Atwell Baker, Commissioner, *Federal Communications Commission*
- Dr. Bruce Fette, Program Manager, *Defense Advanced Research Projects Agency (DARPA)*
- Dr. Paul Kolodzy, *Kolodzy Consulting* (former Chair, *FCC Spectrum Policy Task Force*)
- Dr. Preston Marshall, Director, *Univ. of Southern California, Information Sciences Institute*
- Dr. Joe Mitola, VP for the Research Enterprise, *Stevens Institute of Technology*

17:30 **Exhibits and Technology Showcase** (*Independence A&B*, please see page 22-28 for more information)

19:30 **GNU Radio Users Group**, Sponsored by Ettus Research (*Potomac V & VI)*

Program at a Glance

Thursday, 2 December

08:00 **Breakfast** (*Regency Foyer*), **Speakers' Breakfast** *(Potomac II)*

08:30 **Introduction to Day 3 and Announcements: John Glossner**, *Sandbridge Technologies* and Conference Chair

08:40 **Keynote: Dick Lynch**, Executive Vice President and Chief Technology Officer, *Verizon Communications*

09:20 Break

	Regency C	*Regency D*	*Regency E*	*Regency F*	*Potomac III & IV*	*Potomac V*	*Potomac VI*
	Session 5A	**Tutorial 5B**	**Session 5C**	**Workshop 5D**	**Workshop 5E**	**Expert Lecture 5F**	**Session 5G**
09:50 (p. 16)	System Implementation and Test II ***Chair: Fanny Mlinarsky***	Emerging Commercial Wireless and Cognitive Radio Standards ***Chair: James Neel***	Waveform and Software Design I ***Chair: Daniel S. Iancu***	Analysts I *(Overview on page 17)*	SDR in Space I *(Overview on page 17)*	GNU Radio: Introduction and Computational Capabilities ***Tom Rondeau***	Processors ***Chair: Raghavan Muralidharan***

11:50 Lunch, Exhibits, and Technology Showcase (*Independence A&B,* please see pages 22-27 for more information)

	Regency C	*Regency D*	*Regency E*	*Regency F*	*Potomac III & IV*	*Potomac V & VI*
	Session 6A	**Session 6B**	**Session 6C**	**Workshop 6D**	**Workshop 6E**	**6F**
13:45 (p. 18)	Applications ***Chair: Sanjay Jinturkar***	System Implementation and Test III ***Chair: Fanny Mlinarsky***	Networks ***Chair: Sanyogita Shamsunder***	Analysts II *(Overview on page 19)*	SDR in Space II *(Overview on page 19)*	SCA Next Roll Out *(Overview on page 19)*

(Continues on next page ...)

Call for Presentations

2011 Wireless Innovation Forum European Conference on Communications Technologies and Software Defined Radio

22-24 June 2010 • Brussels, Belgium

In June 2011, leaders in the advanced wireless community will come together to explore the evolution of reconfigurable radio over the next several years.Reconfigurable radio technologies are becoming essential to support the requirements of the wireless market: network operators and wireless service providers in all market domains need to contain their capital and operational expenditures while supporting a proliferation of wireless standards and wireless end users, be they business travelers or first responders in a national emergency, are demanding radio technologies that allow them to communicate with whoever they need to, whenever they need to and wherever they are. This conference will explore these requirements across domains and present innovative solutions in development to address them. **Abstracts due 7 January 2011.**

http://Europe.WirelessInnovation.org

Thursday, 2 December (continued)

15:45 **Break**

16:00 **Keynote: Madan Jagernauth**, Vice President, Wireless Marketing and Product Management, *Huawei Technologies*

16:30 **Keynote: Jörgen Lantto**, Executive Vice President, Chief Technology Officer and Strategy, *ST Ericsson*

17:10 **Panel Session - Comparing FPGA + C compilers with multi-core technology**

Field Programmable Gate Arrays (FPGAs) traditionally have been a replacement for low volume Application Specific Integrated Circuits (ASICs). Recently FPGAs have emerged with large amounts of logic, memory, DSP, CPU, and connectivity components making them a full Multi Processor System On a Chip (MPSoC) system. Historically these devices have been difficult to program following a hardware (HDL) design methodology with difficult placement, wiring, and timing closure constraints. Thus programming FPGAs has historically been difficult.

Processors, in contrast, have historically been programmed in high level languages such as C. Compilers have been developed that efficiently map the high level language to optimized assembly code. Even special purpose DSP types such as fixed point arithmetic have recently been efficiently dealt with in C languages. Parallel compilation has even been effective for modern Vector/SIMD loop nests. However, except for certain special cases of multithreading loop nests, parallelization of arbitrary codes distributed across multiple processors remains difficult.

Historically, the time to develop applications in a Processor has generally been faster because the long iterative cycles of place/route/timing in an FPGA. Recently FPGA vendors have tried to reduce this gap with innovative programming environments, the use of libraries, and the incorporation of processors on the same FPGA fabric.

This panel will look at the costs, programmability, performance, power, and time-to-market of multiprocessor designs versus FPGAs in a shoot-out to see who will ultimately dominate future SDR platforms.

ORGANIZER: Kees Vissers, *Xilinx*
MODERATOR: John Glossner, *Sandbridge Technologies*
PARTICIPANTS:

- Jeff Bier, *BDTI* (balance)
- Seungwon Choi, *Hanyang Univ* (GPUs)
- Dave Kelf, *Signmatix* (programming)Fanny Mlinarsky, *octoScope* (test and verification)
- Chris Rowen, *Tensilica* (Multi core)
- Kees Vissers, *Xilinx* (C tools + FPGA + small cores)
- Sanjay Jinturkar, *Ikanos Communications, Inc.* (Compilers)

18:00-20:00 **Wireless Innovation Forum Members Reception** *(Regency A)* and **Annual Meeting** *(Regency EF)*

Friday, 3 December

08:00 **Breakfast** (*Regency Foyer*), **Speakers' Breakfast** *(Potomac II)*

	Regency C	*Regency D*	*Regency E*	*Regency F*	*Potomac III & IV*	*Potomac VI & VI*
	Session 7A	**Session 7B**	**Session 7C**	**Session 7D**	**Expert Lecture 7E**	**Tutorial 7F**
08:30 (p. 20)	Waveform and Software Design II ***Chair: Richard Taylor***	RF, IF, ADC ***Chair: Mohammed Ismail***	Spectrum, Regulatory, and Standards ***Chair: Zhongren Cao***	Communications Signal Processing III **Chair: Joseph Gaeddert**	Modem Tutorial **fred harris**	ESSOR SDR Architecture – Motivation and Overview *(Overview on page 21)*

10:30 **Coffee Break**

10:45 **Keynote**: **Rich North**, Technical Director, *Joint Program Executive Office Joint Tactical Radio System (JPEO JTRS)*

11:30 **End Note, Conference Close and Satisfaction Survey Prize Drawing**

Complete our survey and be registered to win!
www.WirelessInnovation.org/page/SDR10survey

Workshops, Tutorials and Expert Lectures at a Glance

SDR '10 Workshops

Workshops strive to achieve a topic specific objective through multiple interactive sessions exploring an area relevant to research, design, manufacture or deployment of reconfigurable radio technologies. Workshops are provided in one or two 2 hour sessions which may be extended through a conference keynote or plenary panel session.

During SDR'10, the Wireless Innovation Forum will host 6 Expert Workshops exploring specific topic areas:

Tuesday, November 30

- **Understanding the Rules for TV Band Devices**, Sponsored by the Wireless Innovation Forum Cognitive Radio Work Group, information on page 9.
- **Open Source in Military and Commercial Wireless**, Sponsored by the Military Open Source Software Association (http://www.mil-oss.org), information on page 11.
- **Public Safety Workshop**, Sponsored by the Wireless Innovation Forum Public Safety Special Interest Group, information on pages 10 (a.m. session), and 11 (p.m. session).

Wednesday, December 1

- **Regulatory**, Sponsored by the Wireless Innovation Forum Regulatory Committee, information on pages 13 (a.m. session) and 14-15 (p.m. session).

Thursday, December 2

- **Analysts**, Sponsored by the Wireless Innovation Forum User Requirements Committee, information on pages 17 (a.m. session) and 19 (p.m. session).
- **SDR in Space**, Organized by Dr. R. Scott Erwin & Dr. Jim Lyke, Space Vehicles Directorate, *Air Force Research Laboratory*, information on pages 17 (a.m. session) and 19 (p.m. session).

SDR '10 Tutorials

Tuesday, Nov. 3, 10:00 (information on pages 9-10)

- 1B: Radio-In-The-Loop: Design Tools for Software Radios
- 1C: ETSI Reconfigurable Radio Systems (RRS)
- 1D: Migrating Legacy Radios to the SCA
- 1E: Open Component Portability Infrastructure (Open CPI)

Wednesday, Dec. 1, 09:50 (information on page 13)

- 3E: IPA
- 3F: Two Thirds of SDR is SD
- 3G: A graphical approach to FPGA programming

Wednesday, Dec. 1, 13:45 (information on page 15)

- 4F: Rapid Prototyping Digital SCA-Based SDR Waveforms with OSSIE: A Hands-On Tutorial
- 4G: Extending the SCA to meet international security needs

Thursday, Dec. 2, 09:50 (information on page 16)

- 5B: Emerging Commercial Wireless and Cognitive Radio Standards

Friday, Dec. 3, 08:30 (information on page 21)

- 7F: ESSOR SDR Architecture – Motivation and Overview

SDR '10 Expert Lectures

Tuesday, Nov. 30, 15:15 (information on page 11)

- 2D: Air Interface Innovations Applicable to Cognitive Radio Systems, Donald Steinbrecher, *Naval Undersea Warfare Center, USA*

Wednesday, Dec. 1, 13:45 (information on page 15)

- 4E: Multipath Interference Characterization in Wireless Communication Systems, by Michael Rice, *Brigham Young University, USA*

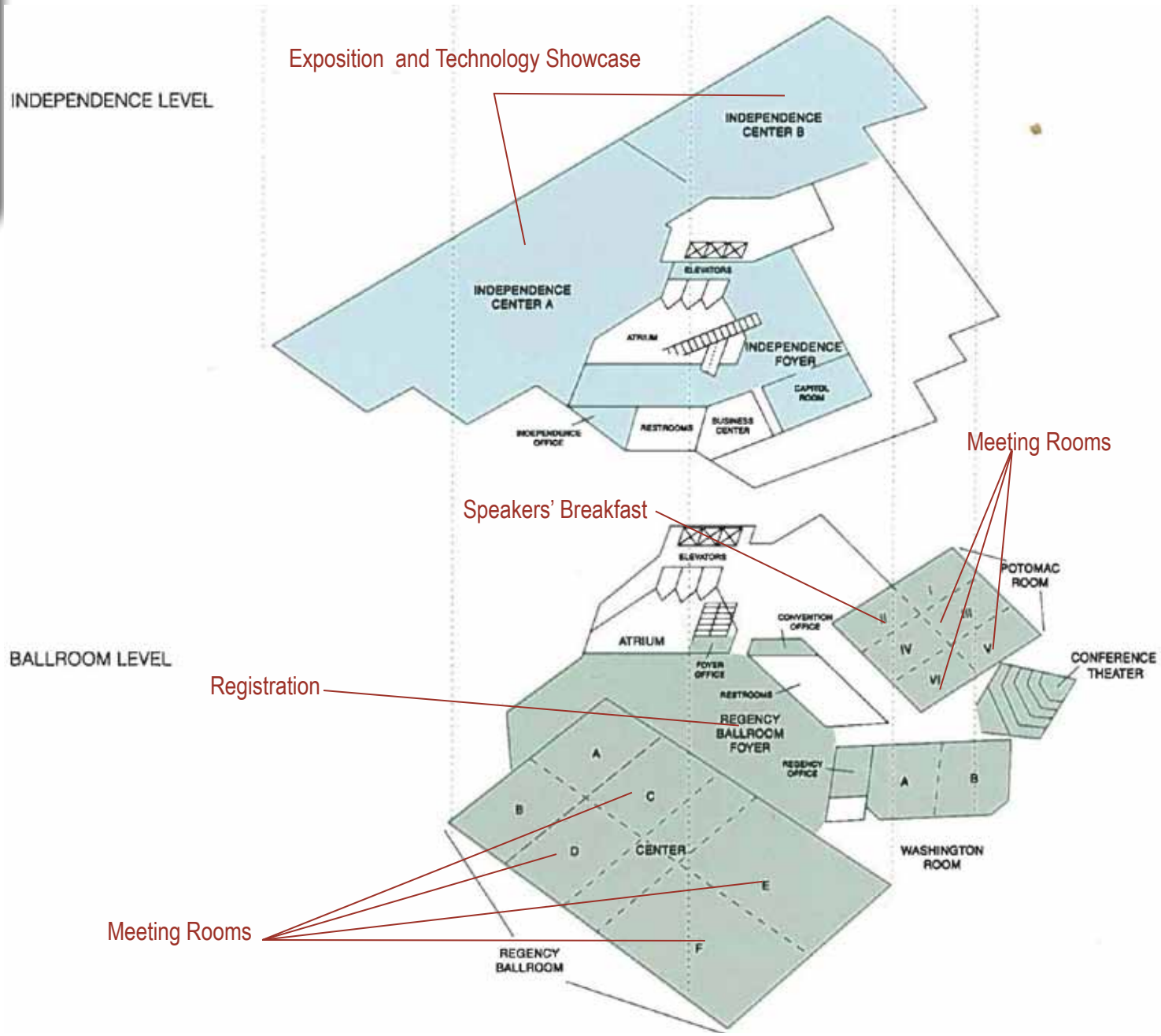
Thursday, Dec. 2, 09:50 (information on page 17)

- 5F: GNU Radio: Introduction and Computational Capabilities, by Tom Rondeau, *Center for Communications Research, USA*

Friday, Dec. 3, 08:30 (information on page 21)

- 7E: Modem Tutorial, by fred harris, *San Diego State University, USA*

Conference Site Map



10:00

Workshop 1A: Understanding the Rules for TV Band Devices

Regency C, ***Note: This workshop begins at 09:00***

Sponsored by the Wireless Innovation Forum Cognitive Radio Work Group

In November, 2008 the U.S. Federal Communications Commission (FCC) announced a landmark decision allowing the use of fixed and personal/portable devices in "unused" TV Band spectrum, referred to as "white space." Numerous petitions for reconsideration were filed along with several database manager proposals and in September of 2010, the FCC published a Second Memorandum Opinion and Order on Unlicensed Operation in the TV Broadcast Bands. In a related action, in November 2010, OFCOM launched a consultation on the implementation of Geolocation Databases in the UK.

The purpose of this workshop is to explore the critical technical, business and regulatory "go to market" issues for TV Band Devices, and to develop a collaborative action plan that addresses immediate needs while maximizing the possibilities for future innovation and success throughout the wireless value chain. The workshop will begin with a tutorial review of the current FCC rules, followed by a round table panel discussion exploring these rules and discussing future requirements for Information Services databases supporting TV Band Devices.

Presentation by **Peter Stanforth**, *Spectrum Bridge*

* A brief summary of what TV White Space is and how the FCC envisions it being used.
* Examples of some of the trial uses to date.
* An overview of the rules related who and what can use TV white space;
  - o Specifically who is protected and how, and the definition and use of High Power and Low Power devices.
* OET database provider update
* Summary of the tertiary activities, including 802.11af, and likely timelines are for early and mass adoption

Panel, moderated by James Neel, *CRT Wireless*
Panelists:
Mark Gibson, *Comsearch*
Paul Lambert, *Marvell Semiconductor*
Rick Rotondo, *xG Technology*
Peter Stanforth, *Spectrum Bridge*
Neil Keon, *WSdB*

Tutorial IB: Radio-in-the-Loop: Design Tools for Software Radios

Regency D

Presented by **John Irza**, *The Mathworks*, USA

The design of next generation communications systems such as cognitive radios will be challenged by real world signals and environments that will be difficult to exhaustively simulate. As a result there is a need to enable engineers to include radio hardware in the design and verification process, allowing them to use actual over-the-air signals as part of their design process. To enable the integrated approach of using radio hardware in concert with design tools and simulation environments, it is also necessary to support streaming signal processing. This is in contrast to the traditional "batch" processing of offline data. In this tutorial we will highlight the advantages for designing wireless systems using radio hardware in the loop in a computational environment that supports streaming data processing. Examples of integrating MATLAB algorithms and Simulink communications system models with the USRP2 and other SDR hardware will be shown.

Tutorial IC: ETSI Reconfigurable Radio Systems (RRS)

Regency E

Presented by **Markus Mueck**, *Infineon Technologies Germany*, and **Andrea Lorelli**, *ETSI France*

The objective of this tutorial is to enable the participant:

- to understand the ETSI framework with a particular focus on the ETSI Reconfigurable Radio Systems (RRS) Technical Committee. Information will be given on the possible deliverables to be produced (Technical Reports (TR), Technical Specifications (TS), European Norm (EN), etc.) and the possibilities for interacting with ETSI RRS;
- to understand the ETSI RRS vision related to Cognitive Radio (CR) and Software Defined Radio (SDR);
- to understand ongoing interactions with regulatory bodies and possibilities for impacting related actions via ETSI RRS; and
- to understand the most relevant future study axes, related to commercial and military related applications of CR and SDR.

Tutorial 1D: Migrating Legacy Radios to the SCA

Regency F

Presented by **Toby McClean** and **Mike Williams**, *Zeligsoft*, Canada

Current software defined radios exist in two common forms: UML models; and/or source code. There is an industry wide desire to migrate a selected set of these radio to the SCA. Lead projects are finding it very costly and error prone to make a legacy radio SCA compliant. Some of the challenges: the steep learning curve associated with the SCA; transforming legacy models to the SCA; refactoring code to make it SCA compliant; ensuring compliance with specification; testing the new SCA components; and that the SCA itself imposes significant implementation challenges. With a Model-Based Engineering (MBE) approach to modernizing a radio, by migrating to SCA, it is possible for the quality of the radio to be increased while at the same time managing if not reducing the project costs. By combining MBE practices with specialized SCA tools the development team can: focus on ensuring the behavior and performance of the radio; leverage the knowledge inherent in an SCA-specific tool; leave the SCA aspects of the radio to the tool; and integrate the SCA tools and processes with their existing environment. This tutorial will demonstrate techniques and tools that will allow a development team to migrate from a "legacy radio' to an SCA radio using a model-based approach. We will start with legacy radio model and code assets and show a possible migration path to the SCA including deployment on a standard operating environment. The tool technology to be shown in this tutorial will be Spectra CX along with other commercially available software design tools used by radio developers.

10:00

Tutorial 1E: Open Component Portability Infrastructure (OpenCPI)

Potomac III & IV

Presented by **Michael Pepe**, *Mercury Federal Systems, Inc.*

Open Component Portability Infrastructure (OpenCPI) An open source software (OSS) software framework to simplify complexity & enable code portability of real-time systems o Middleware for Waveform-Ready™ Processing Platforms o Real-time middleware for embedded systems o Improved waveform code portability with standards-based interfaces o Increased interoperability using container technology o Open source software, www.OpenCPI.org, limits vendor lock-in OpenCPI is an innovative middleware solution that simplifies programming of heterogeneous processing environments consisting of field-programmable gate arrays (FPGA), general-purpose processors (GPP), digital signal processors (DSP), and high-speed switch fabrics. OpenCPI greatly improves code portability, interoperability, and performance in FPGA and DSP-based environments by providing well-defined waveform component APIs with a set of infrastructure building blocks that act as a hardware abstraction layer (HAL). OpenCPI simplifies the programming, integration and deployment of real-time systems to ultimately increase competition in this space. We propose to accomplish this by making the underlying real-time infrastructure and middleware into a technology commodity. Today's myriad communications standards and rapidly evolving new-generation waveforms have created a need to build communications systems that are ready to accept any present or future waveform. Waveform-Ready™ processing platforms combine the latest processor, transceiver, and interconnect technologies with the CPI to help customers meet this challenge. Building on the concepts introduced by the U.S. Government's Software Communications Architecture (SCA) standard, CPI extends component-based architectures into FPGAs and DSPs to decrease development costs and time to market through code portability, reuse, and ease of integration. CPI is based on 30 man-years of funding. OpenCPI is used in real-time signal processing for embedded, heterogeneous systems for communications, xxxINT (Signals, Communications, Electronics, etc. - Intelligence) and CIED (Counter Improvised Explosive Devices) in defense intelligence, surveillance and reconnaissance (ISR) systems.

Workshop 1F: Public Safety Communications I

Potomac V & VI

Sponsored by the Wireless Innovation Forum Public Safety Special Interest Group

This workshop brings together several individuals with diverse roles within the public safety community to discuss user requirements, technologies, and regulatory aspects for public safety communications systems.

Focus for this workshop is on how Software Defined Radio (SDR) and Cognitive Radio (CR) technologies/solutions can benefit the public safety user and the regulatory impact of such solutions.

10:00 Introduction, **Fred Frantz**, *L-3 Communications*

10:10 Advances in SDR/CR Technology, Industry Perspective, **Rick Taylor**, *Harris*

10:45 Advances in SDR/CR Technology, University Perspective, **S.M. Hasan**, *Virginia Tech*

11:20 Research and Evaluation of SDR/CR for Public Safety, **Dr. Nancy Merritt**, *NIJ*

11:55 Session 1 Wrap-up

15:15

Session 2A: SCA

Regency C

Chair: **Eric Christensen**, *General Dynamics C4 Systems*

15:15 "Implementing a Generic Front Panel for An SCA Radio" **Serge Harnois** (*Ultra Electronics - Tactical Communication Systems*, Canada); **Steve Bernier** (*The Communications Research Centre Canada*, Canada)

15:35 "How Different Messaging Semantics Can Affect SCA Waveform Applications" (Best of R&D Track) **Steve Bernier** (*The Communications Research Centre Canada*, Canada)

15:55 "A Path Toward Cost-effective SCA Compliance Testing" **James Ezick** (*Reservoir Labs*, USA); **Jonathan Springer** (*Reservoir Labs*, USA); **Vassily Litvinov** (*Reservoir Labs*, USA); **David Wohlford** (*Reservoir Labs*, USA)

16:15 "A SCA-Compliant Public Safety P25-FM3TR-VoIP Gateway" (Best of R&D Track) **Zhongren Cao** (*University of California*, San Diego, USA)

16:35 "SCA Waveform Applications Porting - Experience in Moving Past the Myths and Legends" (Invited Presentation) **Mark Turner** (*Harris Corporation*, USA)

16:55 "Attacking SDR/SCA Development Costs" (Invited Presentation) **Steve Jennis** (*PrismTech*, USA); Andrew Foster (*PrismTech Limited*, United Kingdom); **Paul Burns** (*Simplexity Communications*, Australia)

Gray = Invited Presentation
Blue = Best of R&D Track (The top papers in the Best of R&D Track will be featured in an upcoming special edition Springer Journal.)

15:15

Session 2B: Cognitive Radio I

Regency D

Chair: **James Neel**, *Cognitive Radio Technologies, LLC*

15:15 "Complexity Analysis of Systematic Spectrum Sensing for Cognitive Radio" **Jui-Chieh Lin** (*National Taiwan University*, Taiwan)

15:35 "A Survey of Basic Channel Selection Techniques for Cognitive Radios" **Benjamin C. Hilburn** (*Virginia Tech*, USA); **Timothy R. Newman** (*Virginia Tech*, USA); **Tamal Bose** (*Virginia Tech*, USA); **Shubha Kadambe** (*Rockwell Collins*, USA)

15:55 "Multi-Level Modeling and Simulation of Cognitive Radio Equipments" **Stephane Lecomte** (*Technicolor*, France); **Christophe Moy** (*Supelec*, France); **Pierre Leray** (*IETR/Supelec Campus de Rennes*, France)

16:15 "Joint Rate and Power Control using Distributed Algorithms in Cognitive Radio Network" **Uvaraj Rajasekaran** (*University of Surrey*, United Kingdom); **Kamran Arshad** (*University of Surrey*, United Kingdom); **Klaus Moessner** (*University of Surrey*, United Kingdom)

16:35 "Modeling Cognitive Radio Performance in High Spectral Density Signal Environments" **David A Leiss** (*Agilent Technologies Inc.*, USA); **Steve Sanelli** (*Agilent Technologies*, USA)

Session 2C: Education & Radio Challenge

Regency E

Chair: **Peter Farkas**, *TU Bratislava*

15:15 "SDR in Undergraduate Engineering Education" **Vuk Marojevic** (*Polytechnic University of Catalonia*, Spain); **Ismael Gomez** (*Polytechnical University of Catalonia*, Spain); **Antoni Gelonch** (*Polytechnic University of Catalonia*, Spain)

15:35 "Teaching Digital Communications in a Developing Country using a Low Cost Software Defined Radio Laboratory" **Yair Linn** (*PMC-Sierra*)

15:55 "Implementation of a Spectrum Sensing Based Emergency Radio Information System" (Invited Presentation) Md. Abdur Rahman (*Tokyo Institute of Technology (Tokyo-Tech)*, Japan)

16:15 "Feature Extraction Methods on a Novel Modulation Classification Technique for Cognitive Radio Applications" **Okhtay Azarmanesh** (*The Pennsylvani State University*, USA); **Pradyumna Desale** (*The Pennsylvania State University*, USA); **Chris Gardner** (*The Pennsylvania State University*, USA); **Sven G. Bilén** (*The Pennsylvania State University*, USA)

16:35 "RF Environment Behavior Modeling Based on 3-D Ray-Tracing and Neural Networks to Mitigate Multipath in Indoor Position Estimation" **Fermin Esparza Alfaro** (*University Of Calgary*, Canada); **Meenakshi Rawat** (*University of Calgary*, Canada); **Ramzi Darraji** (*University of Calgary*, Canada); **Karun Rawat** (*University of Calgary*, Canada); **Fadhel Ghannouchi** (*University of Calgary*, Canada); **Victor Torres** (*Universidad Publica de Navarra*, Spain); **Francisco Falcone** (*Universidad Publica de Navarra*, Spain)

16:55 "Packet Detection, Frequency Synchronization, and Channel Estimation/Equalization of Reconfigurable OFDM-Based Receivers for SDR Applications" **Mohammad Mojtaba Ebrahimi** (*University of Calgary*, Canada); **Seyed Aidin Bassam** (*University of Calgary*, Canada); **Mohamed Helaoui** (*University of Calgary*, Canada); **Fadhel Ghannouchi** (*University of Calgary*, Canada)

Expert Lecture 2D: Air Interface Innovations Applicable to Cognitive Radio Sysems

Regency F

Donald Steinbrecher, *Naval Undersea Warfare Center, USA*

Workshop 2E: Open Source in Military and Commercial Wireless Applications

Potomac III & IV

3:15 Why Open Source Software is Important to DoD, **John Scott**, *RadiantBlueTechnologies, Inc.*, USA

3:35 The Fairwaves SDR Platforms, **Alexander Chemeri**, *Fairwaves*, Russia

3:55 GNU Radio Directions, **Tom Rondeau**, *Center for Communications Research*, USA

4:15 Business Models For Open Source Air Interfaces, **John Glossner,** *Sandbridge Technologies*, USA

4:35 Open SDR, **Philip Balister**, *OpenSDR*, USA

Workshop 2F: Public Safety Communications II

Potomac V & VI

Sponsored by the Wireless Innovation Forum Public Safety Special Interest Group

This workshop brings together several individuals with diverse roles within the public safety community to discuss user requirements, technologies, and regulatory aspects for public safety communications systems.

Focus for this workshop is on how Software Defined Radio (SDR) and Cognitive Radio (CR) technologies/solutions can benefit the public safety user and the regulatory impact of such solutions.

15:15 Afternoon Introduction, **Fred Frantz**, *L-3 Communications*

15:25 Requirements from a Law Enforcement Perspective, **Deputy Chief Eddie Reyes**, *Alexandria PD*

16:00 Regulatory Perspective, **Dr. Bill Lane**, Chief Engineer, Public Safety Outreach and Operations Division, Public Safety and Homeland Security Bureau, *Federal Communications Commission*

16:35 The Role of the Public Safety SIG, **Fred Frantz**, Chair, *WInnF Public Safety Special Interest Group* (SIG)

17:10 Session 2 Wrap-up

Wednesday, 2 December

09:50

Session 3A: Security

Regency C

Chair: **Mark Turner**, *Harris Corporation*

09:50 "Instruction Set Extensions for Accelerating SNOW 3G on a Multithreaded Software Defined Radio Platform" (Best of R&D Track) **Chris Jenkins** (*University of Wisconsin--Madison*, USA)

10:10 "Settling a SDR Reference Security Architecture" **Rafael Aguado** (*Indra Sistemas S.A.*, Spain)

10:30 "New FPGA Security Features are Adding Assurance to SDR Fielded Systems" (Invited Presentation) **Ken Weidele** (*Xilinx*, USA); **John Hoffman** (*Xilinx*, USA)

Session 3B: Cognitive Radio II

Regency D

Chair: **Sherin Kamal**, *Science Applications International Corp.(SAIC)*

9:50 "Robust Automatic Modulation Classification and Blind Equalization: A Novel Cognitive Receiver" (Best of R&D Track) **Barathram Ramkumar** (*Virginia Tech*, USA); **Tamal Bose** (*Virginia Tech*, USA)

10:10 "Evaluation Optimization Techniques for Software Defined Radio - Cognitive Radio System Performance" **Nikhil Challa** (*Virginia Tech*, USA); **Jeong-O Jeong** (*Virginia Tech*, USA); **Carl B. Dietrich** (*Virginia Tech*, USA); **Timothy R. Newman** (*Virginia Tech*, USA); **Jeffrey Reed** (*Virginia Tech*, USA)

10:30 "Collaborative Adaptation of Cognitive Radio Parameters Using Ontology and Policy Approach" (Best of R&D Track) **Shujun Li** (*Northeastern University*, USA); **Mieczyslaw Kokar** (*Northeastern University*, USA); **David P. Brady** (*Northeastern University*, USA); **Jakub Moskal** (*Northeastern University*, USA)

10:50 "Robust Cyclic Cumulants Based Multiuser Automatic Modulation Classifier For Cognitive Radios" **Barathram Ramkumar** (*Virginia Tech*, USA); **Tamal Bose** (*Virginia Tech*, USA); Miloje Radenkovic (*University of Colorado at Denver and the Health Sciences Center*, USA)

11:10 "A Cognitive Radio Prototype For Spectrum Sensing Application" **Michael Steiner** (*Virginia Tech*, USA); **Tamal Bose** (*Virginia Tech*, USA); **S M Hasan** (*Virginia Tech*, USA); **Sam Shearman** (*National Instruments*, USA); **Ahsan Aziz** (*National Instruments*, USA)

11:30 "Prototype of a Spectrum Sniffer Software Implementation for ISM Bands" **Ermano Picco** (*ST Microelectronics*, Italy)

Gray = Invited Presentation
Blue = Best of R&D Track (The top papers in the Best of R&D Track will be featured in an upcoming special edition Springer Journal.)

Session 3C: Communications Signal Processing I

Regency E

Chair: **Kamran Arshad**, *University of Surrey*

09:50 "Polyphase Filter Bank for Unequal Channel Bandwidths and Arbitrary Center Frequencies-I" (Best of R&D Track) **fred harris** (*San Diego State Univ*, USA); **Elettra Venosa** (*Seconda Universita' di Napoli*, Italy); **Xiaofei Chen** (*San Diego State University*, USA)

10:10 "Polyphase Filter Bank with Unequal Bandwidths and Unequal Spectral Centers" **fred harris** (*San Diego State Univ*, USA)

10:30 "Polyphase Filter Bank for Unequal Channel Bandwidths and Arbitrary Center Frequencies-II" **fred harris** (*San Diego State Univ*, USA); **Xiaofei Chen** (*San Diego State University*, USA); **Elettra Venosa** (*Seconda Universita' di Napoli*, Italy)

10:50 "Reception Performance of Flexible Wireless System Receiving Multi-Signals Simultaneously" **Hiroyuki Shiba** (*NTT*, Japan)

09:50

Workshop 3D: Regulatory I

Regency F

Sponsored by the Wireless Innovation Forum Regulatory Committee

This one day workshop will explore the evolving regulatory landscape impacting the deployment of advanced wireless technologies around the world. Co-hosted for the second consecutive year by Peter Tenhula, Chair of the Wireless Innovation Forum's Regulatory Committee, and Paul Kolodzy, Vice Chair of the Regulatory Committee, the workshop will again bring together a multidisciplinary line-up of regulatory/public policy officials and experts from around the world – technologists/engineers, economists, social scientists, and even lawyers. Please join us as we develop a regulatory agenda that promotes the adoption of advanced wireless technologies.

Introductory Address – Mr. Karl B. Nebbia, Associate Administrator, *U.S. National Telecommunications and Information Administration, Office of Spectrum Management*

Morning Panel: "The Next Steps to Implementing the U.S. FCC's TV White Space Rules and Furthering Efforts Around the World to Cash in on the 'Digital TV Dividend'"

ABSTRACT: In the U.S., the FCC is expected to finalize its regulations governing the operation of unlicensed devices in the unused portions of the television spectrum by the end of September 2010. In the U.K., OFCOM is on the verge of taking a leadership role in innovative wireless technologies by authorizing the use of cognitive devices in the so-called "interleaved" spectrum between new digital television channels. The rest of the world is watching closely and poised to follow suit. Following up on the two Forum workshops held in June and September, this panel of experts will provide analysis of the FCC's revised regulations, OFCOM's proposals and other global initiatives to promote spectrum sharing in the TV bands and beyond. Issues to be addressed will include (1) next steps for companies interested in deploying technologies in the TV bands; (2) other pending proposals and initiatives; (3) possible scenarios for success or disaster in these prime spectrum bands for new and innovative broadband applications.

MODERATOR: **Bruce Oberlies**, *Motorola*, Chair, Wireless Innovation Forum

PARTICIPANTS:

Allan Stillwell, *FCC OET*
Robert Sutton, *TDK RF Solutions*
Paul Garnett, *Microsoft Corp.*
Hiroshi Harada, Director of Ubiquitous and Mobile Communications, *NIC*

Tutorial 3E: IPA

Potomac III & IV

Presented by **Peter G. Cook**, *Hypres, Inc.*, USA, and **James Neel**, *Cognitive Radio Technologies, LLC*, USA

Information Systems are having a profound impact on our society, invoking great changes, with an impact similar to those brought about by steam power, electricity, and electronic communication. Communication Systems are a major item of interest for the Wireless Innovation Forum. We are also looking at the consequences of system expansion that leads to intersection, interaction, and integration of independently developed systems, and the resulting Complex Systems. As the means by which data is exchanged between system participants , the role of Communication Systems can best be understood in context of the architecture of Complex Systems. The Cognitive Radio Working Group and the Public Safety Special Interest Group recently released volume 1 of the Information Process Architecture (IPA) project - a multi-part effort to improve understanding of how information and communications systems are evolving to exhibit increasingly intelligent behavior, grow to interact with one another, and enable new applications and capabilities. Future work will further refine these concepts, develop new applications, and further explore how understanding context can improve the performance of automatic information systems. In this tutorial we cover the work to date of the IPA project and describe our future plans.

Tutorial 3F: Two-Thirds of SDR is SD

Potomac V & VI

Presented by **Bruce Trask,** *MDE Systems Inc,* USA

Developing Software Define Radio (SDR) Software is hard. Some could make a case that is it one of the most difficult software domains to tackle. Given the complexities and changes of the problem domain and the complexities and changes in the solution domain, your company's technology has to be at a maximum to even have a chance of success. Many teams have reached a complexity ceiling when using their current tools, techniques and infrastructure. Many engineers and their teams are buried in software artifacts that do not effectively capture their domain. This tutorial will cover how to tackle the above with a host of advanced software technologies including Model Driven Engineering (MDE), Software Product Lines (SPL), Distributed Real-time and Embedded (DRE) technologies as well as Agile Software Development (ASD) all the while tailoring the above to the uniquenesses of the SDR domain. It will show how these can be used in synergy to scalably tackle the complexities of the SDR domain.

Tutorial 3G: A Graphical Approach to FPGA Programming

Potomac 6B

Presented by **Christian Amadasun**, *National Instruments*

In this session you will learn how to use the LabVIEW FPGA Module to program the NI FlexRIO. The following topics will be discussed:

- Elements of the FPGA environment (Memory, FIFO's, Clocks, I/O Nodes, logic)
- Optimizing your LabVIEW FPGA VI using parallel execution and pipelining
- The Single Cycle-Timed Loop
- Importing pre-existing VHDL IP in the LabVIEW FPGA environment
- Simple Debugging techniques

Through-out the session the use of the software environment as well as code samples will be presented. The session is ended with a simple hardware and software demonstrated.

13:45

Session 4A: System Imiplementation and Test I

Regency C

Chair: **Fanny Mlinarsky**, *OctoScope*

13:45 "Insights into building an SCA Test Laboratory" (Invited Presentation) **Randy Navarro** (*SAIC*, USA)

14:05 "Implementation of Smart Antenna and Transceiver API on OSSIE Platform for Wireless Innovation Forum Standards" (Best of R&D Track) **Chiyoung Ahn** (*Hanyang University*, Korea); **June Kim** (*Hanyang University*, Korea); **SeungWon Choi** (*Hanyang University*, Korea)

14:25 "Rapid Prototyping of a SDR Based Reconfigurable MIMO-OFDM Testbed" **Sabares Moola** (*Virginia Tech*, USA); **S M Hasan** (*Virginia Tech*, USA); **Carl B. Dietrich** (*Virginia Tech*, USA); **Jeffrey Reed** (*Virginia Tech*, USA)

14:45 "Addressing SDR MIMO Mixed-Signal Testing Challenges" (Invited Presentation) **Greg Jue** (*Agilent Technologies*, USA); **Brad Frieden** (*Agilent*, USA)

15:05 "Hardware-in-the-Loop Design Verification Testing for Software-Defined Radio Waveforms" **Ying Niu** (*Raytheon*, USA); **David Mussmann** (*Raytheon*, USA)

Session 4B: Cognitive Radio III

Regency D

Chair: **S. M. Hasan**, *Virginia Tech*

13:45 "A Sub-Space Method to Detect Multiple Wireless Microphone Signals in TV Band White Space" (Best of R&D Track) **Dinesh Datla** (*Virginia Tech*, USA); **Harpreet S Dhillon** (*Virginia Tech*, USA); **Jeong-O Jeong** (*Virginia Tech*, USA); **Michael Benonis** (*Virginia Tech*, USA); **Michael Buehrer** (*Virginia Tech*, USA); **Jeffrey Reed** (*Virginia Tech*, USA)

14:05 "Cognitive Radio Testbed - Real-World Electromagnetic Spectrum Survey, Modeling, and Simulation" **Trang Mai** (*Naval Research Laboratory*, USA); **Christopher R. Anderson** (*United States Naval Academy*, USA); **Joseph Molnar** (*Naval Research Laboratory*, USA)

14:25 "Applying Cognitive Radio Concepts to Next Generation Electronic Warfare" **Randall Janka** (*Zeta Associates*, USA)

14:45 "Practical Considerations for Cognitive Radio Networking" (Invited Presentation) **James Neel** (*Cognitive Radio Technologies*, LLC, USA)

15:05 "Using Reactive Inferencing as an Adaptive State Machine in a Terminal System" (Invited Presentation) **Vincent J Kovarik** (*Harris Corporation*, USA)

15:25 "Grey Systems Theory Applications to Communications" (Best of R&D Track) **Ashwin Amanna** (*Virginia Tech*, USA); **Ratchaneekorn Thamvichai** (*Virginia Tech*, USA); Matthew J Price (*Virginia Tech*, USA)

Session 4C: Communications Signal Processing II

Regency E

Chair: **fred harris**, *San Diego State University*

13:45 "Compensation of Symbol Clock Offset and Carrier Frequency Offset in the Multi-Band DFT spreading OFDM System" **Sang Burm Ryu** (*Chungbuk National University*, Korea); **Heung-Gyoon Ryu** (*Chungbuk National University*, Korea); **Jin-Up Kim** (ETRI, Korea)

14:05 "Design and Performance Tradeoffs in Digital Radio Processing Architectures" **Mujun Song** (*Air Force Institute of Technology*, USA); **Jason Pennington** (*Air Force Institute of Technology*, USA); **Mark D. Silvius** (*Air Force Institute of Technology*, USA); **Ryan Thomas** (*Air Force Institute of Technology*, USA); **Richard K. Martin** (*Air Force Institute of Technology*, USA); **Charles Bostian** (*Virginia Tech*, USA)

14:25 "Experimental Results on All-Digital Implementation of the Phase Locked-Loop for Software Defined Radio" **Alexandre Marsolais** (*Ultra-TCS*, Canada); **Doan Nguyen Vo** (*Ultra TCS*, Canada)

14:45 "Analyzing the Effect of Power Control Algorithms on the Receiver's Computing Resource Consumption" (Best of R&D Track) **Ismael Gomez** (*Polytechnical University of Catalonia*, Spain); **Vuk Marojevic** (*Polytechnic University of Catalonia*, Spain); **Antoni Gelonch** (*Polytechnic University of Catalonia*, Spain)

15:05 "On Frequency Lock Detection for Low Signal-to-Noise Ratio (SNR) QAM Signals" (Best of R&D Track) **Doan Nguyen Vo** (*Ultra TCS*, Canada)

15:25 "Performance Evaluation and Parameters Sensitivity of the OFDM modulation in HF Transmission" **R. B. Dutra** (*Brazilian Research Institute/ Digital Systems Group*, Brazil); **Mariane Rembold Petraglia** (*Federal University of Rio de Janeiro*, Brazil); **A. C. Mendes** (*Brazilian Research Institute/ Digital Systems Group*, Brazil)

Workshop 4D: Regulatory II

Regency F

Sponsored by the Wireless Innovation Forum Regulatory Committee

This is a continuation of a one day workshop that will explore the evolving regulatory landscape impacting the deployment of advanced wireless technologies around the world. Co-hosted for the second consecutive year by Peter Tenhula, Chair of the Wireless Innovation Forum's Regulatory Committee, and Paul Kolodzy, Vice Chair of the Regulatory Committee, the workshop will again bring together a multidisciplinary line-up of regulatory/public policy officials and experts from around the world – technologists/ engineers, economists, social scientists, and even lawyers. Please join us as we develop a regulatory agenda that promotes the adoption of advanced wireless technologies.

(Panel descriptions continue on next page ...)

13:45

Workshop 4D: Regulatory II (continued)

Regency F

Sponsored by the Wireless Innovation Forum Regulatory Committee

Panel 2: Applications and Opportunities for Sharing of Wireless Spectrum for Innovative Broadband Applications

ABSTRACT: In the U.S., the Obama Administration is taking steps to meet the urgent need for more spectrum suitable for fixed and mobile broadband applications. The FCC's National Broadband Plan and President Obama's Presidential Memorandum have established a target of finding 500 MHz of new spectrum for over the next 10 years. The President's memo and the FCC's plan also recognize that relying solely on traditional reallocation and relocation approaches will not meet this burgeoning demand and that sharing arrangements are needed. This panel will explore the technical and regulatory mechanisms that will facilitate efficient utilization of the "open spaces" in the spectrum bands along with accompanying challenges to dynamic sharing solutions.

MODERATOR: Peter Tenhula, *Shared Spectrum Company*

PANELISTS:

Byon Barker, Chief, Strategic Spectrum Planning and Reform Division, Office of Spectrum Management, *NTIA*

Mary Brown, Director of Technology and Spectrum Policy, *Cisco Systems, Inc.*

Keith Nolan, *Trinity College*, Dublin

Scott Deutchman, Deputy Chief Technology Officer, Telecommunications, *U.S. Office of Science and Technology Policy*

Panel 3: The World's Regulatory View – a WRC 12 Preview

ABSTRACT: On the agenda for the upcoming World Radio Conference (WRC) are several items that may have long-term impacts on the wireless innovation community's hopes of global penetration of smarter, reconfigurable devices. This panel of international experts will provide a timely preview of this important event. They will address the important issues now under consideration and debate within the international community and working groups, including: (1) how can the ITU facilitate the deployment of software defined radios (SDR) and cognitive radio systems (CRS) in the various existing radiocommunication services; (2) are changes to the ITU Radio Regulations needed to enable these technologies; and (3) how do the definitions, description, or characterization of SDR or CRS effect the studies and debates?

MODERATOR: **Paul Margie**, Partner, *Wiltshire Grannis*, and Co-Chair, FCC WRC Advisory Committee

PANELISTS:

[European perspective]: **Horst Menenga**, *Federal Network Agency for Electricity, Gas, Telecommunications, Posts and Railways*

[US perspective]: **Stephen Ward**, *Micro Managers*

Expert Lecture 4E: Multipath Interference Characterization in Wireless Comunication Systems

Potomac III & IV

Michael Rice, *Brigham Young University*

- Multiple paths between transmitter and receiver
- Constructive/destructive interference
- Dramatic changes in received signal amplitude and phase as a result of small changes (l/2) in the spatial separation between a receiver and transmitter.
- For Mobile radio (cellular, PCS, etc) the channel is time-variant because motion between the transmitter and receiver results in propagation path changes.
- Terms: Rayleigh Fading, Rice Fading, Flat Fading, Frequency Selective Fading, Slow Fading, Fast Fading ….
- What do all these mean?

Tutorial 4F: Rapid Prototyping Digital SCA-Based SDR Waveforms with OSSIE: Hands-On)

Potomac 6B

Presented by **Carl B. Dietrich**, *Virginia Tech, USA;* **Frank Kragh**, *Naval Postgraduate School, USA;* and **Donna Miller**, *Naval Postgraduate School, USA*

In this hands-on tutorial, participants will become familiar with easy-to-use, open-source tools for rapid prototyping and interactive control of SCA-based SDR waveform applications. After developing example applications, participants will use the tools to develop a digital communications waveform. The session begins with a brief overview of software defined radio including basic concepts, education, research topics, and the Software Communications Architecture (SCA). OSSIE, Virginia Tech's open source implementation based on the SCA, is introduced through hands-on activities developed by the Naval Postgraduate School and Virginia Tech. Lab materials as well as the OSSIE core framework and associated rapid development and application software are provided to participants and are also available for free download.

Tutorial 4G: Extending the SCA to meet international security needs

Presented by **Scott Leubner** and **Chuck Linn**, *Harris Corporation*

A key aspect of military software defined radios is the ability to provide appropriate levels of security to ensure that information contained within the radio, and information transferred between radios is protected as expected. A key challenge in meeting security requirements with public standards is the ability to adequately protect limited access or sovereign interests. This tutorial will present and explore the work of the Wireless Innovation Forum's International Radio Security Services API Task Group in the specification and development of an SCA based category 1 API and associated techniques supporting coalition and national interests.

Thursday, 2 December

09:50

Session 5A: System Implementation and Test II

Regency C

Chair: **Fanny Mlinarsky**, *OctoScope*

09:50 "A Real-Time Algorithm Design and Prototyping Platform for MIMO Research" **Murat Torlak** (*The University of Texas at Dallas*, USA); **Sam Shearman** (*National Instruments*, USA); **JIN Yuan** (*University of Texas at Dallas*, USA); **Douglas E Kim** (*The University of Texas at Dallas*, USA)

10:10 "A SDR Testbed Architecture for ACM, MIMO and DSA in Military Applications" **Patrik Eliardsson** (*Swedish Defence Research Agency (FOI)*, Sweden); **Ulrika Uppman** (*Swedish Defence Research Agency (FOI)*, Sweden)

10:30 "DICOMT Software Defined Radio for Search and Rescue" **Robin Addison** (*Communications Research Centre*, Canada)

10:50 "Implementation of an SDR platform using GPU and its Application to 2x2 MIMO WiMAX System" (Best of R&D Track) **JaeHyuk Ju** (*Hanyang University*, Korea); **Chiyoung Ahn** (*Hanyang University*, Korea); **June Kim** (*Hanyang University*, Korea); **Seungheon Hyeon** (*Hanyang University*, Seoul, Republic of Korea, Korea); **SeungWon Choi** (*Hanyang University*, Korea)

11:10 "Unity Multiband SDR for Public Safety" (Invited Presentation) **Richard Taylor** (*Harris Corporation*, USA)

Tutorial 5B: Emerging Commercial Wireless and Cognitive Radio Standards

Regency D

Chair: **James Neel**, *Cognitive Radio Technologies, LLC*

Rather than converging to a common protocol, the number of wireless standards continues to explode. While SDR is enables the move to multimode devices (even octo-mode devices), just staying abreast of all of the standards is a full time job. This tutorial is intended to help the audience keep track of the wireless world by briefly touching on critical aspects of emerging wireless standards. With particular emphasis given to the TV White Space standards, planned topics include:

- TV White Space Standards (802.22, 802.11af, CogNeA, 802.16h)
- Cellular standards (3GPP/3GPP2, cdma2000, TD-SCDMA, LTE, WiMAX)
- Wireless LAN standards (802.11 a/b/g/n, fast roaming, mesh, 802.11y, vertical handoffs)
- Wireless PAN standards (Zigbee, WiMedia, Bluetooth, WiBree, Wireless USB)
- Next Generation Cellular Standards (802.16j, 802.16m, LTE-Advanced)
- Satellite deployments (Iridium, GlobalStar, INMARSAT)
- Underlying communications theory of emerging standards (OFDM, MIMO, Antenna Array Systems)

Note: A version of this tutorial is updated and given every year at VT's conference and normally runs about 4 hours. See http://crtwireless.com/EWS_09.html for the 2009 version.

Session 5C: Waveform and Software Design

Regency E

Chair: **Daniel S. Iancu**, *Optimum Semiconductor Technologies*

9:50 "Computer Generation of Platform-Adapted Physical Layer Software" **Yevgen Voronenko** (*Carnegie Mellon University*, USA); **Volodymyr Arbatov** (*Carnegie Mellon University*, USA); **Christian R Berger** (*Carnegie Mellon University*, USA); **Ronghui Peng** (*University of Utah*, USA); **Markus Pueschel** (*Carnegie Mellon University*, USA); **Franz Franchetti** (*Carnegie Mellon University*, USA)

10:10 "Radio Waveform Development System providing an integrated approach to SDR Waveform Design and Implementation" **Nirali Patel** (*Coherent Logix, Inc.*, USA); **Kevin Shelby** (*Coherent Logix, Inc.*, USA); **Brian A. Dalio** (*Coherent Logix, Inc.*, USA)

10:30 "Describing Radio Hardware and Software Using OWL for Over-The-Air Software Download" **Lubomir Stanchev** (*Indiana Univ Purdue Univ Fort Wayne*, USA); **Todor Cooklev** (*Indiana University Purdue University Fort Wayne*, USA)

10:50 "Resource Management with Real-Time Complexity Monitoring in Software-Defined Radios" **Joseph D. Gaeddert** (*Virginia Tech*, USA); **Jeffrey Reed** (*Virginia Tech*, USA)

11:10 "Component-based Waveform Development: the Nucleus Tool Flow for Efficient and Portable SDR" **Jeronimo Castrillon** (*RWTH Aachen University*, Germany); **Stefan Schürmans** (*RWTH Aachen University*, Germany); **Anastasia Stulova** (*RWTH Aachen University*, Germany); **Weihua Sheng** (*RWTH Aachen University*, Germany); **Torsten Kempf** (*RWTH Aachen University Germany*, Germany); **Aamir Ishaque** (*RWTH Aachen University*, Germany); **Rainer Leupers** (*RWTH Aachen University*, Germany); **Gerd H. Ascheid** (*RWTH Aachen University*, Germany); **Heinrich Meyr** (*RWTH Aachen University*, Germany)

11:30 "'Open Vector Radio,' a C Dialect Standard Proposal for High Performance Software Baseband Coding" (Invited Presentation) **Phil Moorby** (*Sigmatix, Inc*, USA); David Kelf (*Sigmatix, Inc*, USA); **Yuan Lin** (*Sigmatix, Inc*, USA)

Gray = Invited Presentation
Blue = Best of R&D Track (The top papers in the Best of R&D Track will be featured in an upcoming special edition Springer Journal.)

09:50

Workshop 5D: Analysts I

Regency F

SDR has begun to move beyond the innovators and early adopters as defined by Geoffrey Moore in "Crossing the Chasm" into the early majority phase defining the mainstream market. In this phase, adopters select a technology not because it is innovative or visionary but because it has been shown to successfully solve a problem within their specific market.

This workshop, hosted by Manuel Uhm of Xilinx and Chair of the Wireless Innovation Forum User Requirements Committee will explore the use of SDR and SDR technologies in commercial, civil and defense markets, future trends, and key challenges that need to be addressed in further advancing SDR technologies into the mainstream.

09:50 Welcome and Introductions, **Manuel Uhm**, *Xilinx*

10:00 "Self-optimization and Cognitive Radio in Commercial Wireless Infrastructure"**Aditya Kaul**, *ABI Research*

10:35 **Brad Curran**,*Frost and Sullivan*

11:10 **David Krebs** and **Chris Rezendes**, *VDC*

Workshop 5E: SDR in Space

Potomac V & VI

Workshop Organizers: **Dr. R. Scott Erwin** & **Dr. Jim Lyke**, Space Vehicles Directorate, *Air Force Research Laboratory*

This workshop seeks to gather interested parties from government, industry, and academia to discuss the prospects for and technical challenges associated with deploying software-defined radio technologies on space platforms. The objectives of the workshop are:

- To provide a forum for discussion of the potential capabilities enabled by and value provided by the incorporation of SDR technologies on space-based platforms;
- To establish the current state-of-the-art in the incorporation of SDR technologies for space platforms and discuss the technical challenges yet to be overcome; and
- To discuss planned future investments and deployments of SDR technologies on space-platforms for experimental or operational use.

The morning session will include presentations by:

- Space SDR and the CoNNeCT Program, **Richard Reinhart**, *NASA Glenn Research Center*
- Software Defined Payloads - The Challenge Ahead, **Piero Angeletti**, *European Space Agency*
- Facilitating Third Party Waveform Porting on Spaceborne SDR platforms, **Jerry Brand**, *Harris Corporation*

Expert Lecture 5F: GNU Radio: Introduction and Computational Capabilities

Potomac V & VI

Presented by Tom Rondeau, *Center for Communications Research*, USA

Session 5G: Processors

Potomac 6B

Chair: **Raghavan Muralidharan**, *Tata Power SED*, India

09:50 "Data Packet Processor Core"**Manuel Muro** (*Digital Data Innovations*, USA)

10:10 "Leveraging Embedded Heterogeneous Processors for Software Defined Radio Applications" **Almohanad Fayez** (*Virginia Tech*, USA); **Qinqin Chen** (*Virginia Tech*, USA); **Jeannette Nounagnon** (*Virginia Tech*, USA); **Charles Bostian** (*Virginia Tech*, USA)

10:30 "Multi-Ghz Software and Hardware Platform for Software Defined Radio" **Chen Chang** (*BEEcube Inc.*, USA)

10:50 "A Study on the Hardware Reconfiguration Schemes and their Applications on SDR-based Mobile Communications" **Bong-Guk Yu** (*Georgia Institute of Technology*, USA); **Sangchul Oh** (*ETRI*, Korea); **Hong-Soog Kim** (*ETRI*, Korea); **Kyutae Lim** (*Georgia Institute of Technology*, USA)

11:10 "SDR PHY Evolution: How Bandwidth is Driving Architectural Change (Invited Presentation) **Manuel Uhm** (*Xilinx*, USA)

11:30 "Full-Reconfigurable Interleaver Architecture for High-Performance SDR Applications" **Renaud Pacalet** (*Telecom ParisTech*, France); **Jair Gonzalez** (*Telecom Paristech*, France)

Thursday, 2 December

13:45

Session 6A: Applications

Regency C

Chair: **Sanjay Jinturkar**, *Ikanos Communications*, USA

13:45 "Implementation and Evaluation of Distributed Control and Data Channel Coordination Algorithms for V2V Dynamic Spectrum Access" **Onur Altintas** (*Toyota Info-Technology Center*, Japan); **Mitsuhiro Nishibori** (*Toyota InfoTechnology Center*, Japan); **Rama K Vuyyuru** (*Toyota Info Technology Center*, USA, USA); **Youhei Fujii** (*Kyushu Institute of Technology*, Japan); **Kota Nishida** (*Kyushu Institute of Technology*, Japan); **Yuji Oie** (*Kyushu Institute of Technology*, Japan); **Kazuya Tsukamoto** (*Kyushu Institute of Technology*, Japan); **Masato Tsuru** (*Kyushu Institute of Technology*, Japan); **Abdulrahman Al-Abbasi** (*University of Electro-Communication*, Japan); **Takeo Fujii** (*The University of Electro-Communications*, Japan); **Srikanth Pagadarai** (*Worcester Polytechnic Institute*, USA); **Alexander M. Wyglinski** (*Worcester Polytechnic Institute*, USA)

14:05 "Software Defined Implementation of MPEG4 decoder on Sandblaster SB3500 DSP" (Best of R&D Track) **Vaidyanathan Ramadurai** (*Optimum Semiconductor Technologies Inc.*, USA); **Mayan Moudgill** (*Sandbridge Technologies*, USA); **Daniel S Iancu** (*Optimum Semiconductor Technologies*, USA); **Gary Nacer** (*Sandbridge Technologies*, USA); **John Glossner** (*Sandbridge Technologies*, USA)

14:25 "Dynamically Reconfigurable Software Defined Radio for GNSS Applications" **Alison Brown** (*NAVSYS Corporatiaon*, USA); **Nigel Thompson** (*NAVSYS Corporation*, USA)

14:45 "FPGAs Tackle Signal Processing Tasks for a VPX Beamforming System" (Invited Presentation) **Rodger Hosking** (*Pentek*, USA)

15:05 "Sphere Detector for 802.16E Broadband Wireless Systems Implementation on FPGAs using High-level Synthesis Tools" (Best of R&D Track) **Juanjo Noguera** (*Xilinx, Inc.*, Ireland); **Stephen Neuendorffer** (*Xilinx*, USA); **Sven Van Haastregt** (*Xilinx*, USA); **Jesús Barba** (*University of Castilla-La Mancha*, Spain); **Kees Vissers** (*Xilinx*, USA); **Chris Dick** (*Xilinx*, USA)

15:25 "Extensible Baseband DSPs, Tools and Multi-Core Architectures for Low-Power 4G SDR Silicon Platforms" (Invited Presentation) **Chris Rowen** (*Tensilica*, USA)

Gray = Invited Presentation
Blue = Best of R&D Track (The top papers in the Best of R&D Track will be featured in an upcoming special edition Springer Journal.)

Session 6B: System Implementation and Test III

Regency D

Chair: **Fanny Mlinarsky**, *octoScope*, USA

13:45 "Labview Channel Estimator" **Fanny Mlinarsky**, **Sam MacMullan, Ph.D.** (*octoScope*, USA)

14:05 "Port Testing in a Dual-Star Network: Embedded LANs for RF" **Steven Groves** (*Harris*, USA)

14:25 "Clock Scaling Methods For Power Constrained Radios" (Invited Presentation) **John Shanton** (*Thales Communications, Inc*, USA)

14:45 "Real-Time, Software-Based Characterization of Receiver Dynamic Channel Performance on an SDR Development Platform" **Brian A. Dalio** (*Coherent Logix, Inc.*, USA); Ivan Aguayo (*Coherent Logix, Inc.*, USA)

15:05 "On The Use of Scrubbing for SEU Mitigation" **Rainer Storn** (*Rohde & Schwarz GmbH & Co. KG*, Germany)

Session 6C: Networks

Regency E

Chair: **Sanyogita Shamsunder**, *Verizon Wireless*, USA

13:45 "Design Challenges for Robust Ground-to-Ground Waveforms for Tactical Software-Defined Radio Ad-Hoc Networks" **Sebastian Hanigk** (*Universität der Bundeswehr München*, Germany)

14:05 "Fundamental Issues of Wireless Distributed Computing in SDR Networks" (Best of R&D Track) **Dinesh Datla** (*Virginia Tech*, USA); **S M Hasan** (*Virginia Tech*, USA); **Jeffrey Reed** (*Virginia Tech*, USA); **Tamal Bose** (*Virginia Tech*, USA)

14:25 "Software Defined Radio Based Wireless Grids" **Xuetao Chen** (*Virginia Tech*, USA); **S M Hasan** (*Virginia Tech*, USA); **Tamal Bose** (*Virginia Tech*, USA); **Jeffrey Reed** (*Virginia Tech*, USA)

14:45 "Design of Modular SDR Architecture for Resource Constrained MANET" **Dhadesugoor R. Vaman** (*Priarie View A&M University*, USA); **Raghavan Muralidharan** (*Tata Power SED*, India); **Swapna Raj** (*Prairie View A&M University*, USA)

15:05 "Testing Multi-Services Mobile Adhoc Networks Effectively" **Sherin Kamal** (*SAIC*, USA); **JD. Aishman** (*SAIC*, USA)

15:25 "Policy-Based Energy Efficient Data Report Method for Multi-Mode Wireless Sensor Networks" **Kosuke Yamazaki** (*KDDI R&D Laboratories Inc.*, Japan); **Issei Kanno** (*KDDI R&D Laboratories Inc.*, Japan); **Yuji Ikeda** (*KDDI R&D Laboratories Inc.*, Japan); **Hiroyasu Ishikawa** (*KDDI R&D Laboratories Inc.*, Japan)

13:45

Workshop 6D: Analysts II

Regency F

SDR has begun to move beyond the innovators and early adopters as defined by Geoffrey Moore in "Crossing the Chasm" into the early majority phase defining the mainstream market. In this phase, adopters select a technology not because it is innovative or visionary but because it has been shown to successfully solve a problem within their specific market.

This workshop, hosted by Manuel Uhm of Xilinx and Chair of the Wireless Innovation Forum User Requirements Committee will explore the use of SDR and SDR technologies in commercial, civil and defense markets, future trends, and key challenges that need to be addressed in further advancing SDR technologies into the mainstream.

13:45 "Changes in the Mobile Infrastructure Market" **Joe Madden**, *Mobile Experts*

14:20 "The Challenge of Spectrum Sharing and How To Embrace It" **Matthew Botwin**, *The Regent Square Group*

14:40 "Opportunities for Innovative Wireless Technologies that Enable Future Intelligent Transportation System Applications" **Craig Pickering**, *Booz Allen Hamilton*

15:00 Panel Discussion

Workshop 6E: SDR in Space II

Potomac III & IV

Workshop Organizers: **Dr. R. Scott Erwin** & **Dr. Jim Lyke**, Space Vehicles Directorate, *Air Force Research Laboratory*

This workshop seeks to gather interested parties from government, industry, and academia to discuss the prospects for and technical challenges associated with deploying software-defined radio technologies on space platforms. The objectives of the workshop are:

- To provide a forum for discussion of the potential capabilities enabled by and value provided by the incorporation of SDR technologies on space-based platforms;
- To establish the current state-of-the-art in the incorporation of SDR technologies for space platforms and discuss the technical challenges yet to be overcome; and
- To discuss planned future investments and deployments of SDR technologies on space-platforms for experimental or operational use.

Afternoon Panel Session: Enablers and Impediments for SDR in Space
Chair: R. Scott Erwin
Presentations:

- "Spaceborne SDRs: The key to tactical flexibility and spectral efficiency for space systems,"Christopher Huffine, *Naval Research Lab*
- "Open Architectures for Space Software-Defined Radios" **John Liebetreu**, *General Dynamics AIS*

6F: SCA Next Roll Out

Potomac V & VI

Extended battery life and operator response on small processors have become primary requirements for the SCA and JTRS program. Given these and a host of other drivers SCA Next has been restructured to better accommodate a variety of form factors from small radios to prime-power, multi-channel sets. SCA Next has a number of significant changes, most notably: CORBA is no longer required; compliance is flexible – permitting the set to be tailored to the mission and a new "push" architecture reduces messaging traffic and enables faster boot times.

This marks the public release of the SCA Next specification and the intent of this session is to explore some of its technical highlights and discuss strategies for its application to new platforms and domains.

Agenda

- SCA Next Introduction and Overview
- SCA Next Highlights
- Way Forward
- Q&A

Friday, 3 December

08:30

Session 7A: Waveform and Software Design II

Regency C

Chair: **Richard Taylor**, *Harris Corp.*, USA

08:30 "Interference Alignment Using NI FlexRIO" (Best of R&D Track) **N. Prasanth Anthapadmanabhan** (*University of Texas at Austin*, USA); **J. Saul Duran** (*University of Texas at Austin*, USA); **Kyle Miller** (*University of Texas at Austin*, USA); **Vidur Bhargava** (*University of Texas at Austin*, USA); **Shanmugam Sambasevam** (*University of Texas at Austin*, USA); **Takao Inoue** (*National Instruments*, USA); **Ahsan Aziz** (*National Instruments*, USA); **Sriram Vishwanath** (*University of Texas at Austin*, USA)

08:50 "Rapid Prototyping of Communication Waveforms from a High-level Design Language" **Mark Beardslee** (*Coherent Logix, Inc.*, USA); **Matt Hall** (*Coherent Logix, Inc.*, USA); **Zhong Shang** (*Coherent Logix, Inc.*, USA)

09:10 "Interfacing a Reasoner with an SDR Using a Thin, Generic API: A GNU Radio Example" **Jakub Moskal** (*Northeastern University*, USA); **Mieczyslaw Kokar** (*Northeastern University*, USA); **Shujun Li** (*Northeastern University*, USA)

09:30 "Complexity Analysis of Software Defined DVB-T2 Physical Layer" **Stefan Grönroos** (*Åbo Akademi University*, Finland); **Kristian Nybom** (*Åbo Akademi University*, Finland); **Jerker Björkqvist** (*Åbo Akademi University*, Finland)

09:50 "A Lightweight Dataflow Approach for Design and Implementation of SDR Systems" **Chung-Ching Shen** (*University of Maryland*, USA); **William Plishker** (*University of Maryland*, USA); **Hsiang-Huang Wu** (*University of Maryland*, USA); **Shuvra Bhattacharyya** (*University of Maryland*, USA)

Session 7B: RF, IF, ADC

Regency D

Chair: **Mohammed Ismail**, *Ohio State University*, USA

08:30 "Antenna Design Strategy and Demonstration for Software-Defined Radio" (Best of R&D Track) **Taeyoung Yang** (*Virginia Tech*, USA); **William Davis** (*Virginia Tech*, USA); **Warren Stutzman** (*Virginia Tech*, USA); **S M Hasan** (*Virginia Tech*, USA); **Randall Nealy** (*Virginia Tech*, USA); **Carl B. Dietrich** (Virginia Tech, USA); *Jeffrey Reed* (*Virginia Tech*, USA)

08:50 "A High Performance RF Transceiver Implementation" **Neil Dodson** (*University of Notre Dame*, USA); **Glenn Bradford** (*University of Notre Dame*, USA); **J. Nicholas Laneman** (*University of Notre Dame*, USA)

09:10 "Bringing RF Tunability to Mobile Communications Markets" **Peter Bacon** (*Peregrine Semiconductor*, USA)

09:30 "Multi-Radio Coexistence and Collaboration on an SDR Platform" (Best of R&D Track) **Tommi Zetterman** (*Nokia*, Finland); **Antti Piipponen** (*Nokia*, Finland); **Kalle Raiskila** (*Nokia*, Finland); **Sverre Slotte** (*Nokia Research Center*, Finland)

09:50 "Wideband Transceivers for Software Radio: A Space Segment Survey" **Fabrizio Massaro** (*LuxSpace Sárl*, Luxemburg); **Jens P. Elsner** (*Karlsruhe Institute of Technology*, Germany); **Florio Dalla Vedova** (*LuxSpace Sárl*, Luxemburg); **Friedrich K. Jondral** (*Karlsruhe Institute of Technology*, Germany)

10:10 "Trends and Theoretical Limits to ADC Performance and Their Impact on SDR and CR Design" (Invited Presentation) **James Neel** (*Cognitive Radio Technologies, LLC*, USA)

Session 7C: Spectrum, Regulatory, and Standards

Regency E

Chair: **Zhongren Cao**, *University of California, San Diego*, USA

08:30 "State of the Art in ETSI SDR and CR related Standardization and Preparation of Commercialization" **Markus Mueck** (*Infineon Technologies*, Germany); **Kari Kalliojarvi** (*Nokia Research Center*, Finland); **Jens Gebert** (*Alcatel-Lucent*, Germany); **Gianmarco Baldini** (*Joint Research Centre - European Commission*, Italy); **Andrea Lorelli** (*ETSI*, France)

08:50 "Policy-Based Remote Spectrum Coordination" **Thaddeus Konicki** (*Lockheed Martin Advanced Technology Labortories*, USA); **Timothy Bieniosek** (*Lockheed Martin Advanced Technology Labortories*, USA); **Ritu Chadha** (*Telcordia*, USA); **Jason Chiang** (*Telcordia*, USA); **William Kline** (*Lockheed Martin Advanced Technology Laboratories*, USA); **Constantin Serban** (*Telcordia*, USA); **Harris Zebrowitz** (*Lockheed Martin Advanced Technology Laboratories*, USA)

09:10 "Power Fingerprinting in Unauthorized Software Execution Detection for SDR Regulatory Compliance" (Best of R&D Track) **Carlos Aguayo Gonzalez** (*Virginia Tech*, USA); Jeffrey Reed (*Virginia Tech*, USA)

09:30 "Euler" **Ottavio Picchi** (*University of Pisa*, Italy); **Taj Sturman** (*EADS Astrium Ltd*, United Kingdom); **Fabrizio Vergari** (*Selex - Communications*, Italy); **Timo Braysy** (*University of Oulu*, Finland); **Raúl Dopico López** (*Indra Sistemas S.A.*, Spain); **Gianmarco Baldini** (*Joint Research Centre*, European Union); **Marco Luise** (*University of Pisa*, Italy); **Emilio Bolzan** (*Selex - Communications*, Italy); **Julio Diez Ruiz** (*Indra Sistemas S.A.*, Spain)

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Friday, 3 December

08:30

Session 7D: Communications Signal Processing III

Regency F

Chair: **Joseph Gaeddert**, *Virginia Tech*, USA

08:30 "Software Implementation of Near-ML Soft-Output MIMO Detection" **Daniele Lo Iacono** (*STMicroelectronics*, Italy); Teo Cupaiuolo (*STMicroelectronics*, Italy)

08:50 "LDPC Decoding on the Sandbridge Sandblaster SDR Platform" (Best of R&D Track) **Murugappan Senthilvelan** (*University of Wisconsin - Madison*, USA); **Meng Yu** (*Sandbridge Technologies Inc.*, USA); **Daniel S Iancu** (*Optimum Semiconductor Technologies*, USA); **Mihai Sima** (*University of Victoria*, Canada); **Michael Schulte** (*University of Wisconsin-Madison*, USA)

09:10 "Reduced Complexity Soft MMSE MIMO Detector Architecture" **Kiarash Amiri** (*Rice University*, USA); **Chris Dick** (*Xilinx*, USA); **Raghu Rao** (*Xilinx*, USA); **Joseph R. Cavallaro** (*Rice University*, USA)

09:30 "Exploiting Cyclic Prefix Redundancy in OFDM to improve decoding of LDPC code" (Best of R&D Track) **Peter Farkas** (*Slovak University of Technology*, Slovakia); **Tomas Palenik** (*Slovak University of Technology*, Slovakia)

09:50 "Bandwidth Efficient Coded Modulation for SDR" **Saleh Faruque** (*Department of Electrical Engineering, University of North Dakota*, USA); **Mohit Dhawan** (*University of North Dakota*, USA)

Expert Lecture 7E: Modem Tutorial

Potomac III & IV

Chair: **fred harris**, *San Diego State University*

Our technological society has fielded modems for 50 years. The early modems moved 600 bits per second through shielded 4-kHz bandwidth wire-line channels. Modern modems move 108 bits over sever multipath corrupted 100 MHz bandwidth RF channels. In this 50 year time span the modem has undergone quite striking changes in architecture and hardware as it embraced wider bandwidth in pursuit of higher capacity. The modem permeates our economy, our commerce, our military, our entertainment media, and our research and development activity. The half day modem tutorial will emphasize the signal processing that is performed in the physical layer of the communication link. We will cover the three major processing tasks performed in the modem. These are first tier processing: that of filtering, spectral translating, and signal conversion, second tier processing: synchronization, the alignment of frequency and phase of carrier and symbol timing, and the third tier processing: the suppression of artifacts due to imperfect analog components in the signal conditioning and signal transport path between transmit and receive ports. Reference: fred harris, Wade Lowdermilk, "Software Defined Radio", Tuturial 22, IEEE Instrumentation and Measurement Magazine, February 2010, pp.23-32.

Tutorial 7F: ESSOR SDR Architecture – Motivation and Overview

Potomac V & VI

ESSOR is a major SDR program established under the umbrella of the European Defense Agency (EDA), sponsored by the governments of Finland, France, Italy, Poland, Spain and Sweden, and awarded by the Organisation Conjointe de Coopération en matière d'ARmement (OCCAR) to the dedicated joint venture Alliance for ESSOR (a4ESSOR S.A.S.) in charge of managing the industrial consortium composed of the following respective National Champions: Elektrobit, THALES Communications., SELEX Communications., RADMOR, INDRA Sistemas and Saab ABs.

One of the main goals of the ESSOR program is the development of the ESSOR Architecture, an Software Defined Radio (SDR) Architecture relying on the already published Joint Tactical Radio System (JTRS) Software Communications Architecture (SCA) and Application Programming Interfaces (APIs). The ESSOR Architecture is a complete and consistent Secure SDR Architecture addressing the European military radio-communications market, and fostering on Waveform portability amongst heterogeneous SDR Platforms.

Featuring speakers:

- **Fabio Casalino**, *Selex Communications*
- **Eric Nicollet**.*Thales Communications*
- **Rafael Aguado**. *Indra*

On behalf of all ESSOR Industries

Wednesday

A Unified Platform for Communication System Design and Prototyping: An LTE MIMO Demonstration

Ian C. Wong (*National Instruments*, USA); Yong Rao (*National Instruments*, USA); Takao Inoue (*National Instruments*, USA); Wes McCoy (*National Instruments*, USA); Ahsan Aziz (*Freescale Semiconductor*, USA)

A development platform that unifies software, hardware, and radio system design aspects for SDR remains elusive. The challenges SDR platforms face include the need for custom prototyping hardware, discrete RF designs, VHDL/Verilog RTL development, C/DSP assembly programming, and creating I/O interface drivers. Consequently, large engineering teams that have expertise across the many disciplines of radio design and implementation, from communication and algorithm experts to hardware, software, analog, and RF engineers are typically needed in order to meet the stringent time-to-market requirements of modern radio systems. From both a cost and time-to-market savings standpoint, it is desirable to engage the algorithm experts early in the development cycle. At the same time, it is beneficial for the implementation-oriented engineer to understand the overall system performance, which includes all the practical aspects of radio design, such as the impact of radio impairments, overall system architecture, and software-hardware interaction, prior to the development of custom hardware. The availability of development platforms that address these issues can bring significant cost and time-to-market savings, and are thus highly valuable for the wireless industry as a whole.

In this demonstration, we elaborate on the National Instruments hardware and software solution for SDR development. The generic hardware architecture consists of a general purpose processor, FPGA, and tightly-integrated I/O. These elements are interconnected via a high-speed standard bus with extensions for triggering and synchronization, all of which are programmed within a unified system design environment called LabVIEW. LabVIEW is a graphical system design language that brings together various models of computation, e.g. data-flow, textual math (i.e. .m files), state charts, and C-language, and is capable of targeting a variety of computational platforms including desktop/embedded processors, DSPs, and FPGAs, while at the same time integrating real-time performance and I/O seamlessly with the computational aspects. The power of this flexible software design language, together with a diverse suite of computation and I/O hardware, provide a scalable and flexible SDR platform that delivers on the promise of a unified platform for the entire SDR design flow.

In order to highlight the power of the National Instruments hardware and software platform for SDR, we demonstrate a prototype of a 3GPP-LTE Frequency Division Duplex (FDD) mode MIMO downlink and SC-FDMA uplink system that was developed entirely within LabVIEW. The prototype demonstrates a closed-loop 2x2 MIMO over-the-air link with adaptive modulation and coding (AMC) that supports all of the LTE bandwidths from 1.4 MHz to 20 MHz. The prototype includes the complete RF and baseband physical layer signal processing chain for both the base station and mobile station, each of which resides in an NI PXIe-1075 industrial form-factor PCI-express based chassis. Each chassis includes a PXIe-8130RT embedded multi-core CPU running a real-time operating system, which handles the link control, higher-layer protocol software, and communication with an optional host PC via TCP-IP. The core high-rate physical layer processing functions are implemented in an NI PXIe-5641R Intermediate Frequency (IF) Transceiver module, which is an NI LabVIEW targetable FPGA board with integrated 2-input, 2-output IF ports. In the case of the transmitter, after generating the baseband signals in the FPGA, it is digitally upconverted to IF on the PXIe-5641R, and subsequently modulated onto a radio frequency carrier using the NI PXI-5610 2.7 GHz RF upconverter. In the case of the receiver, the NI PXI-5600 2.7 GHz RF downconverter performs the modulation of the RF signal down to IF. This IF signal is then fed into the IF transceiver PXIe-5641R for receiver signal processing. The physical layer processing blocks are developed using LabVIEW for Windows, LabVIEW Realtime, and LabVIEW FPGA. The partitioning is determined based on the realtime rate requirements and also the bandwidth of the PXI-express bus. The low-rate blocks in the transmit signal chain, namely bit generation, constellation mapping, data and pilot subcarrier multiplexing, and precoding for closed-loop MIMO are all done in the embedded real-time controller. The high-rate blocks including the turbo encoding, OFDM symbol generation (which includes IFFT and Cyclic Prefix extension), and sample rate conversion are done in the FPGA. Similarly on the receiver chain, timing synchronization, FFT, CP removal, frequency offset correction, channel estimation, MIMO processing, and turbo decoding are all done partly in the FPGA and partly in the realtime controller. The final constellation, packet error rate, and spectrum displays, in addition to other non-real-time operations like hardware configuration are done in the host PC.

It is important to note that this working prototype was implemented entirely by communications and signal processing algorithm experts, rather than hardware or software experts, within a matter of months. This is a testament to the potential cost and development-time benefits of a unified hardware and software platform that truly provides a software-defined approach to rapid wireless design and prototyping.

LabVIEW Channel Emulator

Fanny Mlinarsky (*octoScope*, USA); Samuel MacMullan (*ORB Analytics*, USA)

Fox is a software based channel emulator that models a wireless channel with up to 4x4 MIMO paths. While currently supporting 802.11n channel models, Fox can be extended to incorporate other channel models, including LTE and a variety of military or proprietary models. Fox operates in the LabVIEW environment and works on MIMO streams of IQ samples. The demo will show operation on IQ streams stored in files and will include a presentation explaining the background and theory of wireless channel modeling. We will overview the industry standard channel models, including 802.11n, ITU (pedestrian and vehicular), LTE, LTE-Advanced, 802.11ac, 802.11ad channel models. We will explain and demonstrate the statistical nature of channel models.

Execution Time Monitoring and Real-Time Multi-Processing with the ALOE SDR Middleware

Ismael Gomez (*Polytechnical University of Catalonia*, Spain); Antoni Gelonch (*Polytechnic University of Catalonia*, Spain); Vuk Marojevic (*Polytechnic University of Catalonia*, Spain)

Monitoring waveform execution time in Software-Defined Radios is essential in modern multi-processor radios. The process of assigning computing resources to waveform components improves

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Technology Showcase Days and Hours: Wednesday 17:30 - 19:30 and Thursday 11:50-13:45 (see insert map for booth locations)

Wednesday

with the accuracy of waveform components resource demands. In shared-resource radio infrastructures, this feature is essential since it provides a mechanism for resource accounting while ensures that a client is unable to block another. Multi-processor platform must ensure, in addition, that data-flows from one processor to another do not violate end-to-end latency constraints. Moreover, modern iterative algorithms (LDPC, turbo-decoding, etc.) consume different resources as a function of the receiver EbNo or target QoS. Therefore, computing resource managers capable to measure resource consumption can potentially make a tighter adjustment of its decisions as a function of these environment variables (Cognitive Radio). The demo shows how the ALOE middleware is able to analyze computing resource consumption as well as ensure all waveform deadlines are met in a distributed multi-processor environment.

Multi-Ghz Platform for Software Defined Radio

Chen Chang (*BEEcube Inc.*, USA)

Developed out of the Berkeley Wireless Research Center (BWRC) at University of California at Berkeley, the BEE3's high-speed multiple FPGA based platform allows for flexible algorithm and feature set definitions to fit mission critical needs. The BEE3 excels as a true real-time development and deployment platform for:

* Software Defined Radio (SDR)
* Signal Intelligence
* Wireless (digital based RF) Algorithm Applications

As a result, the BEE3 has attracted leading industry companies worldwide such as Aerospace Corporation, L3 Communications, and Thales Group.

BEEcube's SDR Demonstration Our demonstration highlights BEE3 as an SDR prototyping platform - showing off our FPGA based continuous wideband vector signal generator, controlled by software in real-time via Wind River's VxWorks over Gigabit Ethernet, with carrier frequency tone sweeps ranging from 0 to 2GHz. BEE3's inherit I/Q 2Gsps DAC highlights BEE3's wideband capability. The BEE3 ADC expansion board simultaneously captured analog output with Data being displayed directly and integrated with Matlab(tm). BEE3's ADC can sample up to 3 GHz, offering a true direct RF sampling capability.

BEE3 Easy Algorithm Deployment

Coupled with high-speed I/O and infrastructure, the BEE3 system software allows algorithm designers without any RTL or implementation knowledge to easily program the target BEE3 system. BEEcube Platform Studio (BPS) is a system-level, hardware/software co-development environment on top of the MathWorks" Simulink® framework. BPS provides automatic generation of all platform specific hardware interfaces and corresponding software drivers. Months of engineering tasks to convert complex DSP algorithms to implementation can be achieved through BPS in a matter of days, all without requiring user knowledge of the low level FPGA implementation details, such as high speed I/O interfaces, timing closure, HW/SW interfaces, and IP integration issues.

BEE3 Hardware Meets All Your Changing Mission Critical Needs

* Combined with the BEEcube's 3rd generation Xilinx Virtex-5 FPGA based hardware platform, the BEE3, the integrated BEEcube solutions enables a wide range of high-performance real-time implementations in multiple military and defense applications, including signal intelligence, signal warfare, software defined radio, MIMO communications, radar applications, and many more.
* Advanced signal processing algorithm can be rapidly prototyped on the BEE3 system, running at hundreds or MHz clock rates, which directly interface to multi-GHz A/D and D/A converters. When it comes to deployment, the same design can be easily retargeted in the BEEcube Platform Studio (BPS) design environment to fit into various hardware platforms with different form factors, capabilities, and FPGA technologies.

Common Data Link Quad-band Relay

Benjamin Egg (*fred harris and Associates*, USA); fred harris (*San Diego State Univ*, USA)

The Common Data Link (CDL) system is an essential DoD asset that suffers significant performance and reliability losses due to multipath interference and fading, particularly in low Angle of Arrival (AoA) operating conditions. This work was undertaken to mitigate those losses via minimally-intrusive firmware updates of existing hardware, while ensuring continuous legacy compatibility. Emphasis is given to low AoA operations.

The Quad band Relay (QbR) architecture is a simple, yet powerful solution that utilizes existing hardware and additional CDL bandwidth to create link diversity. Utilizing an efficient frequency diversity architecture, link-loss due to multipath is significantly reduced. This is due to the fact the multipath losses are frequency dependent, and QbR's redundant transmissions have offset frequency centers transmitting encoded versions of the original legacy waveform.

Legacy systems communicate with QbR upgraded platforms seamlesslywithout hardware, software, or firmware modification. Furthermore, QbR upgraded systems receive the same transmission and are able to extract additional link gains via processing. An unmodified CDL system's default br45 (bit rate45 Mbps) filter bank rejects the redundancy of QbR, thus receiving a 100% legacy waveform. On the other hand, a QbR receiver's firmware selects the br274 filter path, allowing the legacy waveform and 3 diversity encoded waveforms to be digitized, demodulated, and combined into one final br45 data stream. Only the IF receiver filter bank selection changes, as far as the hardware is concerned. Upgrading the sea of current CDL hardware has been a key consideration in developing the QbR architecture, and the two enabling criteria which determine upgradability are: 1) The presence of a br274 filter path, and 2) sufficient processing power (FPGA size). The later requirement is likely satisfied if the system supports, or was originally designed to support the br274 waveform (regardless of br274 functionality).

Using MLM for Signaling: A Cognitive Radio Capability on the GNU Radio

Jakub Moskal (*Northeastern University*, USA); Shujun Li (*Northeastern University*, USA); Mieczyslaw Kokar (*Northeastern University*, USA)

The Modeling Language for Mobility Work Group is developing a language (MLM) to be used by Cognitive Radios to exchange control (signaling) information. In particular, radios can use MLM to exchange information about themselves (their "knobs" and "meters") in order to achieve interoperability. This demonstration will show an initial implementation of this functionality on the GNU radio toolkit and Universal Radio Software Peripheral (USRP).

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Wednesday

Sora -- High Performance Software Radio Platform Based on PC Architecture

Jiansong Zhang (*Microsoft Research Asia*, P.R. China); Kun Tan (*Microosft Research Asia*, P.R. China); Ji Fang (*Beijing Jiaotong University*, P.R. China); Yongguang Zhang (*Microsoft Research Asia*, P.R. China)

This demo shows Sora, a fully programmable software radio platform based on general-purpose processors. With Sora, developers can implement and experiment with high-speed wireless protocol stacks, e.g. IEEE 802.11a/b/g and LTE, on commodity PCs, using familiar programming environments with powerful tools on standard operating systems. In the demo, we first show a Sora-based demonstration radio system, called SoftWiFi. SoftWiFi is a full suite of 802.11a/b/g implementation that can seamlessly interoperate with commercial 802.11 NICs at all modulation rates, and achieves equivalent performance as commercial NICs at each modulation. Then, we show another application that performs spectrum analyzing based on Sora on a normal PC. We demonstrate that with proper software architecture and programming optimization, general purpose processors have sufficient processing power for many wireless processing tasks. We believe such processing power of GPPs will continue increasing with ever falling price driven by Moore's law and large market. Sora is now available for non-commercial use as Microsoft Software Radio Academic Kit.Our final goal is to make Sora a common research platform to the community to facilitate the experimental research in high-speed wide-band cognitive and wireless research.

OSSIE/GNU Radio Generic Component Demonstration

Duyun Chen (*University of Pennsylvania*, USA); Garrett Vanhoy (*University of Arizona*, USA); Marypat Beaufait (University of Michigan, USA); Carl B. Dietrich (*Virginia Tech*, USA)

A Generic Component (GC) was created to integrate OSSIE and GNU Radio (GR), two widely used open source development suites for Software Defined Radio (SDR). The GC is an OSSIE component which can encapsulate one or more GR blocks and provide the necessary data conversions to interface OSSIE I/O with the GR blocks. The GCs encapsulated GR blocks and the GR block properties can be reconfigured at runtime. The purpose of this demonstration is to show the functionality of the GC in addition to the distributed waveform capability of OSSIE applied to GR.

Thursday

High performance, small footprint NCO for communications applications

Frank Raffaeli (*RF Instrumentaion*, USA); Stephen Dark (*National Instruments*, USA)

SDR applications are becoming more demanding, increasing the need for both implementation efficiency and performance. An NCO (Numerically-Controlled Oscillator) is one of the fundamental building blocks for any frequency-agile Software-Defined Radio. This presentation reviews the detailed implementation of a high-performance NCO in a graphical programming language, LabView FPGA, and analyses the noise spectrum results, tuning speed, and FPGA footprint. Using a recursive algorithm, this NCO can achieve a close-in (100 Hz) phase noise of -120 dBc, a noise floor of -180 dBc, all without using any block memory.

In a live demo, attendees can get under the hood of a high-performance software-defined radio as we walk through the implementation using the NI Flex-RIO adapter module hardware and the high-performance NCO LabView FPGA firmware design.

Demonstration of LTE OFDM Transmitter / Receiver with channel model IP core on Xilinx FPGA

Amit Mane (*Innovative Integration*, USA)

The next generation 3GPP wireless standard long-term evolution (LTE) provides a leap in performance and a move to complete packet-based processing. In the physical (PHY) level of the LTE specification, specific challenges exist when dealing with higher data throughput rates, as well as the move to OFDM technology for data transmission.

Innovative Integration has developed, and is in the processing of continuing to develop several new IPcore solutions to meet the demands of this new specification. With such blocks, it is critical not only to verify them as stand- alone blocks- but also to validate them in real systems with real-world data and channel conditions.

The Transmitter in the IP core performs the function of converting the message bits into real I/Q data using the OFDM engine with windowing and filtering options. The Channel model in the IP core converts the I/Q data into real-world signals showing various effects such as multipath and fading. The receiver section performs the synchronization and the OFDM demodulation to recover the message bits.

Our demonstration consists of verification of the LTE OFDM transmitter/receiver core using Innovative Integration's X5-400M board. Successful operation of the LTE OFDM core will be demonstrated under various channel conditions for a variety of transmission bandwidths, cyclic prefix and modulation schemes.

Amit Mane, Amit Mane is a senior Digital Design Engineer at Innovative Integration Inc since May 2003. His expertise include DSP algorithm development on FPGA, high speed digital system design based on popular bus architectures such as PCI, PCIe and cPCie. Amit holds a bachelors degree in Instrumentation and a M.S.E.E. from Texas Tech University. Amit may be reached at amane@innovative-dsp.com | 1-805-578-4285

Signal Intelligence using LabVIEW FPGA and Peer-to-Peer Streaming

Stephen Dark (*National Instruments*, USA); Jerry Lopato (*National Instruments*, USA)

Signal intelligence requires the acquisition, movement, and processing of massive amounts of data. In order to achieve this kind of performance, typically FPGAs have been employed for performance reasons. However, while FPGAs have great computational power, they require an unfamiliar programming paradigm shift from the traditional sequential based processor model. This is in addition to the many FPGA programming pitfalls including safe resets, clock crossings, and reset crossings that often plague the inexperienced FPGA developer. LabVIEW FPGA is a graphical FPGA programming tool that allows the algorithm developer to more easily express their design at a higher level of abstraction thus removing them away from the many low level FPGA details and potential pitfalls. While still programming parallel algorithms,

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Thursday

LabVIEW FPGA provides a more intuitive graphical environment where parallelism is more easily understood and programmed. LabVIEW FPGA enables engineers at various levels of FPGA programming experience an integrated development environment where both the expected high level programmatic expressiveness of LabVIEW is available while still allowing FPGA experts to develop low level optimized IP. In addition, third party HDL IP can easily be integrated into this environment including the Xilinx CORE Generator IP included with LabVIEW FPGA. Coupled with LabVIEW, PXIe, RF Hardware, Flex-RIO, and LabVIEW Real-Time, LabVIEW FPGA provides an environment where a wide array of development, prototyping, and production signal intelligence systems are more easily achievable.

This signal intelligence example demonstrates the wide potential of National Instruments' hardware and software platforms for developing systems with demanding hardware specifications and custom FPGA processing. This demonstration will show the platform's ability to 1) acquire three highly synchronized RF wireless channels, 2) stream wide bandwidth RF signals between hardware modules, 3) calculate real-time power spectrums, 4) detect signals of interest, 5) record the detected signals of interest to disk, 6) geolocate the signal source, and 7) determine the signal's modulation standard. First, the signal will be acquired using three of National Instruments PXIe based VSAs. Next, using Peer-to-Peer streaming, data is transferred directly via DMA from the three VSAs to the FlexRIO for FPGA signal processing without the need for any host computer interaction. Then, the FlexRIO's Virtex 5 SX95T FPGA performs the various signal processing algorithms including DDC channelization, overlapped windowing and FFTs, signal detection, location triangulation, and blind modulation detection all programmed using LabVIEW FPGA. In addition, once a signal of interest is detected, the raw time-domain signal is logged to a RAID drive. Throughout this entire process, the host computer functions as the user interface that controls the FPGA based signal processing and displays various pieces of feedback.

A SystemC Radio-in-the-Loop Modeling for Cognitive Radio Equipments

Stephane Lecomte (*Technicolor*, France); Wassim Jouini (*Supélec*, France); Christophe Moy (*Supelec*, France); Pierre Leray (*IETR/Supelec Campus de Rennes*, France)

In the context of reconfigurable cognitive radio equipment it can be interesting to propose a high level modeling approach. The advantage is that the obtained model can be simulated in order to observe the impact of the cognitive cycle (including all three: sensing, decision making and reconfiguration) into the global operation of the system, far in advance of its effective implementation. According to the results of the simulation, it is then possible to modify the functional architecture or/and the hardware architecture in order to be compliant with the specifications of the system. The modeling part description is presented in the paper entitled "Multi-Level Modeling and Simulation of a Cognitive Radio Equipment" at the conference in the research and development papers track.

The proposed demonstration offers the validation and the illustration of a modeling approach for cognitive radio equipment design, through a SystemC simulation of a transmitter and a receiver connected via a real RF channel using USRP boards. This demonstration consequently shows the new concept of "radio-in-the-loop" modeling for cognitive radio.

The demonstrator is a wireless transceiver composed of two main parts: a transmitter (Tx) and a receiver (Rx). Each part is subdivided into three sub-parts which use different technologies. Both Tx and Rx are reconfigurable and have been designed with HDCRAM management architecture [1]. The cognitive scenario is the following: " A sensor at the receiver's side evaluates some quality metric (for example BER or SNR); " A simple decision making process based on thresholds decides if the modulation order is correct (neither too high, nor too low for the measured SNR); " A reconfiguration process is activated to change the constellation order accordingly. The main functions of the transmitter and the receiver are modeled in untimed SystemC. The cognitive cycle supervision is done through HDCRAM in SystemC also. These two SystemC sub-models are generated from a UML model developed with MOPCOM methodology [2]. USRP boxes are used to connect Rx to Tx through the radio channel. Thus it is necessary to connect the SystemC model with the USRP card. For that the GNU radio environment provides the adaptation means between the data from SystemC to URSP card. The GNU radio adapter is connected with SystemC model through a local TCP link emulated by a socket. On the other side of GNU Radio processing, this adapter is communicated with URSP card via a USB link. During the demonstration, the transmission starts at a high SNR, in a QPSK modulation scheme. The level of amplification at transmitter (Tx) is decreased and the receiver (Rx) automatically detects the level under which reception is no more good enough. Then it sends and activates a constellation change at Tx and reconfigures itself so that the transmission comes back at a good quality of service again. An interactive view of the HDCRAM manager elements activations is available to observe the progress of the reconfiguration.

References [1] L. GODARD, C. MOY, J. PALICOT, "An Executable Meta-Model of a Hierarchical and Distributed Architecture Management for the Design of Cognitive Radio Equipments", Annals of Telecommunications, Special issue on Cognitive Radio, vol. 64, pp.463-482, number 7-8, Aug. 2009. [2] S. LECOMTE, S. GUILLOUARD, C. MOY, P. LERAY and P. SOULARD, "A Co-design methodology based on model driven engineering for SDR equipments", SDR Forum, Washington, DC, USA, December 2009.

Low Cost Single Chip FPGA Based Software Defined Radio Platform

Joseph Enke (*Johns Hopkins University*, USA)

This demonstration provides a low cost generic VHDL based software defined radio platform implemented on a field programmable gate array. The platform reduces cost of a traditional software defined radio by using a truly single chip system-on-a-chip architecture implemented on a low cost Xilinx Spartan3A DSP FPGA. The single chip implements an analog to digital converter interface, digital down converter, demodulator, stereo digital to analog converter interface, and a soft core microprocessor for system control and debug. This single chip replaces analog and digital signal processors and microprocessors. The platform uses an undersampling technique to sample an intermediate frequency provided by the analog front end. This technique further reduces cost of the system by lowering the system sample rate and allowing the use of an ADC with a lower sample rate. It also allows the use of a low cost FPGA with a system architecture that utilizes extra clock cycles between samples to reuse FPGA DSP hardware blocks. The VHDL based architecture of the system allows for rapid

development, highly reconfigurable, and highly reusable digital signal processing hardware and software. This single chip architecture allows the Xilinx ISE Design Suite tool chain to be used for all simulation, development, debugging, and deployment of system hardware, firmware, and software.

The platform is demonstrated by digitizing, down converting, demodulating, and analog converting a frequency modulated signal from a simple dipole antennae connected to an RF front end. The analog output signal is played through a set of headphones and recognized as the local radio station that the platform software is tuned to. The system software can be stepped through while simultaneously viewing the signal at various stages of the DSP hardware via the JTAG interface.

The system is demonstrated using an Ettus Research TVRX daughterboard as an analog front end with a simple dipole antennae connected, a Nu Horizons Spartan3A DSP development board with a high speed analog to digital converter and stereo digital to analog converter, and a pair of speakers. The demonstrations system costs under $200 and the author proposes that a system can be realized for less than $100.

Wireless Distributed Computing

Sahana Raghunandan (*Virginia Tech*, USA); *Jeffrey Reed* (Virginia Tech, USA)

With increase in demand for improved performance of computing systems, distributed paradigms have become ubiquitous. Specifically, in the absence of wired infrastructure or untethered operation, wireless distributed computing (WDC) can prove to be very effective in the execution of distributed algorithms for remote sensing, position location and computer vision, to name a few. The demonstration of the prototype test bed aims to provide an insight into the feasibility analysis, design tradeoffs and capabilities of WDC, enhanced by cognition at each radio node. One of the primary goals is to provide a test environment to investigate resource allocation techniques for efficient distributed image processing in the presence of variable channel conditions.

GNU Radio software distribution has been used as a baseline for development with the USRP hardware platform. The block diagram below gives an overview of the functional workflow of the system.

FPGA-based Multi-Element Antenna Beamforming System

Rodger Hosking (Pentek, USA)

FPGAs are handling an increasing number of the intensive real-time signal processing tasks for communications and signal intelligence system. This demonstration system features an array of eight antennas receiving a signal from a portable transmitter source. Each antenna signal is amplified, translated to IF, and then digitized by an A/D converter. Each digitized IF channel is down converted to baseband and then adjusted with beamforming phase and gain coefficients. Finally, all eight channels are summed together.

The A/D conversion, down conversion, phase and amplitude processing and summation operations are all performed on FPGA-based software radio modules in a highly scalable architecture to support any number of antennas.

The resulting system effectively steers the antenna array to a specific angle of receptivity to support applications including direction finding, diversity receivers and cell sectoring for mobile telecom base stations.

The operational demo system provides a live display of detection of the angle of arrival of the portable transmitter signal as it moves in front of the antenna array.

Hyper-processed FIR Filters

Benjamin Egg (*fred harris and Associates*, USA); fred harris (*San Diego State Univ*, USA); Chris Dick (*Xilinx*, USA)

Increasing data rates and spectrally adaptive modulation techniques continue to drive analog-to-digital and digital-to-analog converter frequencies higher. A previously rare data processing phenomenon, generally isolated to surveillance and electronic warfare engineering teams, is becoming a general challenge Converter-to-Core Clock Cycle Inversion (C4I). As conversion rates climbed closer to the C4I boundary, the processing challenges were efficiently managed by distributing multiply and accumulate (MAC) functions over increasingly parallel paths. As the data conversion rate approaches the processing clock frequency, a linear filter's processing necessarily becomes more and more parallel, until the C4I boundary is reached, at which point the designer must choose between reducing bandwidth or extending their 2-dimensional (parallel) filters to a third dimensionhyper processed filter architectures.

When data is not separable into multiple channels, nor can the bandwidth or data rate be reduced, hyper-processed filters manage the signal processing by re-arranging standard FIR filters into "doubly parallel" filter structures, or 3 dimensional filters. This class of filter efficiently operates without reducing bandwidth or limiting throughput. In addition, timing constraints can be relaxed significantly, substantially increasing designer productivity. The price is paid in additional silicon to support the growing cubic architecture; however, this is a desirable trade off as silicon prices drop according to Moore's Law.

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Agilent Technologies Inc. (NYSE: A) is the world's premier measurement company and a technology leader in communications, electronics, life sciences and chemical analysis. The company's 20,000 employees serve customers in more than 110 countries. Agilent had net revenues of $5.8 billion in fiscal 2008.

BEEcube provides High-Speed multiple FPGA prototyping and development platforms. With over 150 BEE systems purchased world-wide, BEE3 technology targets: " High-end Signal Processing applications " Computation/Algorithm prototyping BEE3: - Direct DAC/ADC interfaces, - Symmetrical Honeycomb" architecture - High-speed Gigabit Sting I/O", - Monitoring/Control with Nectar OS ", - Industry's largest Trace memory - 64GB. BEEcube Platform Studio" (BPS), a hardware/software co-development environment on top of MathWorks Simulink" framework, along with IP-Stitcher" allows Easy Algorithm deployment without any RTL knowledge.

For over 50 years, **CRC** has been providing technical expertise to both the Government of Canada and Industry in satellite, terrestrial, wireless, and optical communications. CRC is recognized as a world leader in software development for SDR technology. Maker of the JTRS certified SCA reference implementation (SCARI), CRC also offers the most comprehensive integrated development environment for the SCA. CRC has been intimately involved in driving the evolution of the SCA and draws from its long experience to offer consulting services and training. CRC's team is constantly pushing the limits to improve performance, collaborating with best-in-class partners to support the major RTOS, ORBS, processors, boards and systms. Visit our booth to see a demonstration of our latest Core Framework and SCA Development Tools for Eclipse.

Coherent Logix is the world leader of the lowest power, high performance, C-programmable processors for the embedded systems market. Coherent Logix's comprehensive solutions portfolio includes processors, integrated system development tools, optimized libraries, system reference designs, and a customizable system development platform to reduce development complexity and time-to-market. These solutions are designed to support a wide variety of industries, including automotive, broadcast, computer, consumer, industrial, medical, military, test and measurement, wireless, and wireline.

D-TA Systems Inc. simplify high-end Sensor Processing System development for Radio, Wireless, Radar, Signal Intelligence, and RF Test. Leveraging the leading edge technologies and many decades of experience, D-TA Systems has developed a complete slate of 10 Gigabit Sensor Processing and Recording solutions that drastically reduce deployment time and cost. Whatever your application Radio, Radar, Basestation, MIMO, Cognitive Radio, SIGINT - we have you covered from RF to Baseband to Multi-Core Software Processing. Let's get started!

DataSoft provides HW & SW products and design services for SDRs and Cognitive Radios. Our products include RF Transceivers, Tunable RF Filters, SCA-Compliant Waveform Development kits, Radio Network Test and Analysis Tools, SDR Tool Suite for SCA-compliant waveform development and analysis, Intelligent Agent SW for end-to-end performance monitoring; and middleware for power management. More information can be found at www.datasoft.com.

DRS Defense Solutions LLC provides advanced products and services in the areas of intelligence, communications, avionics, sensor technologies, control systems, security, cyber warfare, sonar, training systems, satellite communications and unmanned technologies. Headquartered in Bethesda, MD, the company employs more than 3000 people around the globe.

EB creates advanced technology and turns it into enriching end-user experiences. EB is specialized in demanding embedded software and hardware solutions for wireless and automotive industries. EB's Wireless Communications Tools is a global technology leader in test tools for measuring, modeling and emulating radio channel environments for commercial, military, aerospace and satellite radio applications.

Epiq Solutions designs and builds state-of-the-art low-power reconfigurable radio systems for mission-critical applications. We have extensive experience developing high performance hardware and signal processing solutions for a wide variety of commercial and government customers. Our expertise spans multiple disciplines, including hardware (RF, analog, FPGA, and digital design), software (DSP, embedded, and PC), mechanical, and system engineering. Epiq Solutions specializes in developing physical and protocol layer processing solutions in both FPGA fabric and software. This includes the detection, classification, and geo-location of radio emitters, as well as real-time processing and decoding of Layers 1, 2, and 3 for numerous wireless radio standards (including 2G/3G/4G cellular). The Epiq Solutions Bitshark family of broadband receivers includes the recently released FMC-1RX, which covers 300 MHz to 4 GHz and can be connected to a variety of commercially available FPGA boards that support the VITA-57 FMC interface. The FMC-1RX dramatically lowers the barrier to entry for complex SDR application development in terms of both cost and capability. Custom spins of Bitshark boards can be rapidly developed to meet specific customer requirements, such as transmit capability, MIMO processing, or stand-alone operation. We pride ourselves on developing practical, elegant radio solutions with demanding size and power constraints, and do it on time and within budget. For more information, please visit http//www.epiq-solutions.com.

Etherstack is a wireless communications software company, and a leading independent waveform specialist. The company has been developing waveforms for radio manufacturers and defence clients internationally for over ten years - since the outset of commercial Software Defined Radio (SDR) - and pioneered many unique techniques and tools key to successful SDR waveform development. Etherstack's engineers combine waveform design best-practice with a detailed knowledge of communications standards such as APCO P25, TETRA, DMR, MPT1327, UMTS, WiMAX, LTE and military specifications. They also specialise in multi-protocol IP core networks, which can be used with waveforms for completely flexible wide-area, field-deployable communications.

Ettus Research specializes in low cost, high quality software defined radio (SDR) systems. Universal Software Radio Peripheral (USRP) systems all over the world enable users to address a broad range of research, academic, industrial, and defense applications. The USRP platform is designed to address applications that require RF modulations in frequencies up to 6GHz with wide bandwidths and MIMO setups. A few example application areas include white spaces, mobile phones, public safety radio, land mobiles, broadcast TV, FM radio, satellite navigation, and amateur radio bands.

Green Hills Software, Inc. is the largest independent vendor of embedded development solutions. In 2008, the Green Hills INTEGRITY-178B RTOS was the first and only operating system to be certified by the NSA to EAL6+ High Robustness, the highest level of security ever achieved for any software product. Based on the royalty-free INTEGRITY RTOS, Green Hills Platform for Software Defined Radio delivers a complete, standards-based reference platform for developing and deploying SDR systems ranging from the armed forces Joint Tactical Radio Systems (JTRS) to public safety radios as well as commercial small form-factor reconfigurable radios. Our Platform for SDR includes multiple SCA OE solutions that are compliant with the latest POSIX and SCA standards. The Platform for SDR also provides integrated, host-based tools for every aspect of development, debugging, optimization, and deployment as well as a variety of integrated hardware platforms. Founded in 1982, Green Hills Software is headquartered in Santa Barbara, CA with European headquarters in the United Kingdom.

Harris Corporation is an international communications and information technology company serving government and commercial markets in

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more than 150 countries. Headquartered in Melbourne, Florida, the company has approximately $5 billion of annual revenue and more than 16,000 employees — including nearly 7,000 engineers and scientists. Harris is dedicated to developing best-in-class assured communications® products, systems, and services.

Innovative Integration is a leader in signal processing and data acquisition hardware and software. Our products combine DSPs and FPGAs with high performance analog, ready for integration into demanding real-time applications such as wireless, medical, and military. Innovative Integration offers a complete solutions for software-defined radio (SDR) applications by integrating IP for software defined radio (SDR) with Innovative's high performance X5 family of digitizers and powerful application development tools for FPGA development.

Lyric Semiconductor is a fabless semiconductor company founded in 2006 by MIT Ph.D. Ben Vigoda and 25-plus year semiconductor veteran David Reynolds. Lyric s probability processing technology is a rethinking of computers from the ground up. Lyric enables order-of-magnitude performance wins for some of the most interesting applications of today and tomorrow.

MathWorks products are used throughout the automotive, aerospace, communications, electronics, and industrial automation industries as fundamental tools for research and development. They are also used for modeling and simulation in increasingly technical fields, such as financial services and computational biology. MathWorks software enables the design and development of a wide range of advanced products, including automotive systems, aerospace flight control and avionics, telecommunications and other electronics equipment, industrial machinery, and medical devices. More than 5000 colleges and universities around the world use MathWorks solutions for teaching and research in a broad range of technical disciplines. MATLAB®, the language of technical computing, is a programming environment for algorithm development, data analysis, visualization, and numeric computation. Simulink®is a graphical environment for simulation and Model-Based Design of multidomain dynamic and embedded systems. The company produces nearly 100 additional products for specialized tasks such as data analysis and image processing.

MDE Systems Inc. specializes in Software Defined Radio infrastructure, Model Driven Engineering, Network Management Solutions and Customer Software development for distributed real-time and embedded systems.

National Instruments delivers fast, flexible, and accurate RF hardware powered by LabVIEW software to meet the evolving demands of the wireless industry and see the engineering process through from design to validation to production. Virtual instrumentation from NI helps engineers keep pace with the constantly growing number of standards by delivering tools for signal generation, analysis, visualization, and processing of standard and custom digital and analog modulation formats. Tailored software for standards ranging from WLAN and GPS to WiMAX deliver powerful and cost-reducing wireless test systems that engineers have come to rely on.

Objective Interface Systems provides real-time connectivity software development tools to meet the high-performance needs for worldwide telecommunications, data communications, industrial automation, consumer electronics, military, and aerospace markets. Objective Interface offers advanced communications infrastructures with ORBexpress®RT, ORBexpress DSP, ORBexpress FPGA and PCSexpress™. ORBexpress, the middleware foundation for the industry's first certified JTRS software-defined radio, is used successfully in virtually every major SDR program worldwide. PCSexpress is the industry's first high-assurance secure communications middleware for software-defined radio.

Pentek offers powerful VME, VXS, PMC, XMC, PCI and cPCI commercial and rugged board and system solutions. Pentek's data acquisition, software radio and digital signal processing products utilize TI's C6000 DSPs, Motorola's G4 PowerPC and Xilinx FPGAs. Pentek's I/O includes A/D's, D/A's, Digital Receivers and more. Pentek equips products with high-speed interfaces including Serial RapidIO and Fibre Channel and offers strong FPGA, I/O and DSP software support.

PrismTech is an acknowledged leader in Software Defined Radio infrastructure solutions. Our Spectra product suite for SDR/SCA developers includes: Spectra CX - a model-driven development tool that greatly simplifies, accelerates, and validates the SCA development process; Spectra OE - a high-performance, low-overhead, core framework and middleware implementation that runs on any mix of GPP, DSP, and FPGA processor technologies.

RFMD® is a global leader in the design and manufacture of high-performance RF systems and solutions. RFMD's industry-leading portfolio includes RF products for Point-to-Point Microwave Radio, WiFi, WiMAX, SmartEnergy/AMI, ZigBee®, Wireless Infrastructure, Military and Space, Broadband Transmission and General Purpose RF product markets.

Rohde & Schwarz is an independent group of companies specializing in electronics. It is a leading supplier of solutions in the fields of test and measurement, broadcasting, radio monitoring and radiolocation, as well as secure communications. Established more than 75 years ago, Rohde & Schwarz has a global presence and a dedicated service network in over 70 countries. It has about 7,400 employees and achieved net revenue of ¬ 1.2 billion (US$ 1.7 billion) in fiscal year 2008/2009 (July 2008 to June 2009). Company headquarters are in Munich, Germany.

Shared Spectrum Company (SSC) was founded in 2000 to develop technology that dramatically increases the efficient use of RF spectrum resources. During that same year, SSC became the first company to file comments at the Federal Communications Commission (FCC) proposing the shared use of white spaces in the television band for broadband Internet access. Over the past 10 years, SSC has become a leading expert and innovator in the development of cognitive radio technologies.

Spectrum Signal Processing, part of Vecima Networks Inc., is a leading provider of wireless solutions for the world's top defense, government, and communications firms. Spectrum delivers compelling time-to-market and performance advantages with integrated, application-ready products and unparalleled support, training, and product life cycle management services. Spectrum's software-reconfigurable products are optimized for military and satellite communications, signals intelligence, surveillance, electronic warfare, and video content distribution.

Tubitak Uekae The Scientific and Technological Research Council of Turkey (TÜBİTAK) is the leading agency for management, funding and conduct of research in Turkey. It was established in 1963 with a mission to advance science and technology, conduct research and support Turkish researchers. The Council is an autonomous institution and is governed by a Scientific Board whose members are selected from prominent scholars from universities, industry and research institutions. TÜBİTAK is responsible for promoting, developing, organizing, conducting and coordinating research and development in line with national targets and priorities.

xG Technology has developed xMax, the world's first carrier-class cognitive radio network solution that has been optimized to operate in unlicensed spectrum. The network includes a complete ecosystem of base stations, mobile switching centers, handsets and network management tools. xMax incorporates xG's patented technologies to deliver the first fully mobile VoIP network that can offer an end-to-end IP infrastructure, excellent quality of service and low latency.

Xilinx is the world's leading provider of programmable logic solutions to the wireless infrastructure market, provides highly flexible solutions for high performance applications, facilitating rapid and low risk product evolution strategies, whilst reducing time-to-market and cost. As standards rapidly evolve, programmable logic is now widely considered a strategic technology that delivers a powerful, flexible, cost-effective and scalable processing platform for evolving portfolios.