Building a 128x128 Coherent Massive MIMO Testbed: Architecture, Challenges and Real-time Implementation

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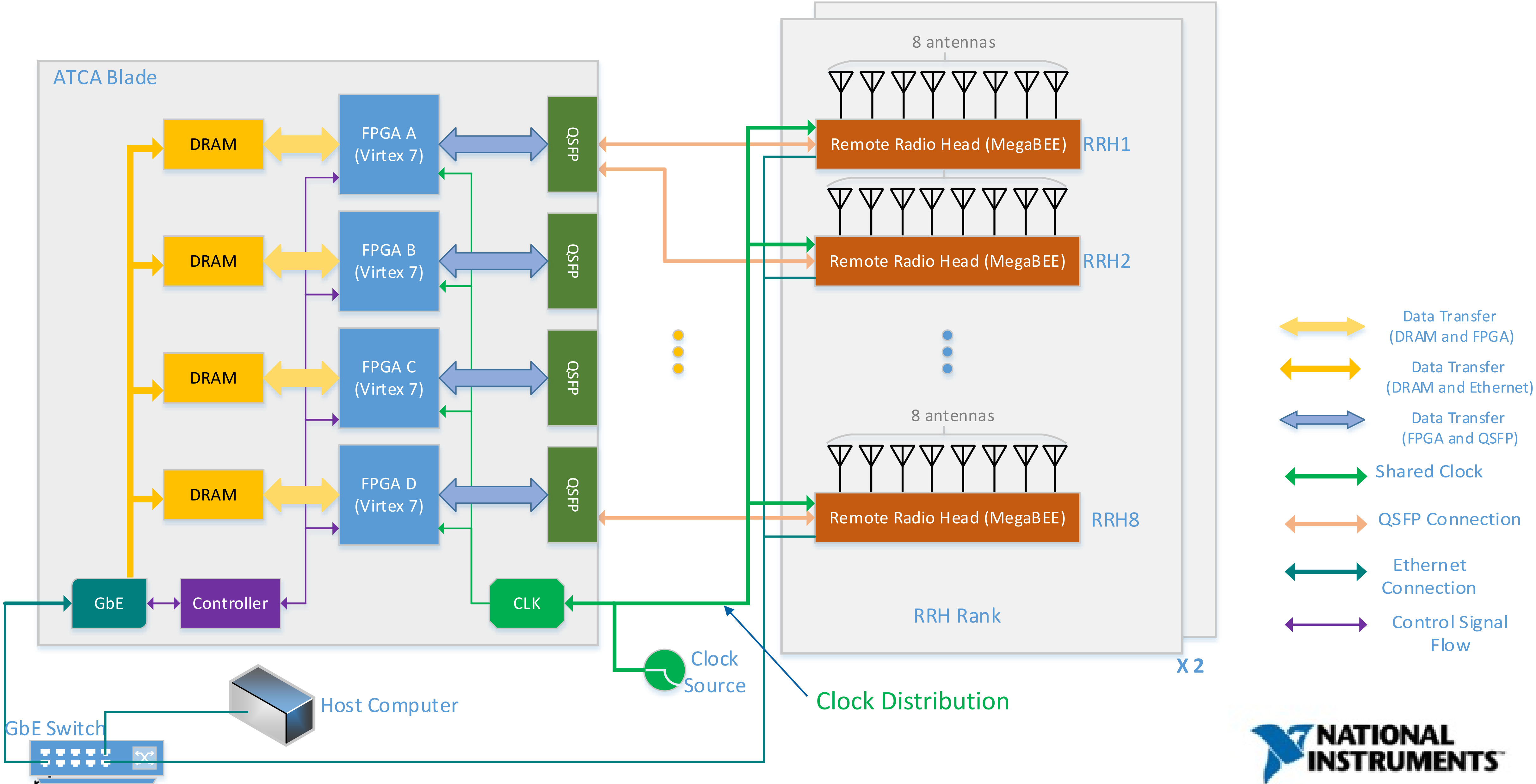
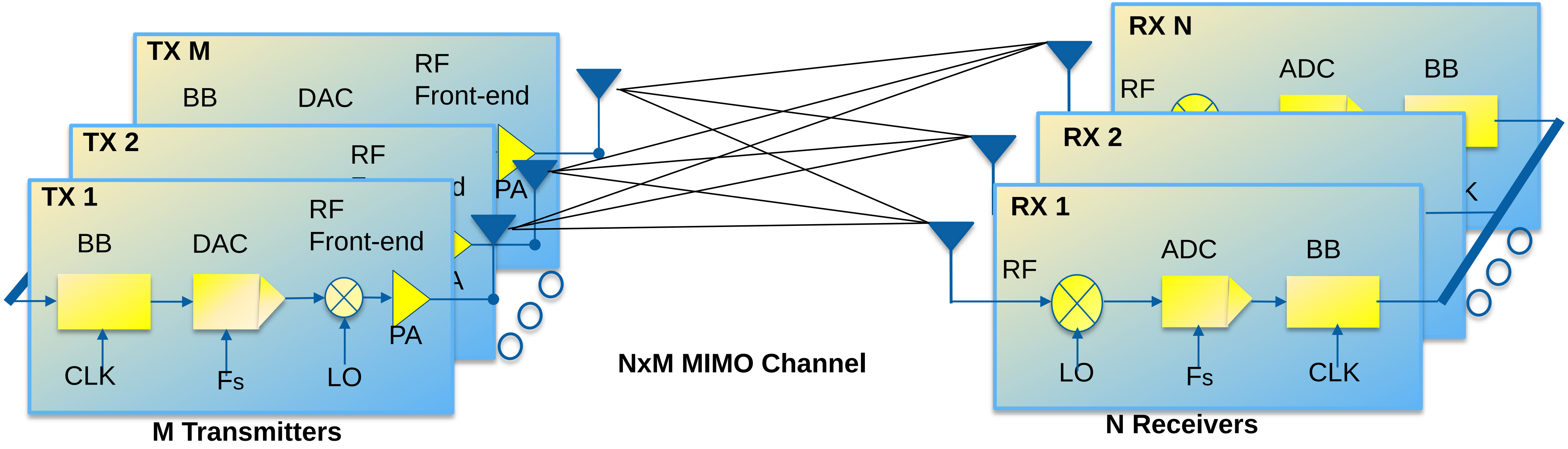
Agenda

- Architecture of 128x128 phase-coherent MIMO testbed
- Overview of phase-coherence and synchronization techniques
- Real-time implementation of phase-coherent massive MIMO testbed
- Testing and validation of phase-coherence and synchronization

Architecture of 128x128 Phase-coherent MIMO Testbed



Challenges in Prototyping Large-Scale MIMO Systems



Challenges at hardware level (impairments and distortions):

- Nonlinearities amplifier
- I/Q-imbalance
- Phase noise
- Clock/timing symbol errors (clock jitter, random fluctuation etc.)
- Quantization errors

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Overview of Phase-coherence and Synchronization Techniques

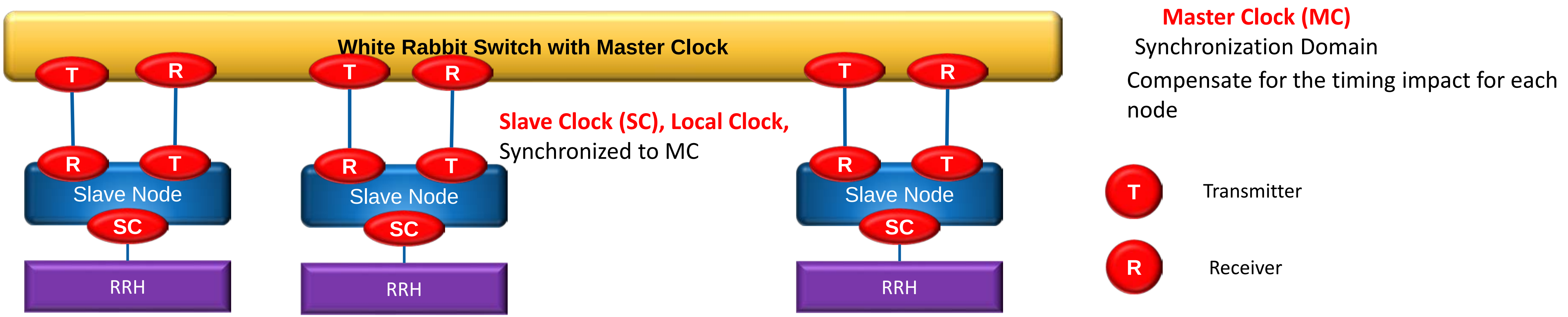
Synchronization mechanisms in digital receivers:

- **Clock/Symbol timing recovery**
  Adjusting directly the sampling clock.

- **Carrier recovery**
  Coarse frequency adjustment; Fine frequency adjustment and phase recovery.

- **Frame synchronization (data-aided)**
  Training signals, preambles, pilot frequencies, etc.

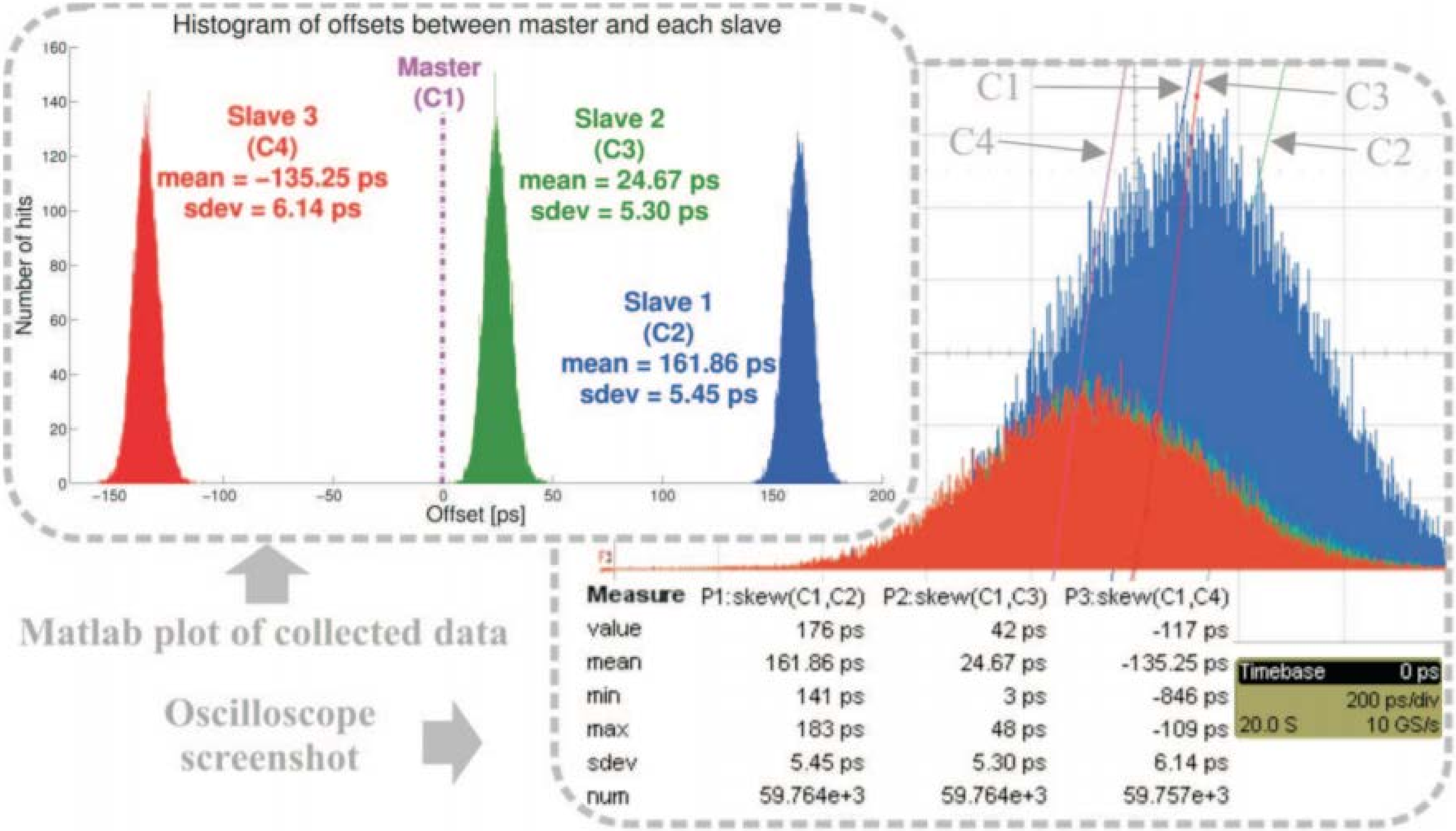
High-Precision Clock Distribution Using IEEE 1588v2



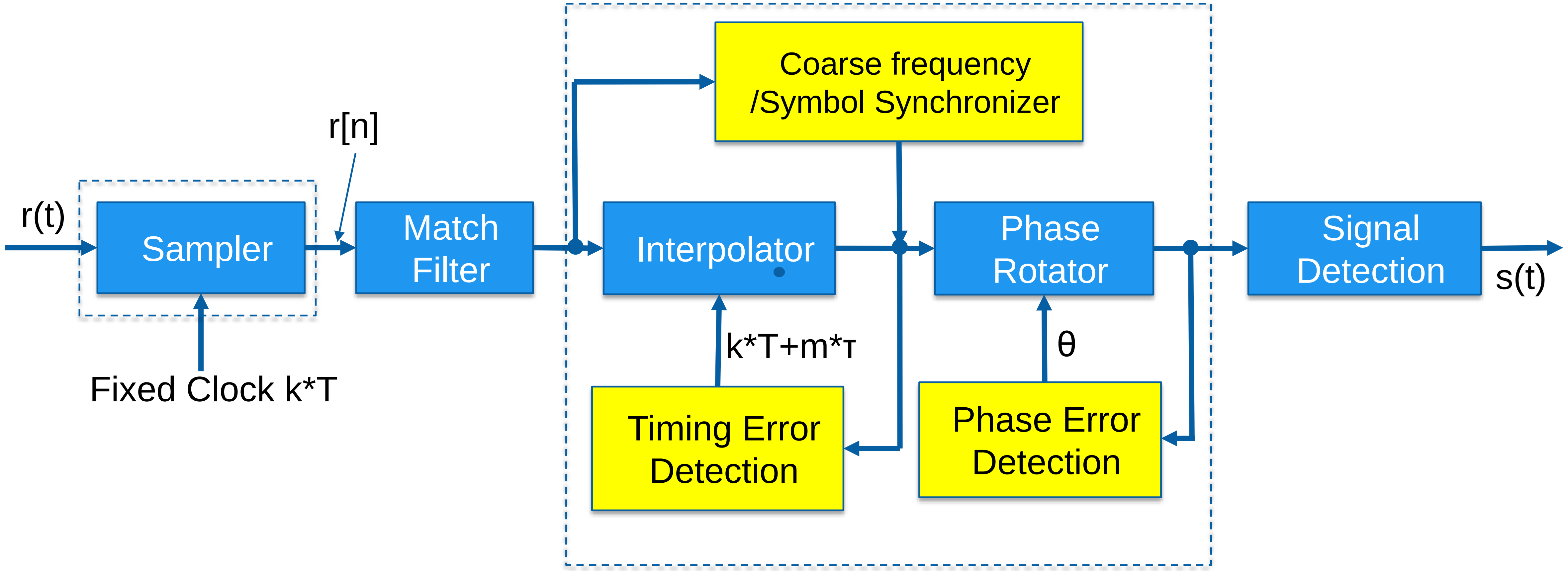
- Synchronization with **sub-ns** accuracy and **ps** precision
- Combination of
  - Precision Time Protocol (**PTP**) synchronization
  - Synchronous Ethernet (**SyncE**) syntonization
  - Digital Dual-Mixer Time Difference (**DDMTD**) phase detection

IEEE 1588 v2, also known as Precision Time Protocol (PTP), or White Rabbit (WR), provides accurate and robust synchronization for distrubuted Remote Radio Heads (RRHs) in massive MIMO systems.

Typical WR Performance Numbers

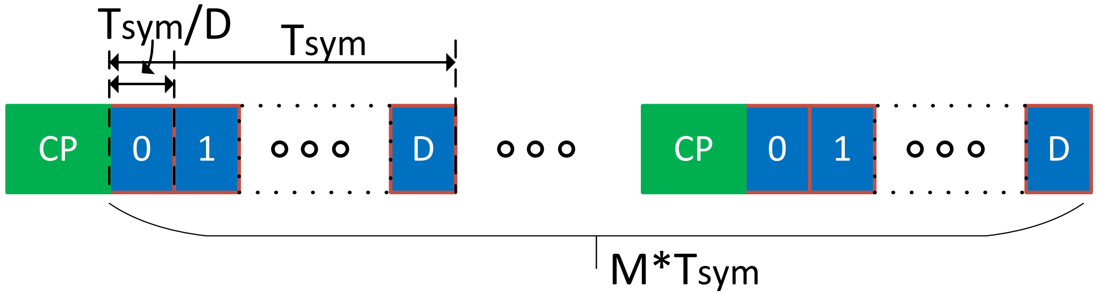


All-Digital Timing and Carrier Recovery



Timing Error Estimation

Frame structure of test signal vector for joint estimation of timing, carrier frequency offset (CFO) and phase errors



M=4
D=4

CP Cyclic Prefix (CP)

OFDM OFDM Symbols

$$x[n+\delta] \overset{\mathrm{DTFT}}{\longleftrightarrow} X[k]e^{2\pi k\delta/N}, \ \delta \text{ is the timing error.}$$

Timing Error Estimation

$$\boxed{\hat{\delta} = arg\max_{\delta} \frac{|y_l[n+i+\frac{N}{2}\cdot m]y_l^*[n+i+\frac{N}{D}+\frac{N}{2}m]|^2}{(\sum_{m=0}^{M-1}\sum_{i=\delta}^{N/D-1+\delta}|y_l[n+i+\frac{N}{D}+\frac{N}{2}\cdot m]|^2)^2}}$$

$$l = \{0, 1, \cdots, D-1\}$$

CFO and Phase Offset Estimation

Overall CFO Estimation

$$\boxed{\hat{\epsilon} = \hat{\epsilon}_I + \hat{\epsilon}_f}$$

Average Phase Offset Estimation

$$\boxed{\text{Phase Offset} \approx \frac{1}{N} \sum_{N-1}^{n=0} x[n] e^{2\pi n \hat{\epsilon}/N}}$$

$$\hat{\epsilon}_0 = \frac{1}{2\pi M} \sum_{m=0}^{M-1} \{tan^{-1}\{\frac{\sum_{k=0}^{N-1} I_m[Y_m^*[k]Y_{m+1}[k]]}{\sum_{k=0}^{N-1} R_e[Y_m^*[k]Y_{m+1}[k]]}\}\}$$

Initial CFO Estimation

$$x[n]e^{2\pi n \epsilon/N} \overset{\text{DTFT}}{\longleftrightarrow} X[k-\epsilon], \; \epsilon = \frac{f_{offset}}{\Delta_f}$$

where ϵ is the CFO.

$$\hat{\epsilon}_I = \frac{1}{2\pi T_{sym}} \max_{\hat{\epsilon}_0} \left\{ \left| \sum_{j=0}^{\frac{N}{D}-1} Y_{m+D}[j-\hat{\epsilon}_0] Y_m^*[j-\hat{\epsilon}_0] X_{m+D}[j] X_m^*[j] \right| \right\}$$

Integer CFO Estimation

$$\hat{\epsilon}_f = \frac{1}{2\pi T_{sym} DM} arg \left\{ \sum_{m=0}^{M-1} \sum_{j=0}^{\frac{N}{D}-1} Y_{m+D}[j-\hat{\epsilon}_I] Y_m^*[j-\hat{\epsilon}_I] X_{m+D}[j] X_m^*[j] \right\}$$

Fractional CFO Estimation

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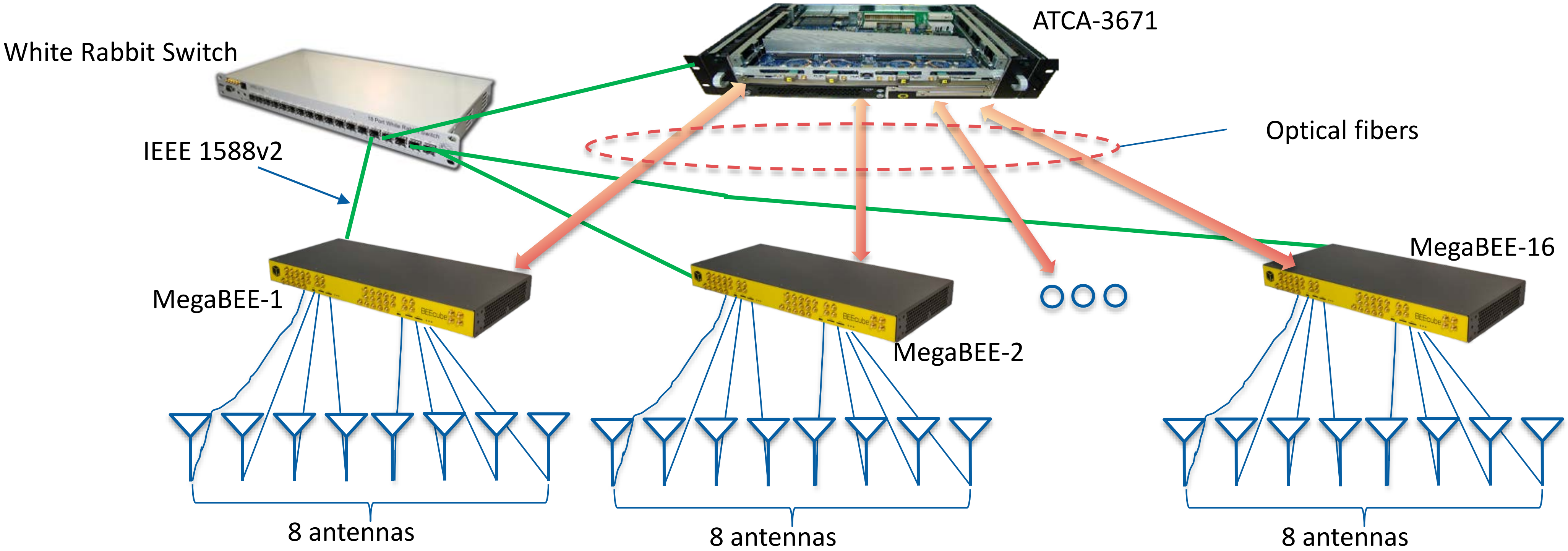
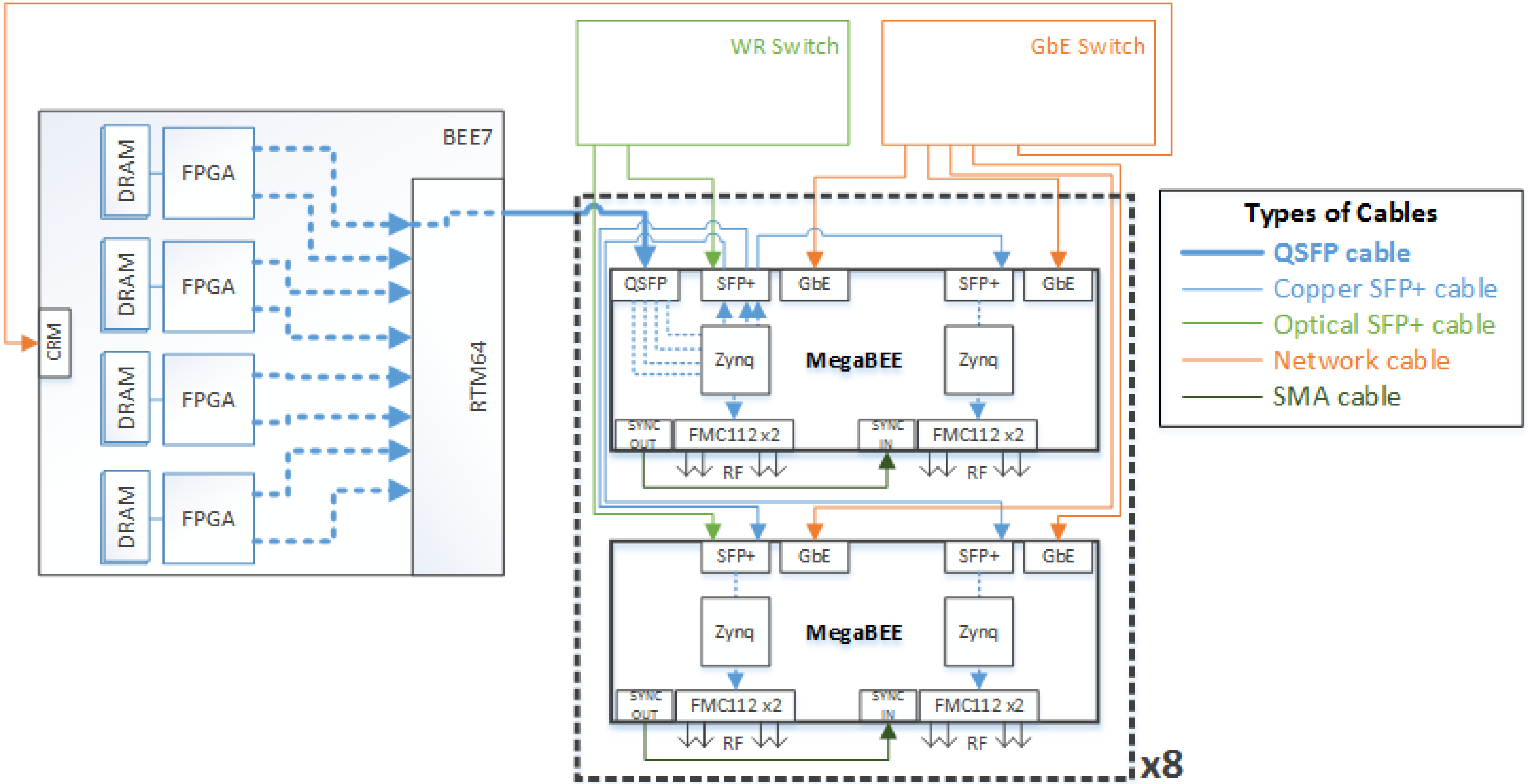
Prototyping 128-Channel Distributed Massive MIMO Testbed



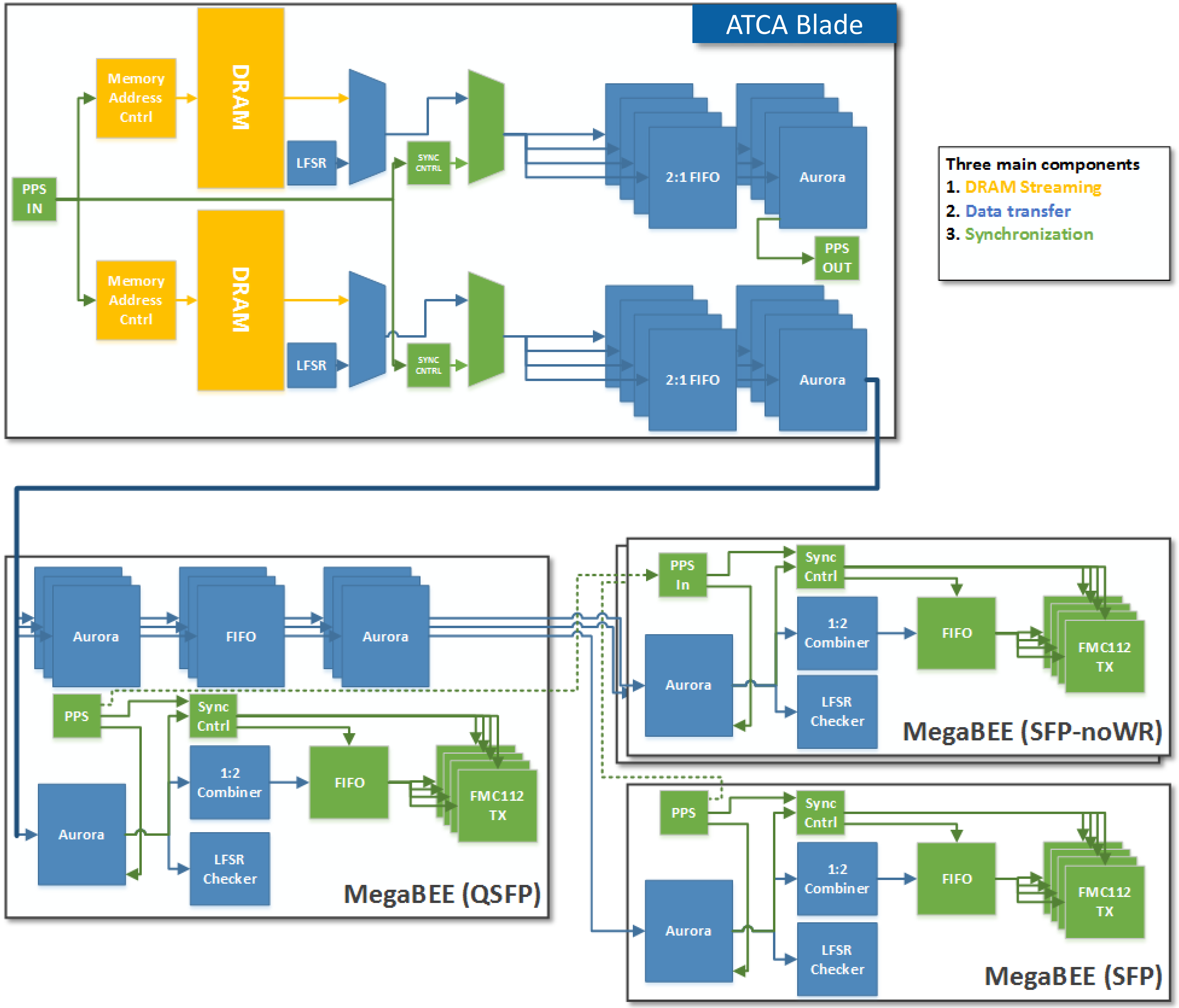
Configurations of 128-Channel Distributed Massive MIMO Testbed:

- 16 MegaBEE units (each has 8 RF ports)
- ATCA-3671 blade streams 640 Gbps throughput data from Rear Transfer Modules (RTMs) up to 16 MegaBEE units.
- Sub-nanosecond synchronization among multiple MegaBEEs

High Level Diagram of Distributed and Phase-coherent Massive MIMO



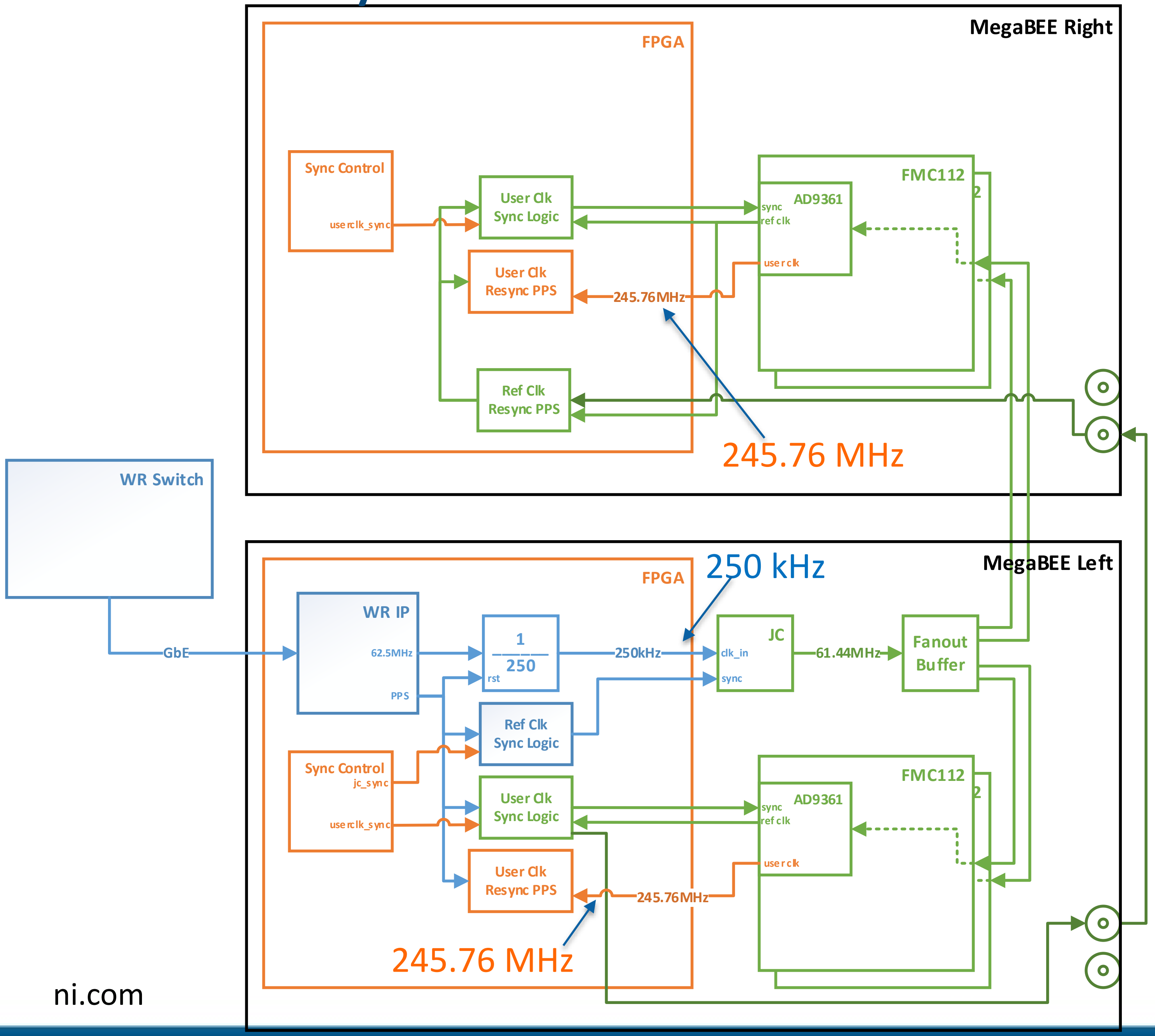
Block Diagram of System Design



Three main components:

1. DRAM Streaming
2. Data Transfer
3. Synchronization

Clock Synchronization in Remote Radio Head Units

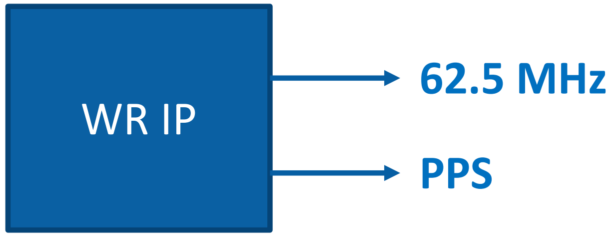


3 Clock Domains

WR Clock Domain
Ref Clock Domain
User Clock Domain

Three Clock Domains:

1. WR Clock Domain
2. REF Clock Domain
3. User Clock Domain



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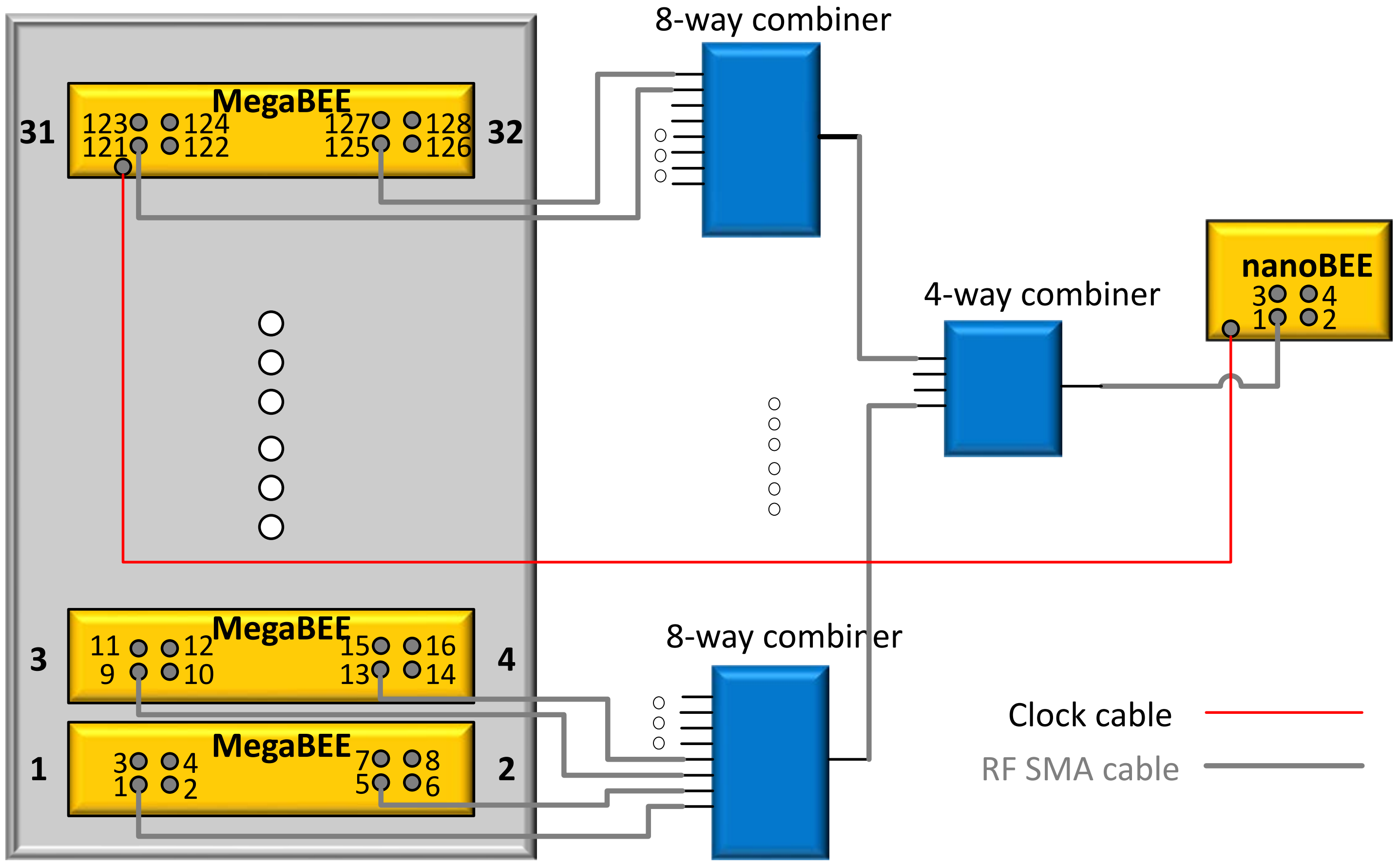
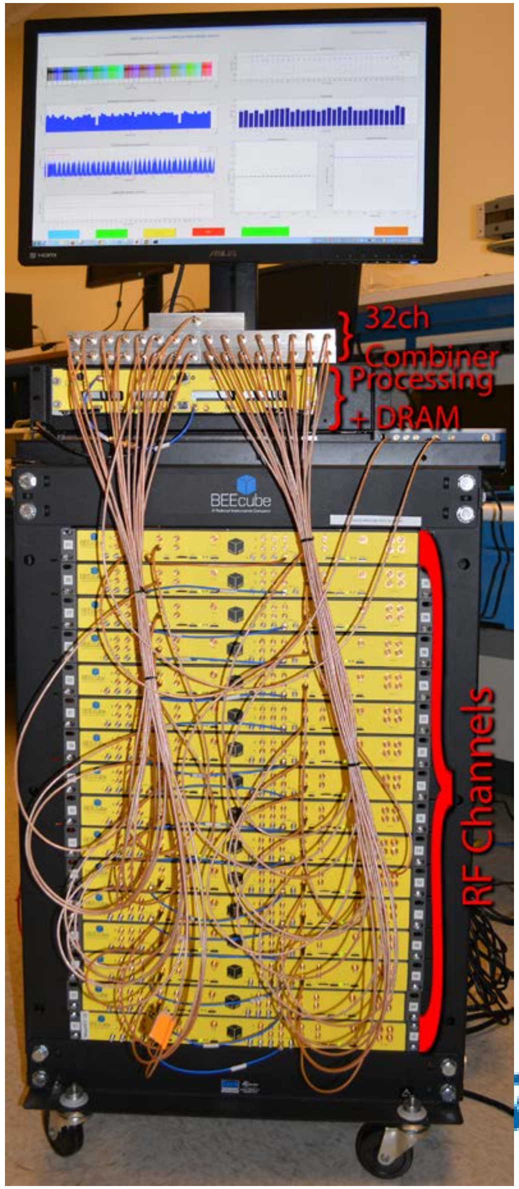
Testing Environments Setup



MegaBEE RRH Rack

Block diagram of testing setup for 32 RF channels



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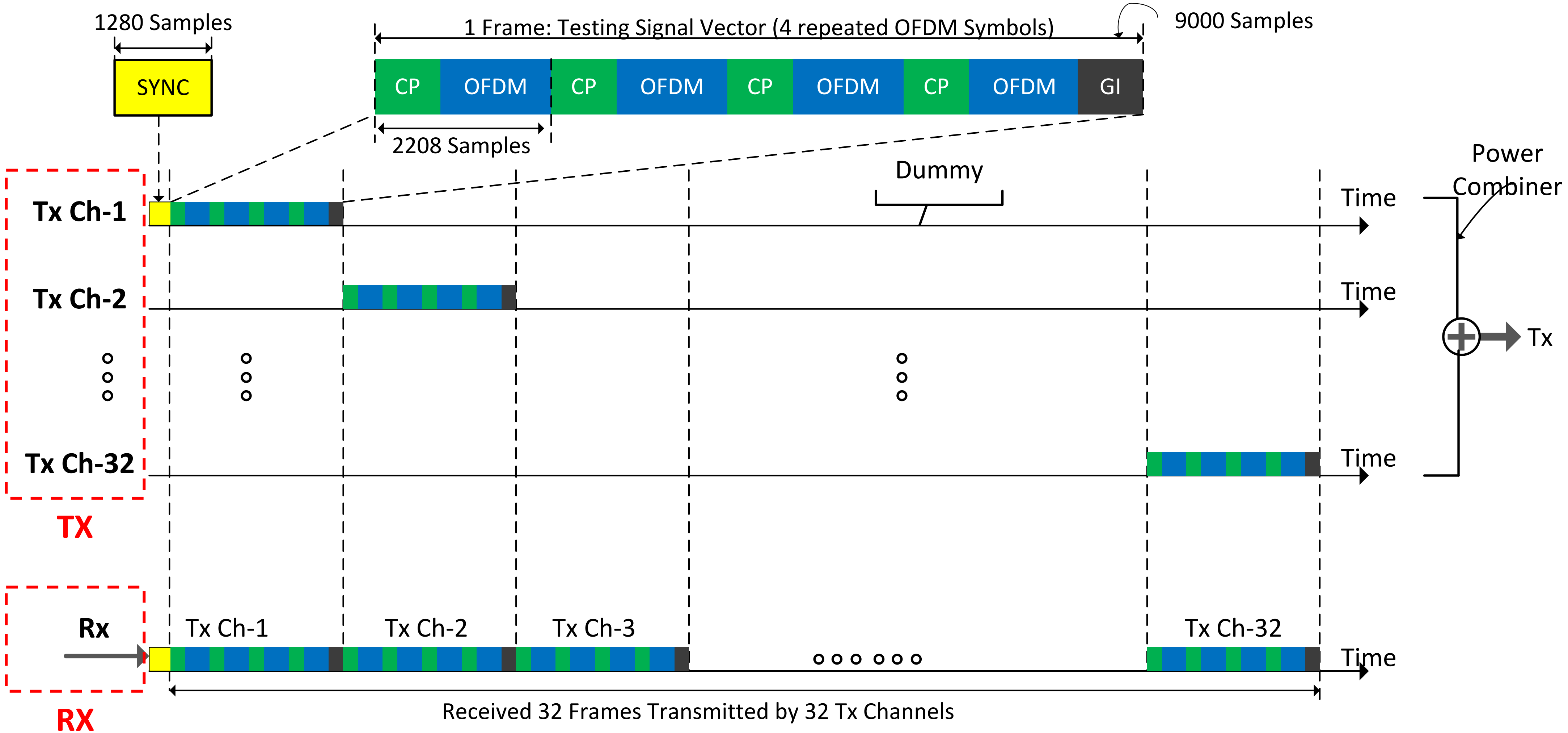
Block Diagram of Test Signal Vector for 32 Transmit Channels



CP Cyclic Prefix (CP)

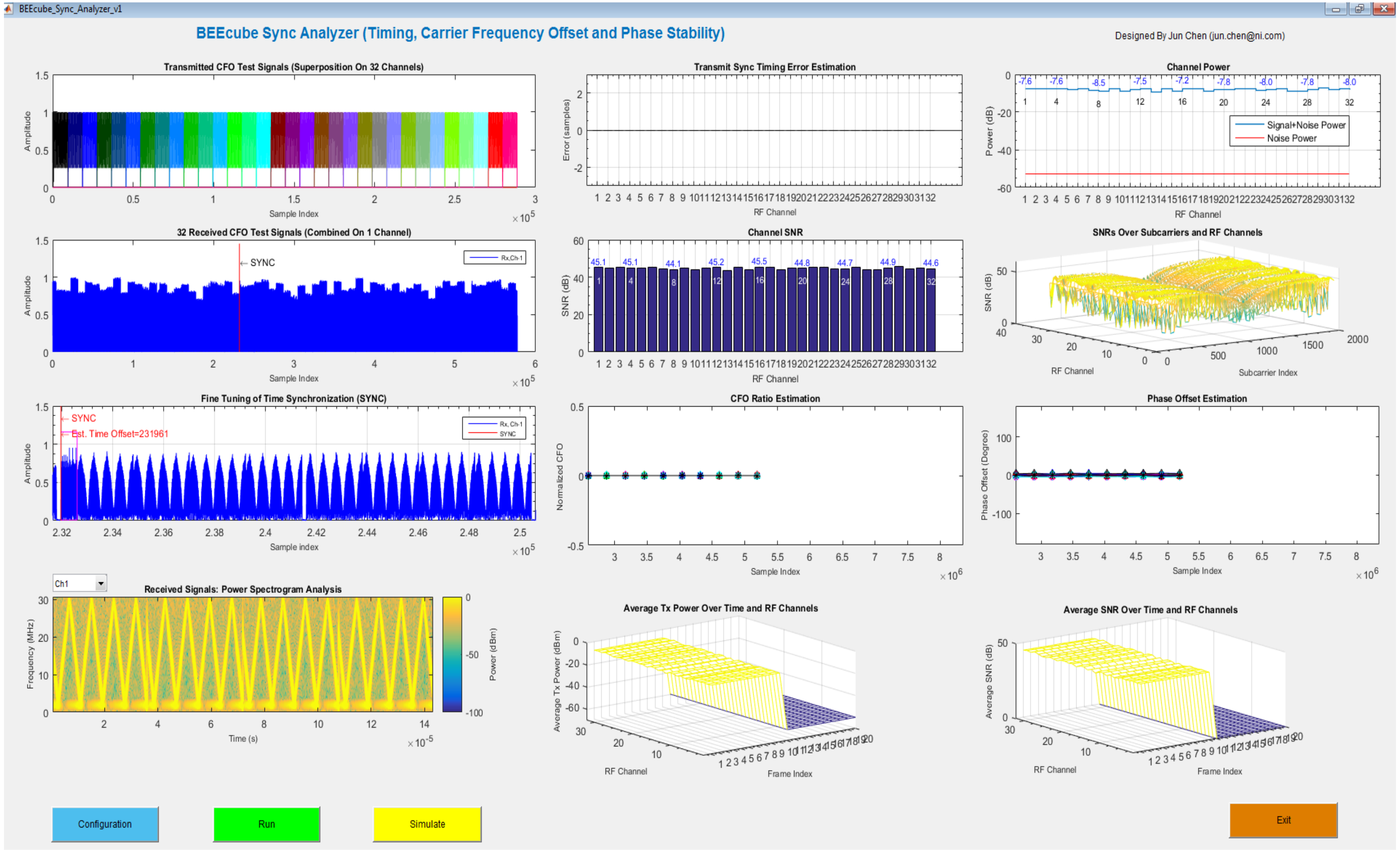
OFDM OFDM Symbols

GI Guard Interval (GI)

SYNC Synchronization Header

Massive MIMO Sync Analyzer

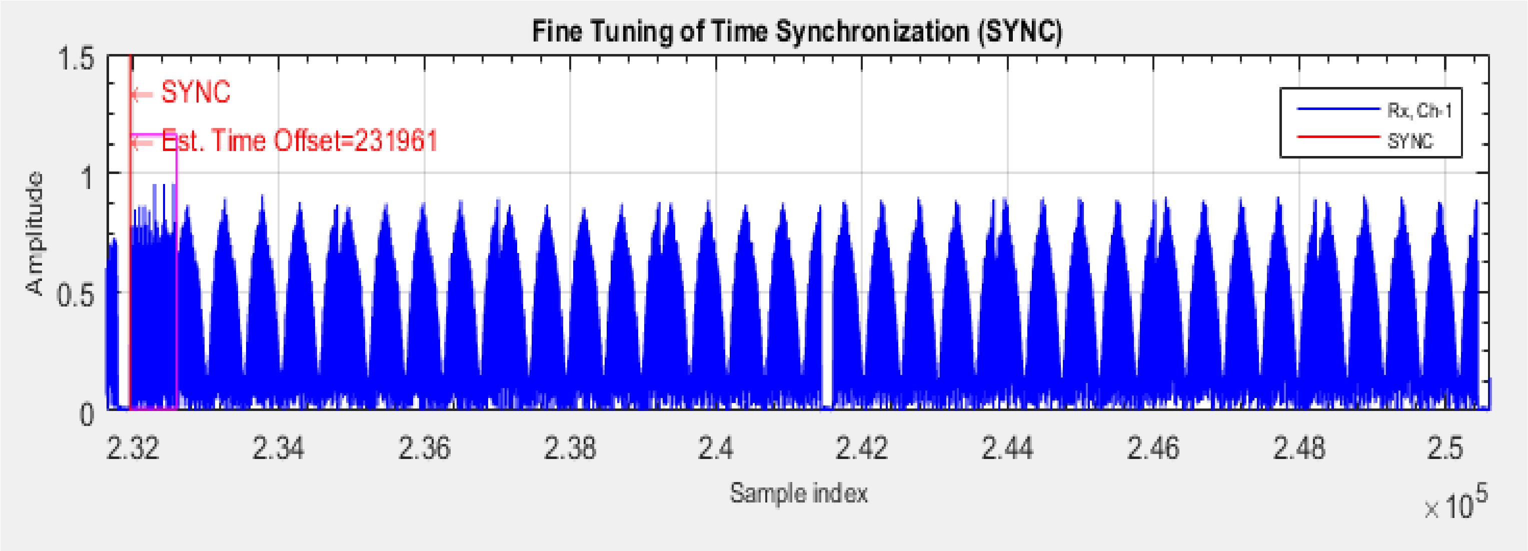
Graphic User Interface (GUI) of Massive MIMO Sync Analyzer



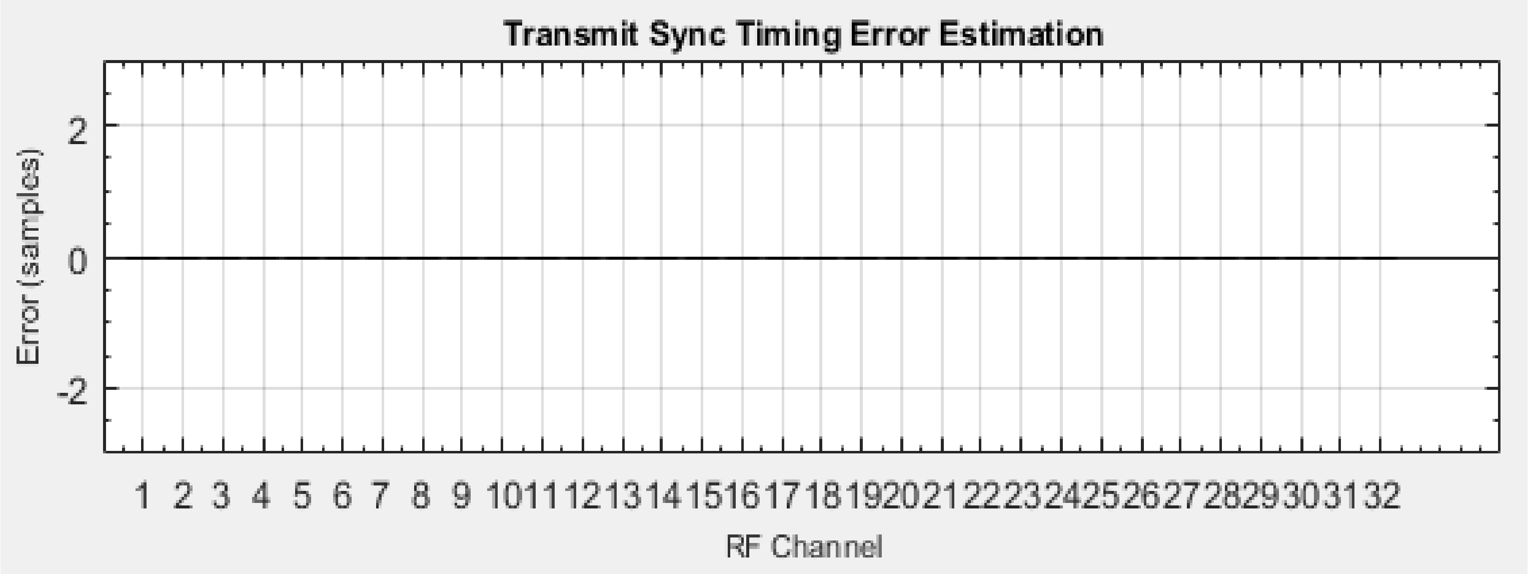
List of Measurements:

- **Sync Timing Error**
- **Carrier Frequency Offset (CFO)**
- **Phase Offset**
- **Average TX Power Over Time and Channels**
- **SNR over Subcarrier**
- **Power Spectrogram Analysis**

Timing Synchronization Error Estimation

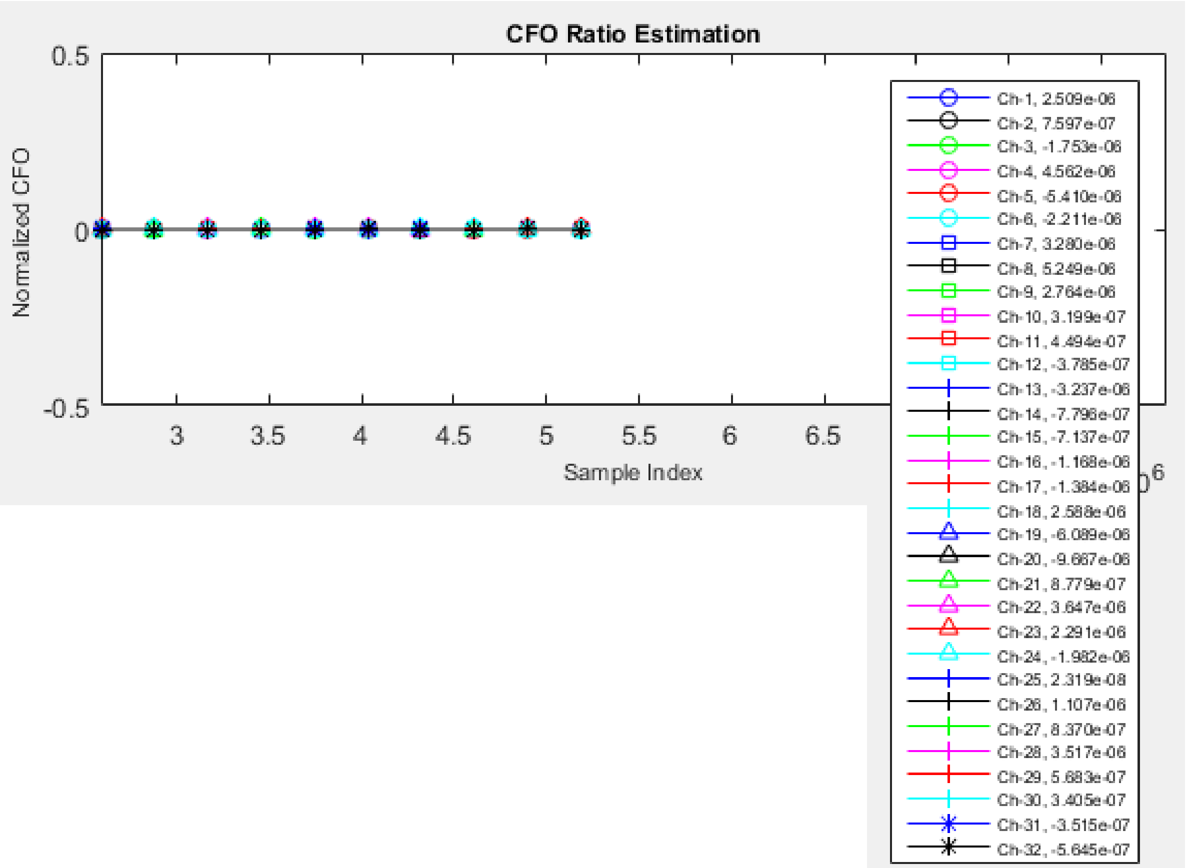


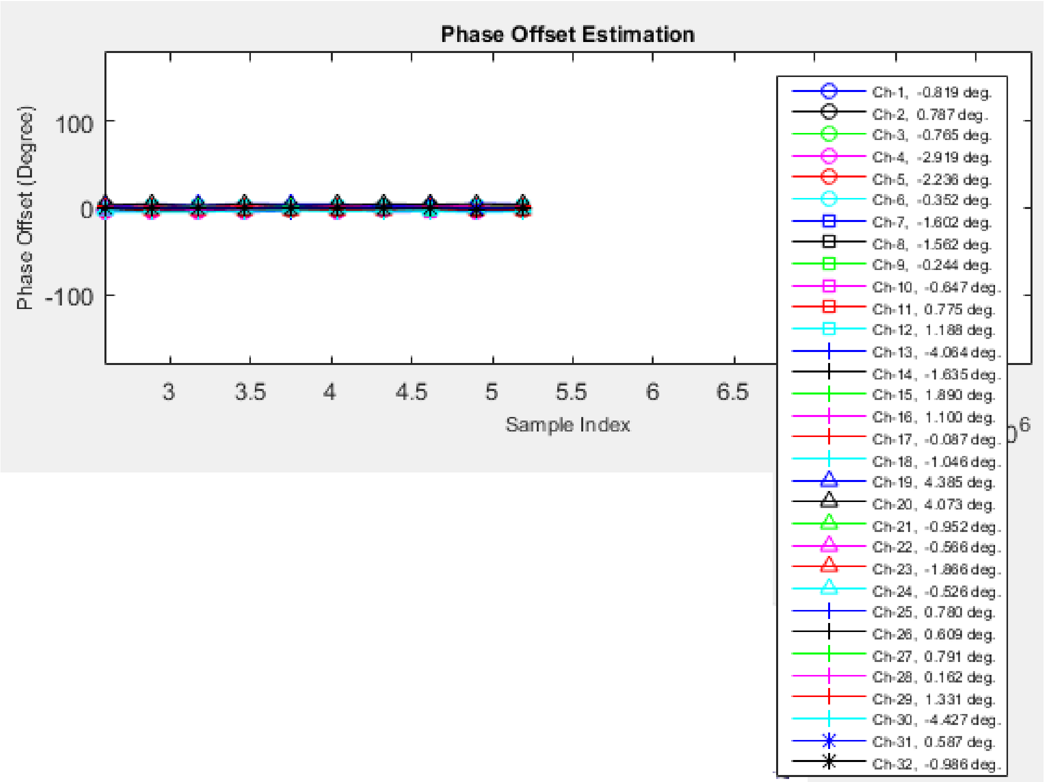
Fine tuning for timing synchronization header



Timing synchronization error across 32 transmit RF ports

CFO and Phase Stability Estimation





This plot shows that the normalized CFO estimation varies with time and RF ports (channels). The CFO ratio (-0.5 < CFO ratio < 0.5) is referred to bandwidth of subcarrier. The average CFO ratio is less than 5×10^{-6}.

The phase stability averaged over one hour measurements on selected RF channels is estimated as low as +/-0.5 degree.

Conclusions

- Introduce architecture, challenges and synchronization techniques in prototyping a 128x128 MIMO systems
- Propose a joint detection method for timing synchronization error, CFO and phase offset across multiple channels.
- Show good results of high-precision synchronization: the timing error less than 1 sample period, the CFO less than 0.1 Hz and the phase stability less than 0.5 degree at room temperature.

Thank you!

Questions?