ANALOG-TO-DIGITAL CONVERSION – THE BOTTLENECK FOR SOFTWARE DEFINED RADIO FRONTENDS

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ABSTRACT

Multi-standard capability of current wireless equipment requires a major degree of complexity and flexibility of classical radio frontends. Wideband architectures in combination with software defined radio (SDR) technologies can considerably reduce the demands on the analog frontends. Consequently, analog-to-digital converters (ADC) with high sampling rates and large dynamic range are necessary. Even though current ADCs are improving steadily, they are still one of the limiting components in software defined receivers.

This paper gives an overview of the state-of-the-art of analog-to-digital converters and dynamic range enhancement techniques like signal averaging or non-uniform quantization.

1. INTRODUCTION

An increasing number of radio access technologies and frequency bands for mobile communications present a major challenge for the equipment manufacturers. Future base stations have to handle GSM (Global System for Mobile Communications) with EDGE (Enhanced Data rates for GSM Evolution), UMTS (Universal Mobile Telecommunications System) with HSPA (High Speed Packet Access) and LTE (Long Term Evolution), handsets additionally Wi-Fi, near field communication (NFC), Bluetooth, ultra-wideband (UWB) or GPS (Global Positioning System) in a frequency range between roughly 800 and 3000 MHz. Therefore, software defined radio is considered the most attractive technology to meet the multi-standard and multi-band challenges for future radios.

There are several architectures of radio frequency (RF) frontends for multi-standard and multi-band radios. It is now 20 years since J. Mitola III coined the term *software radio* in 1992 and with that the vision of a radio only defined by software [1]. The idea behind is to abstain from an RF frontend and do everything in software. Of course, some RF components like antennas, low noise amplifiers (LNA), power amplifiers (PA) and anti-aliasing filters will still be necessary in most instances. However, there are no mixers or band filters which are otherwise required in conventional RF frontends.

The determining component of a software radio receiver is the ADC. Since there are no frequency selective components in that kind of frontend, all interferers reach the ADC without any attenuation. Svensson pointed out that the transmit signal of a GSM terminal can reach a power of up to -3.5 dBm at the antenna of a second terminal 2 m away [2]. A dynamic range of at least 110 dB is required in order to not decrease the sensitivity of that terminal. In addition to the dynamic range requirement, the consumed power of an ADC with more than 6 GHz sampling rate and the desired dynamic range would be not acceptable [3].

For multi-band application with carrier frequencies of up to 3 GHz, direct sampling seems not to be feasible in the near future. However, software radios are already available for HF receivers with a performance comparable to a high performance conventional architecture [4], [5]. Several technologies and techniques have been developed to increase the dynamic range of the analog-to-digital conversion in order to face the challenges of future software defined radios.

This paper reviews the process of the analog-to-digital conversion in Chapter 2, in Chapter 3 provides an overview of ADC technologies and the dynamic performance currently available in research and products. Chapter 4 provides methods and techniques to enhance the dynamic range of the analog-to-digital conversion on board level, and finally, Chapter 5 concludes this paper.

2. ANALOG-TO-DIGITAL CONVERSION

The process of the analog-to-digital conversion comprises three operations: 1) sampling, as a conversion from continuous time to discrete time; 2) quantization, as a conversion from continuous values to discrete values; and 3) coding, generating a binary representation of the sampled value.

2.1. Sampling

Ideal sampling is expressed as the multiplication of the analog signal $x(t)$ and a periodic pulse train $s_a(t)$

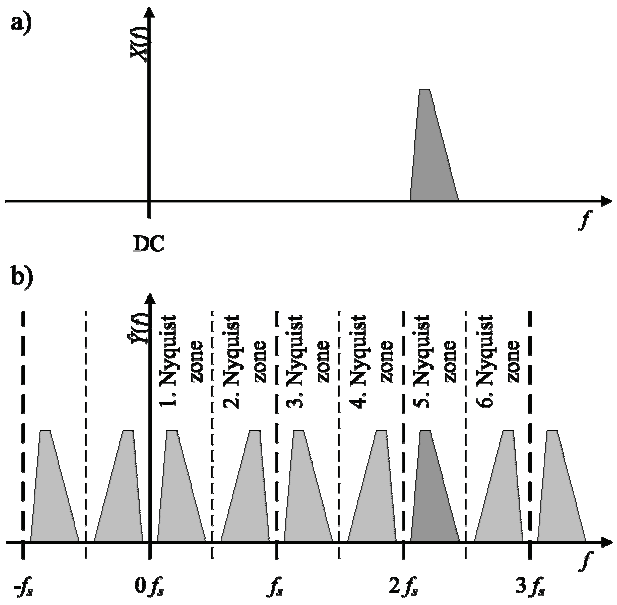

Fig. 1: Sampling process: Spectrum of a) continuous time signal, b) images created by sampling

$$\hat{y}(t) = x(t) \cdot s_a(t) = x(t) \sum_{n=-\infty}^{\infty} \delta(t - nT) = \\ = \sum_{n=-\infty}^{\infty} x(nT)\delta(t - nT). \tag{1}$$

$s_a(t)$ can also be described as a Fourier series

$$s_a(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT) = \frac{1}{T} \sum_{n=-\infty}^{\infty} e^{jn\frac{2\pi}{T}t}. \tag{2}$$

Substituting equation (2) into (1), we obtain

$$\hat{y}(t) = \frac{1}{T_S} \sum_{n=-\infty}^{\infty} x(t) e^{jn\frac{2\pi}{T_S}t}. \tag{3}$$

With the frequency shift property, we obtain for the Fourier transformation

$$\hat{Y}(f) = \frac{1}{T_S} \sum_{n=-\infty}^{\infty} X(f - nf_S), \tag{4}$$

with $f_S = 1/T_S$.

It can be seen from (4) that the spectrum of the sampled signal includes the spectrum of the original signal, but also an infinite number of images spaced at multiples of the sample frequency. The result of the sampling process of a bandpass signal is illustrated in Fig. 1. We can conclude that the analog signal has to be bandlimited to at least half of the sample frequency f_S in order to prevent aliasing. Fig. 1 demonstrates how subsampling can be used to shift a bandlimited signal to a low intermediate frequency (IF) by using a digital low-pass filter.

2.2 Quantization

After sampling, the resulting numbers still can take on an infinite amount of values, which cannot be represented by a digital word. With quantization, each sample is mapped to a discrete value causing a quantization error $e_k(x)$. Assuming $e_k(x)$ has zero mean and is uniformly distributed within a quantization step, the power of the quantization error can be calculated for an ideal ADC according to [6]

$$P_q = \sigma^2 = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e_k^2(x) dx = \frac{\Delta^2}{12}, \tag{5}$$

with Δ being the value of a quantization step.

If the analog input signal of the ADC is zero mean and uniformly distributed, the signal-to-quantization-noise ratio (SQNR) is

$$\begin{aligned} \text{SQNR} &= 10 \log_{10}\left(\frac{P_s}{P_q}\right) \text{dB} = 10 \log_{10}\left(\frac{V_{FS}^2}{\Delta^2}\right) \text{dB} = \\ &= 10 \log_{10}(2^{2N}) \text{ dB} = 6{,}02N \text{ dB}, \end{aligned} \tag{6}$$

with $V_{FS} = \Delta \cdot 2^N$ denoting the full scale voltage, and N the number of ADC bits. Typically, analog signals are not uniformly distributed. If the peak-to-average power η of the signal is known, the SQNR is calculated according to

$$\begin{aligned} \text{SQNR} &= 10 \log_{10}\left(\frac{P_{s,peak}/\eta}{P_q}\right) \text{dB} = \\ &= 10 \log_{10}\left(\frac{\left(V_{FS}/2\right)^2}{\eta\sigma^2}\right) \text{dB} = \\ &= 6{,}02N + 4.77 - 10 \log_{10}(\eta) \text{ dB}. \end{aligned} \tag{7}$$

The signal-to-quantization-noise ratio of a sinusoidal input signal is the well-known equation

$$\text{SQNR}_{\text{sinus}} = 6{,}02N + 1{,}76 \text{ dBFS}. \tag{8}$$

2.3 Coding

The digital output of the quantizer is coded to a specified output format. Typically, ADCs use straight binary codes with 0 as minimum and $2^N - 1$ as maximum value for single ended inputs, and two's complement with 2^{N-1} as most negative and $2^{N-1} - 1$ as maximum value for differential inputs. Other codes like Gray or BCD coding are possible but scarcely used.

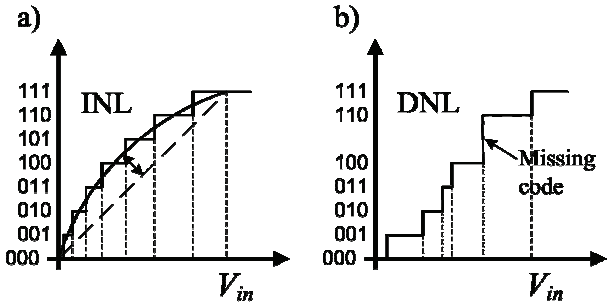

Fig. 3: 3-bit ADC with a) integral non-linearities, b) differential non-linearities

2.4 Non-ideal analog-to-digital conversion

So far, we only have considered ideal ADCs. In practice, the ADC comprises imperfections which limit the performance.

2.4.1 Static converter characteristics

Though the analog-to-digital conversion is a non-linear process, the transfer characteristic can be approximated within the input range of the converter by the linear equation $D = K + GA$, where D is the digital output, A the analog input signal, and K and G are constants. Linear errors occur if K (*offset error*) and G (*gain error*) are not ideal. Non-linear errors are separated into *integral non-linearities* (INL) and *differential non-linearities* (DNL) as illustrated in Fig. 3.

INL is defined as the maximum deviation of the transfer characteristic from a straight line. Two different methods are common to define INL with different results: 1) maximum deviation from the ideal transfer characteristic, and 2) maximum deviation from a straight line with minimum mean squared error (MSE) to the measured characteristic. Typically, the first method is used for values in datasheets.

The change of the input amplitude by $\Delta = V_{FS}/N$ is causing a step of 1 LSB at the digital output of an ideal ADC. The maximum deviation thereof is defined as the DNL. DNL can result in *missing codes* meaning that a quantization level is missing.

All four errors of the transfer characteristic are causing signal distortion and reducing the dynamic performance of the ADC. For choosing the right ADC for a communication receiver, the dynamic characteristics are of greater significance than the static ones.

2.4.2 Noise performance

In Section 2.2 we have already calculated the quantization noise and the SQNR of an ideal ADC, but we have not considered its spectral distribution. Bennett derived in [7] that the quantization noise is typically Gaussian distributed and white within the Nyquist bandwidth.

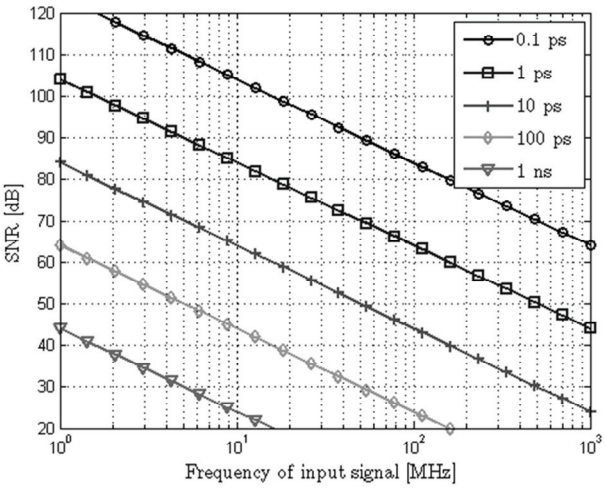

Fig. 2: SNR degradation due to jitter

Quantization noise is not the only and not necessarily the most significant noise source within an ADC. According to [8], three other noise sources can degrade the signal-to-noise ratio (SNR): 1) thermal noise, 2) jitter, and 3) comparator ambiguity. Thermal noise is generated at the analog frontend of the ADC by temperature dependent random movement of electrons in resistive components. Assuming a full scale sinusoidal input signal, the SNR affected by thermal noise in reference to the input is given by the equation

$$\mathrm{SNR}_{\mathrm{therm}} = 10\log_{10}\left(\frac{\Delta^2 \cdot 2^{2N}}{16kTR_{\mathrm{eff}}f_S}\right)\ \mathrm{dBFS}, \qquad (9)$$

with k being Boltzmann's constant $1.38 \cdot 10^{-23}$ J/K, T the temperature in Kelvin and R_{eff} the effective ohmic resistance, representing the complete thermal noise power of the ADC.

So far we assumed an ADC sampling the signal with a periodic pulse train. Due to imperfections of the sample and hold circuitry (*aperture jitter*) and phase noise of the external sample clock (*clock jitter*), the time $T_S = 1/f_S$ is constant in average but not from one sample to the next. The error caused by jitter is proportional to the slew rate of the input signal. That implies higher errors with increasing signal frequency. We assume a sinusoid full scale input signal $v(t) = V_{FS}/2\ \sin(2\pi ft)$. Using that, the derivation of a sinusoid is again sinusoidal and the RMS value of a sinusoid is the amplitude divided by $\sqrt{2}$, the SNR caused by jitter is

$$\mathrm{SNR}_{\mathrm{jitter}} = 20\log_{10}\left(\frac{1}{2\pi f\tau_a}\right)\ \mathrm{dBFS}, \qquad (10)$$

where τ_a is the RMS jitter. The resulting degradation of the SNR due to jitter is illustrated in Fig. 2.

The fourth noise source is based on the finite regeneration time constant of the comparators. According to

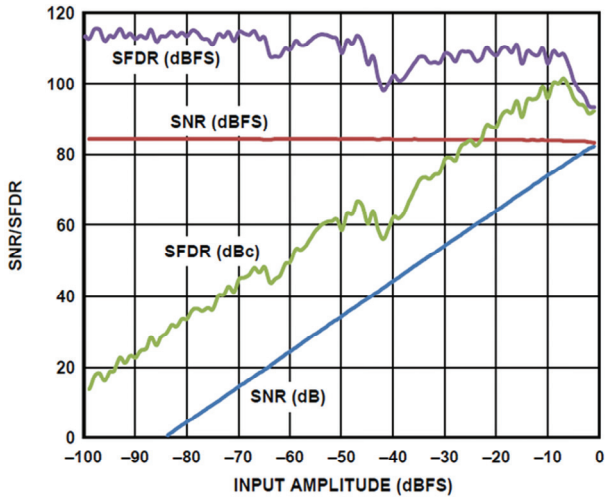

Fig. 4: SNR and SFDR of the 16-bit ADC AD9650 versus input amplitude (from [8])

[8], the effect is only significant at frequencies above several GHz and shall not be further considered.

The cumulative SNR is calculated according to

$$\mathrm{SNR} = -20\log_{10}\sqrt{\sum\left(10^{-\frac{\mathrm{SNR}_i}{20}}\right)^2}, \qquad (11)$$

with SNR_i being the signal-to-noise ratio caused by one individual noise source. Like the quantization noise, we also consider the cumulative noise as white within the Nyquist bandwidth. Since the total noise power does not depend on the sampling frequency, we can conclude that increasing the sampling frequency will improve the SNR with respect to the channel bandwidth (BW). This so-called *processing gain* is increasing the SNR to

$$\mathrm{SNR}_{\mathrm{channel}} = \mathrm{SNR} + 10\log_{10}\left(\frac{f_S}{2\cdot \mathrm{BW}}\right)\ \mathrm{dB}. \qquad (12)$$

Assuming an ADC with $f_S = 104\ \mathrm{MSample/s}$ and 82 dB SNR, sampling the complete 35 MHz wide GSM900 band we calculate the SNR with respect to the 200 kHz GSM channel to

$$\mathrm{SNR}_{\mathrm{channel}} = 82 + 10\log_{10}\left(\frac{104}{2\cdot 0.2}\right)\ \mathrm{dB} = \\ = 106.1\ \mathrm{dB}. \qquad (13)$$

2.4.3 Spurious Signals

Similar to non-linearities in the analog domain, INL and DNL add harmonic distortion to the digitized signal. *Total harmonic distortion* (THD) is one measure to determine the dynamic effect of the non-linearity of the ADC and is calculated using

$$\mathrm{THD} = 10\log_{10}\left(\frac{\sum_{i=2}^{\infty} P_i}{P_0}\right)\mathrm{dB}, \qquad (14)$$

with P_0 being the power of the fundamental and P_i the power of the i-th harmonic. Typically, only the first five harmonics are considered. The THD is a measure of how much power is lost in the harmonics, but of minor interest for communication receiver applications since the lost power can be neglected due to the high linearity of state-of-the-art ADCs.

For a software defined radio receiver, the spurious-free dynamic range (SFDR) is given particular attention, instead. The SFDR is the relation of the strongest spur within the Nyquist bandwidth to the power of the fundamental. For an SDR receiver, the power of the highest spurious signal is important, because generated by an interferer it can cover the wanted signal. Typically, second and third harmonics of the input signal are most significant. Using equation (4), we discover that harmonics, which are initially outside, convolute into the Nyquist band and become relevant. A careful selection of the IF and sampling frequency ensures that the highest spurious fall outside the frequency band of interest and improves the effective SFDR.

In contrast to non-linear distortion in analog circuits, the power of the spurious signals in state-of-the-art ADCs is almost independent of the input signal power, as depicted in Fig. 4. This example of a state-of-the-art 16-bit ADC shows clearly a linear degradation of the SFDR with decreasing input power. Only close to full scale, the behavior is opposite.

In addition to harmonics, two or more in-band interferers can cause harmful intermodulation distortion (IMD). Most attention is turned on third order IMD at $2f_2 - f_1$ and $2f_1 - f_2$, where f_1 and f_2 are the frequencies of interfering signals.

3. ADC ARCHITECTURES

There are quite a few ADC architectures known with pros and cons which shall not be considered here in detail for which comprehensive information is found in the literature (e.g. [6]). Flash converters promise the highest sampling rates, because the result is generated within one single clock cycle. The high speed is bought by a huge circuit complexity if high resolution is required. The number of comparators grows exponentially with the resolution bits of the ADC and a 12-bit converter necessitates already 4095 equal comparators. The power consumption increases also with the number of comparators and therefore, flash converters are common only for high speed applications (several GSamples/s) with resolutions up to 8 bits.

Most of the state-of-the-art ADCs for wireless communications receiver applications are folded flash, subranging or pipelined architectures. These architectures use more than one flash ADC with reduced resolution. There are several clock cycles necessary to generate the

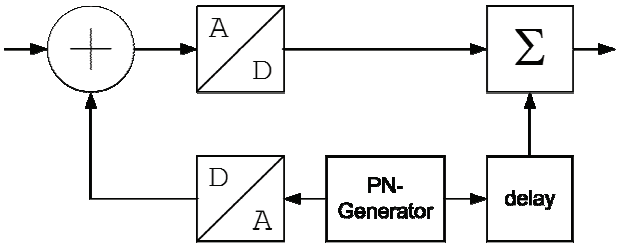

Fig. 5: Subtractive large-scale dither

digital output signal of the converter, which limits the maximum sampling speed.

Within recent years, ΣΔ-converters found their way also into wireless communication receivers. Their high dynamic range is achieved by oversampling in combination with noise shaping. The maximum oversampling ratio and stability of the noise shaping loop limit the useable bandwidth to about 10 MHz.

A good overview of published ADC performance can be found in [10]. State-of-the-art converters currently available on the market achieve an SNR around 80 dB and an SFDR of almost 100 dB at sampling rates above 100 MHz.

4. DYNAMIC RANGE ENHANCEMENT TECHNIQUES

Even though ADC performance is increasing permanently, their SNR and SFDR will be not sufficient for multi-standard, multi-band Software Radios within the near future. However, there are a few measures able to increase the dynamic range of an SDR receiver which shall be discussed within this chapter.

4.1 Automatic Gain Control

Almost every wireless receiver comprises an automatic gain control (AGC) to react on changing input levels. In classical analog frontends, the gain is controlled for maximum signal to noise and distortion ratio (SINAD) within the wanted frequency channel. Actually, the dynamic range of an AGC is only limited by the dynamic range of the controllable amplifiers or attenuators of the analog frontends which can be up to several tens of dB. With software radios, the situation is more critical. No narrowband filters suppress interfering signals before analog-to-digital conversion and controlling the gain for optimum SINAD of the wanted signal might not be possible.

The main goal of the AGC is to ensure not to overdrive the ADC. Of course, other constrains like linearity of amplifiers and mixers have to be considered, too. A strong interferer could cause the AGC to attenuate the received signal so far that the SINAD for the wanted signal is not anymore sufficient for correct demodulation. Therefore, *a priori* information about the expected waveform and the actual interference scenario can help to find the optimal AGC parameters (e.g. time constants, switching thresholds). More details available about the AGC loop dynamic behavior can be found in [11].

4.2 Dither

In literature, two different forms of dither are known: small scale and large scale dither. In Section 2.4 we assumed uniformly distributed quantization errors and therefore a white quantization noise. Depending on the input signal, this is not always the case. According to Bennett, quantization noise is only white if the input signal is random to a certain extent and exercises a high number of quantization levels of the ADC [7]. This is e.g. not true for small sinusoidal input signals. In order to get a flat frequency response of the quantization noise in any case, a so-called small-scale dither signal is added before quantization. [12] and [13] demonstrate that an additive random signal in the range of $\pm\Delta/2$ eliminates the nonlinearity and whitens the noise. The noise power added to the signal is equal to the quantization noise and the noise power increases by 3 dB, which typically can be neglected compared to thermal noise and jitter SNR degradations.

Small-scale dither is not able to whiten the distortion caused by the INL of the ADC and a higher power of the dither signal is required. This dither signal adds a significant amount of interference. There are two methods known to remove this interference from the digital signal: If band-limited noise is added in a frequency range outside the wanted frequency channel, it can easily be rejected by digital filtering. The second method is to generate a pseudo random noise (PN) sequence in the digital domain and to add it after a digital-to-analog conversion before quantization. The dither signal can be subtracted afterwards in the digital domain (see Fig. 5). If the dither level is well adjusted, a significant increase of SFDR can be achieved. Estrada showed in [14] a 13 dB improvement of the SFDR of an 8-bit high-speed ADC by injection of a band-limited dither signal. Note that dithering can only reduce spurious signals caused by the quantizer. Spurs generated e.g. by non-linearities of the frontend are not affected.

4.3 Non-uniform quantization

In order to still be able to receive a weak signal in the presence of a strong interferer, one approach is to quantize small levels with fine quantization intervals and strong levels with coarse intervals. This technique is well-known in audio signal processing. Non-uniform quantization can be performed with particularly designed ADCs, but it is more common to use an analog compressor and a uniform

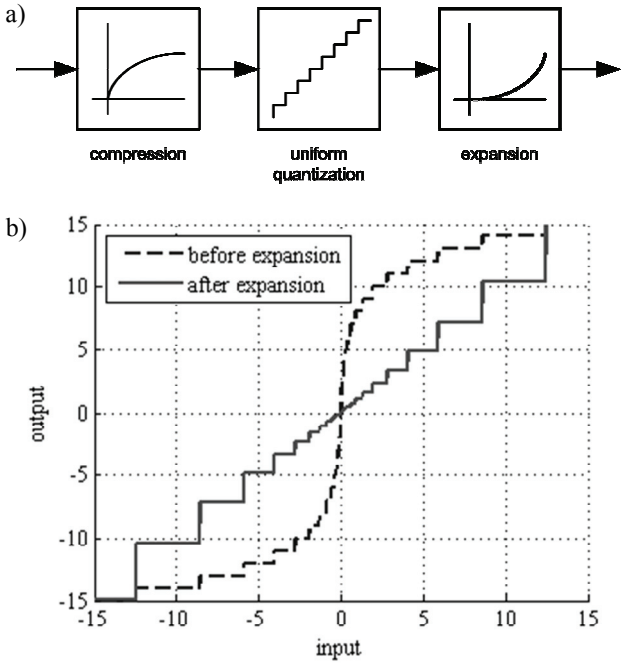

Fig. 6: Non-uniform quantization a) block diagram b) μ-law compression with 8-bit quantizer, μ = 255

quantizer. For compensation of the non-linearity, a digital expansion is necessary after analog-to-digital conversion as shown in Fig. 6a, e.g., a μ-law non-linearity can be used for a compression according to

$$y(x) = \operatorname{sgn}(x)\frac{\log(1+\mu|x|)}{\log(1+\mu)}. \qquad (15)$$

Fig. 6b shows the characteristic of the output signal of the uniform quantizer and the expander, respectively.

Fox demonstrates in [15] that non-uniform quantization does not work properly for an SDR receiver. The weak signal is superimposed on a strong interfering signal and is experiencing fine and coarse quantization depending on the current level of the interferer. Fig. 7 illustrates the difference of the power spectral density (PSD) for uniform and non-uniform quantization. In both cases, a 14-bit uniform quantizer was simulated, the non-uniform quantization was generated by a μ-law compressor with μ=255.

In a), a weak QPSK-signal was used as an input signal. Due to the finer quantization of small input levels, the non-uniform quantization shows an improved SNR. The plot shows also that the uniformly quantized PSD exhibits a non-white noise characteristic since the input signal contains only little frequency content and is utilizing only a few quantization levels.

In b), the input signal additionally contains a strong QPSK-interferer. Now, non-uniform quantization results in higher quantization noise due to reasons described above. Non-uniform quantization does not seem to give an improvement for SDR receivers, since receiving scenarios

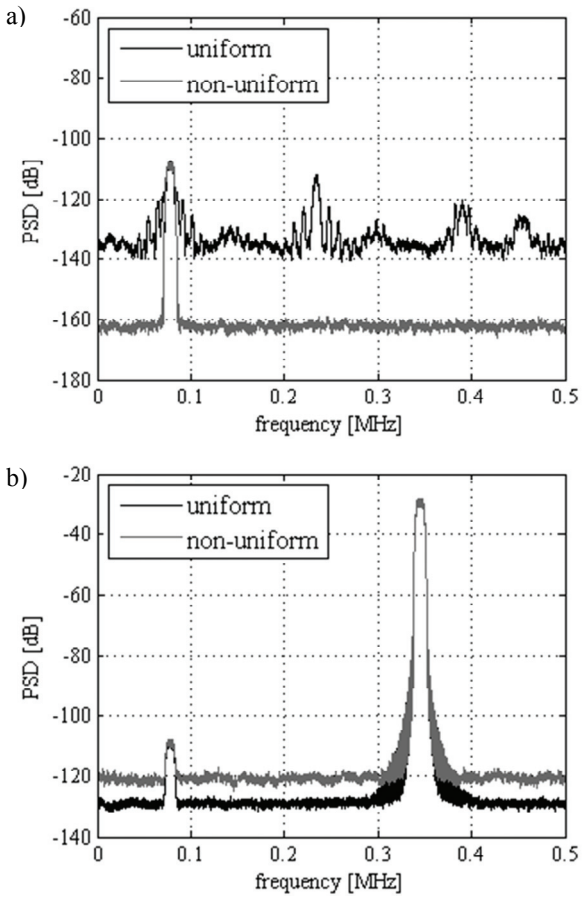

Fig. 7: Uniform and non-uniform quantization, N=14, μ=255 a) PSD of a weak signal b) PSD of a weak signal and a strong interferer

similar to these simulated in case a) can be managed by an AGC.

4.4 Oversampling and time-interleaved ADCs

The complete noise power of the analog-to-digital conversion is considered to be within one Nyquist bandwidth ($f_S/2$). Assuming white noise, the SNR improves with increasing sampling frequency f_S. Doubling of the sampling frequency increases the channel related SNR by 3 dB as shown in Equation (12). In addition, oversampling relaxes the requirements for the anti-aliasing filter, but increases the power consumption and is limited by the maximum sampling rate of the ADC.

With time-interleaving of two or more ADCs the sampling rate can be increased beyond the maximum sampling rate of the single component. The technique was first disclosed by Black and Hodge in [16]. Each ADC samples the same input signal with the same frequency f_S, but with a different phase of the sample clock. The phase of

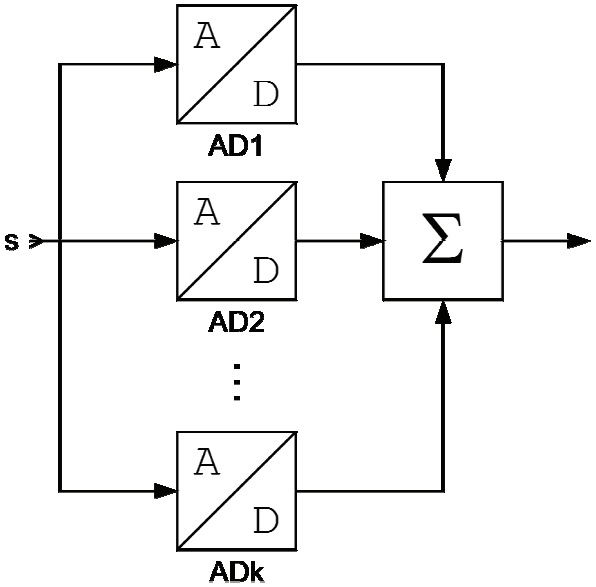

Fig. 8: Signal averaging with parallel ADCs

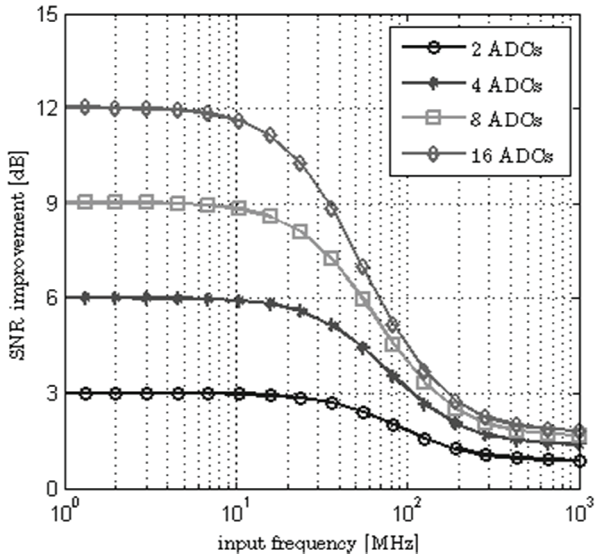

Fig. 9: SNR improvement with signal averaging; data were calculated with SNR_{therm} = 82 dB, τ_a = 75 fs, and τ_c = 100 fs

the sample clock for the individual ADC can be calculated according to

$$\varphi_k = 2\pi \cdot \left(\frac{k-1}{K}\right), \qquad (16)$$

with k being the individual ADC and K being the total number of time-interleaved ADCs. The output signals of the ADCs is multiplexed to result in a total sampling rate of $K \cdot f_S$.

The spurious performance of a time-interleaved ADC depends on the offset, gain and phase matching of the ADCs. The effect of these errors is thoroughly analyzed in [16], [17] and [18]. Spurs caused by offset errors are almost independent of the input signal and occur at multiples of f_S, while spurs due to gain or phase errors depend on the input signal and occur at $f_{in} + i \cdot f_S$, with f_{in} being the frequency of the input signals and $i = 1,2,3,...$ [17] provides the theory and the equations to calculate the resulting SFDR. [18] demonstrates that a gain and phase error of 0.02% causes an SFDR of 74 dB. Digital post-processing can improve the spurious response of time-interleaved ADCs in the presence of mismatch (see e.g. [18]).

4.5 Signal averaging

A further method to improve the SNR of the analog-to-digital conversion was first presented by Seifert and Nauda in [19], known in the literature as signal averaging with parallel ADCs. The idea behind signal averaging in general is increasing the SNR by generating and adding several replicas of the wanted signal. If the noise of the replicas is uncorrelated, it adds on an RMS basis, while the signal adds coherently.

The principle of the technique is illustrated in Fig. 8. Every ADC runs with the same sampling clock. Assuming uncorrelated noise, the SNR increases by 3 dB with every doubling of the number of parallel ADCs. In practice, only thermal noise and aperture jitter is uncorrelated, while clock jitter and quantization noise has to be assumed to be correlated. With that, the SNR is a function of the frequency of the input signal for k parallel ADCs according to [20]

$$\mathrm{SNR} = \left(\frac{1}{k \cdot \mathrm{SNR}_{\mathrm{therm}}} + \frac{(\omega \cdot \tau_a)^2}{k} + (\omega \cdot \tau_c)^2\right)^{-1}, \qquad (17)$$

with τ_a being the RMS aperture jitter, τ_c the RMS clock jitter, and ω the angular frequency of the input signal. The improvement of the SNR for $k = 2 \ldots 16$ ADCs is illustrated in Fig. 9. For SNR and aperture jitter, values from the datasheet of the AD9650 [8] were used and a clock jitter of 100 fs was assumed. Fig. 9 shows that almost no improvement is possible when the clock jitter becomes dominant over thermal SNR. Unfortunately, SFDR does not improve with averaging signal ADCs.

Analog Devices demonstrated about 5.5 dB SNR improvement within the 1st Nyquist zone with its AD10678 comprising four parallel 14-bit ADCs [21].

There has been some effort expended to decorrelate the clock jitter of the individual ADCs e.g. by phase or frequency offsets of the input signal. Lauritzen proves in [20] that 3 dB is the maximum increase of SNR in that case. A further benefit of phase or frequency offsets is the decorrelation of the spurious response. Decorrelation can also be achieved by using independent clock sources for each individual ADC.

5. CONCLUSION

A review of noise and distortion sources limiting the performance of the state-of-the-art analog-to-digital converters was assessed in this paper. There is still a gap between the requirements of a software radio for multi-standard mobile communications receivers and the dynamic range of available ADCs. The paper presented techniques which are able to enhance the dynamic range of the frontend. Automatic gain control is an appropriate method, but the ADC remains the limiting device at the presence of a strong interferer. Significant improvement of the dynamic range can be achieved with signal averaging at the expense of high hardware effort. However, the increase of the SNR is limited to 3 dB at frequencies where the jitter is the dominant noise source.

6. ACKNOWLEDGEMENT

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