Vehicle Power Line Communication (VPLC) implementation with USRP2 Platforms

Philippe Tanguy, Fabienne Nouvel, Clovis Lunel

prenom.nom@insa-rennes.fr

IETR-INSA –Rennes – France

Abstract **- This paper deals with the implementation of an embedded power line communication system for vehicle (VPLC) using USRP platforms and GNU Radio environment. This platform allows a modular design of VPLC. Many configurations of the PHY layer of can be tested in a real PLC environment, without developing them on a specific board. In conjunction with USRPs platform and daughter cards, the signal processing performed in software is transmitted over a real channel. Several frequency bands can be tested by using different daughter cards without changing the signal processing.**

Index terms – USRP, OFDM, PLC

I. INTRODUCTION

Software-defined radio (SDR) [1] has been defined to help the wireless operators to maximise their investments in multiple mobile standards and base stations. With such approach, many of the drawbacks involved with a classical approach (specify FPGA, DSP designs, RF designs) fall down as one can re-use sub-parts of an existing radio system, and just adapt its operation through code reprogramming.
Similar approach can be adopted for wired communication, and more specifically for power line communication (PLC) communication, the radio link is equivalent to the wired PLC.
Today the car manufacturers have to face with an increase of electronic nodes (ECU) connected each other. The ECUs already use networks like CAN and Flexray, but the number of specific wired always increase. One solution to reduce the amount of wires would be to use the PLC technology that is currently being developed for domestic networks to transmit information or at least some of it, over the 12V power distribution system found in cars. However, the PHY layers may be optimised according to the channel states and embedded environment.
Many projects have investigated SDR and cognitive radio using flexible platforms [2]. SDR platforms provide flexibility, reducing the amount of time it takes to develop and update communication systems. With software update, many communication systems can be achieved using the same hardware. SDR technology has first focus on wireless communications. Implementing the new ideas of cognitive radio on inexpensive and known hardware will allow for practical tests. Using software generated standard waveforms "on the fly" reconfiguration will allow radios to fit into rapid prototyping platform.
Today, wired systems are concerned by the issue of spectrum management and aim to provide a single device to network over any supported wire types and more specifically in home. Thanks to the advance made in access technologies, the triple play services become widespread [3]. For example, the recent VDSL2 technology provides high data rate and takes advantages of the higher frequency bands up to 30 MHz. At the same time, the indoor PLC standards take advantage of the power grid in the [2-30] MHz band. VDSL2 and PLC technologies are complementary to provide high data rates by using the telephone copper pair and the power cables.
Nevertheless, the band plans used by both technologies overlap: [0.138 - 30] MHz for VDSL2 and [1.8 - 30] MHz for PLC. Methods to improve the co-existence of different wired standards become necessary.
In addition, the ITU [4][5] has begun to address this "SDR wired" and has specified a PHY layer and the architecture of G.hn, the common name for a home network technology family. A single G.hn device will be able to network over any supported interfaces in home. The advantages are lower costs, lower equipment and lower time development.

In our paper, SDR can be considered to be a "wired" communication system, where some of its functional components, such as modulations, coding, synchronisation, etc., are generated in software and implemented on open hardware. This makes it possible to configure the signal according to the requirements of the application and the characteristics of the communication channel. The software generated signal is then applied to USRP [6] platforms that are connected to a host computer through USB or Ethernet connections. To help the designer, the GNU Radio Companion is a friendly environment for the development of baseband processing thanks to a set of pre-defined block sets, which enables to build a complete radio chain without developing specific code (most of the time).
Ettus Research (part of National Instrument) provides the USRP2 hardware platforms supporting any carrier frequency between DC and 5.9 GHz depending on the daughter board. Then RF to baseband conversion sub-system is ready for prototyping (except specific requirements in terms of transmitting power, depending on each application).
In addition, the GNU Radio Companion [7] is a friendly environment for the development of baseband processing thanks to a set of pre-defined block sets, which enables to build a complete radio chain without developing specific code (most of the time). More recently, MATLAB and Simulink connect to the USRP to provide a radio-in-the-loop design and modelling environment. With the support package, Communications System Toolbox and a USRP radio, it is possible to design and verify practical SDR systems rapidly. Furthermore, comparison between simulation and real environment can be performed using the same developed

algorithms and codes. In this case, the GNU Radio open-source software is not required to use this support package.
In [8] SDR-GNU Radio is used to implement a power line data transmission link between a motor and an inverter, but at a low data rate. In our study, SDR-GNU Radio is used to implement power line communication system in a vehicle (VPLC) for high data rates and non-safety applications. The orthogonal frequency division multiplex (OFDM) is used to efficiency fight against the fadings. The system operates at the center frequency of 12,5 MHz (VPLC) thanks to the daughter boards.

The reminder of the paper is organized as follows. In Section II, the communication system and channel are studied. The OFDM has been chosen for the VPLC communication as for domestic PLC based on different previous works. Using the measurements, we can now optimize some parameters like the CP length, the FFT size, etc. The main idea is to optimize the PHY parameters without developing all the TX/RX boards. Another objective is to be able to test the VPLC modem parameters on other channel (wireless has been tested), by using another RF interface while keeping the same PHY layers. Section III concentrates on GNU Radio and implementation of the data transmission link. The VPLC testbed is based on two USRP2 cards with the daughter board's LFTX and LFRX. Using these daughter boards, the possible operation frequency range is very modular (from DC to 5.9 GHz). Section IV details the results we obtained, both on indoor PLC and VPLC. Section V concludes the paper and perspectives are given.

II. COMMUNICATION SYSTEM AND PHY LAYER

A.Transmission scheme

The orthogonal frequency division modulation or Discrete Multi-Tone (OFDM or DMT) has been chosen for the VPLC communication as for domestic PLC. Several standards with different kinds of multi-carrier modulations like HPAV and HD-PLC [9] are already proposed and investigated. In the previous paper [10][11], different measurements have been performed and have shown the OFDM modulation combined with bit loading and equalization is convenient for VPLC. Those standards have been applied in car to measure data throughput on DC channels [10].
However, the indoor and car channels are different. We need to optimize some parameters like the CP length, the FFT size, and other PHY parameters. The main idea in this study is to optimize the PHY parameters without developing all the hardware of the modem. Another objective is to be able to test the VPLC modem parameters on other channels, by using another RF frontend.

The transmitted OFDM waveform can be expressed as:

$$s(t) = \frac{1}{\sqrt{N_p}} \sum_{m=0}^{N_p-1} R_{eal}\left\{c_m \prod(t) e^{2.j\pi F_m t}\right\} \quad (1)$$

With Np= M/2, M the FFT size, cm the complex symbol on sub-carrier Fm. The sub-carrier spacing Δ_{OFDM} is defined as $1/T_{OFDM}$ with T_{OFDM} the OFDM symbol duration. In order to generate a real OFDM signal, the hermitian symmetry is first applied before the IFFT of size M as depicted in Figure 2. As the indoor and vehicle channels are not completely similar, the CP and FFT size will be optimized in the reminder of the paper.

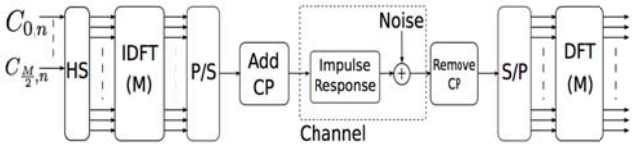

Figure 2. OFDM PLC transmitter and receiver

B.PHY layer specifications

All the PHY parameters have been defined according to the previous channel measurements carried out on different vehicles and described in details in [11]. For the embedded tests, we have used a Peugeot 407SW gasoline.
If we focus on PLC, results in [11] have shown it is possible to reduce the FFT size compared to the HPAV standard, as the coherence bandwidth is about 500 KHz, two times less than in indoor channel. Concerning the CP length, as the mean delay spread is about 135 ns, it can be shorter than the HPAV CP duration of 5.56 us. After software simulations using channel measurements, it is interesting to test different combinations in other VPLC environments like boat or aircraft. By using the VPLC demonstrator, it will be possible to manage rapidly different configurations. The parameters of the VPLC system are summarized in TAB I.

TABLE I. VPLC PARAMETERS

Parameters	**Values**
Transmission bandwidth/sampling rate	DC-25 MHz/25 MHz
M FFT size	1024/512/512
Subcarrier spacing Δ_{OFDM}(KHz)	24.414/48.428
Modulation per carrier(according to bit loading)	BPSK/ QPSK/16QAM/256 QAM
Number of used carriers	412/207/207
CP length(samples)	139/60/20

Theses parameters have been first simulated thanks to MATLAB and with a PLC channel model. In the next step, we will convert the simulations in reality, using the same PHY parameters and using a real channel.

The OFDM symbols are generated and organized in frames. However, it is necessary to generate a synchronization symbol in order to detect the beginning of the useful signal.

C.Time and frequency synchronization

The frame format illustrated in Figure 3 is based on (DMTN+1) OFDM/DMT symbols with a preamble for the time synchronization. Before the frame begins, null symbols are used to separate the different frames. The time synchronization symbol includes a pseudo noise sequence with good autocorrelation property of length equal to (L=M/4) and the CP. The synchronization symbol includes consequently four sequences. Then all the DMT symbols of the file are transmitted. The value of DMTN is configured according to the performances we want to test, with a default tvalue of 20. The synchronization symbol is organized as:

$$[\ P\ P\ -P\ -P\ ] \quad (2)$$

With P the IFFT of the pseudo random sequence of size L.

At the receiver, the synchronization is performed on the first symbol using the Minn & Bhargava algorithm [12] in the time domain. The four sequences of the synchronization symbol are correlated and generate a peak when the sliding window of size M includes these four sequences and zero everywhere else.

The correlation function is given by:

$$R(n) = \sum_{k=0}^{1} \sum_{m=0}^{N_p - 1} r(n + 2Lk + m) r(n + 2Lk + m + L) \quad (3)$$

Figure 4 illustrates the peak when the synchronization is detected. On the green curve, we observe the different peaks given by (3).

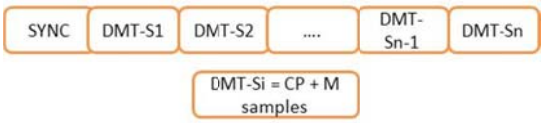

Figure 3. Frame - PHY Layer

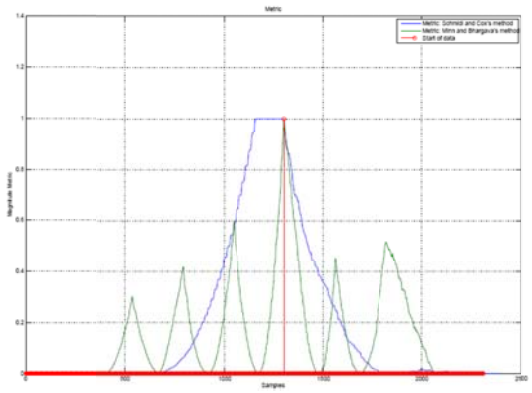

Figure 4 Synchronization detection

The received data begins with the red peak. The blue curve illustrates the algorithm proposed by Schmidl and Cox, which is weaker. This approach is simple and robust enough for our experiments.

This frame structure will be used both for the channel sounding and the data transmission. The length of the frame could be different.

III. USRP2 PLATFORM FOR VPLC

The VPLC platform is based on USRP2 boards combined with daughter boards [6]. Using these daughter boards, the possible operation frequency range is very modular (from DC up to 5.9 GHz). The mother board includes ADC, DAC, a FPGA (Xilinx Spartan XC3S2000) and a Gigabit-Ethernet interface used to transmit data or configuration to the USRP2 board. The two slots of the board are for the front-end daughter boards. As we can see on Figure 5, the two 14-bit ADC and the two 16-bit DAC are independent and can work up to 100 Msps.

For the PLC interface, we use the LFTX and LFRX cards because they allow transmitting and receiving signal from DC up to 30 MHz. These daughter boards include differential amplifiers and low pass filters for antialiasing.

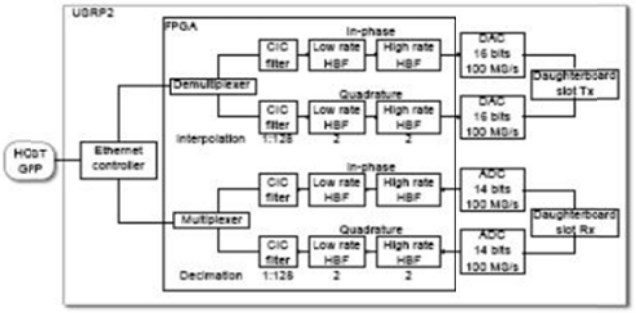

Figure 5. USRP2 board (from [2])

On the transmission side, the real baseband signal is generated thanks to MATLAB and saved in a file. It is then transferred through the Ethernet link to the USRP2 board, converted into analog by one of the two DAC converters and then transmitted over the PLC or RF channel. A passive coupler provides isolation between the output of the card and the PLC link. Both I and Q signal components are transferred to the USRP2 board and can be considered as independent. It is then possible to consider several configurations: real baseband signal (Q =0), complex baseband signal (I and Q), real IF-frequency signal.

At the receiver, the analog signal is translated to baseband and then digital converted. Samples transmitted by the Ethernet link are stored on the workstation. They will then be processed "off line". As above, the ADC conversion paths are independent but must be used consistent with the transmission part.

The maximum bandwidth of the OFDM signal depends on the interpolation and decimation factors N of the ADC and DAC. The sampling rate Fs of the ADC/DAC (Fs at 100MHz) is divided by N (4 to 512) and results in the output sample rate of the data sent from/to the host.

TAB II illustrates some PLC configurations of the USRP2 boards we can use for the transmission of the software generated signal.

TABLE II. USRP2 PLC CONFIGURATIONS

Parameters	Configurations
N =4, I channel	real signal, bandwidth = 12, 5 MHZ
N=4, I& Q complex channels	complex signal , bandwidth = 25 MHZ, external I&Q mixer
N=4, I& Q , two independent real channels	real signal , bandwidth = 12,5 MHZ, two independent transmissions , multiple outputs
N=512, I channel	real signal , bandwidth = 87,5 KHZ, for narrow bandwidth
N=512, I& Q complex channels	complex signal , bandwidth = 195 KHZ , two independent narrow bands transmission

IV. EXPERIMENTS AND RESULTS

The VPLC platform has been tested first for PLC transmissions, both in indoor PLC and VPLC environments. Two USRP2 board are used, one for the transmitter and one for the receiver, allowing a point to point transmission. Thanks to the GNU-Radio interface, we can change easily the configurations as presented in TAB II and adjust the transmitted power. Another important benefit is the option to probe and analyze the signal in the processing chain.
We have first tested our system overs the 220v electrical power. The Tx and Rx USRP2 boards were linked to the 220V power network through couplers plugged on the same multi-outlets. The aim of this test was to prove the concept of SDR over wires. We will describe the VPLC experiments below.

A. VPLC experiments

The two USRP2 boards are arranged in the vehicle according to Figure 5 in points G, F, H and D. We have considered the GH, GF and HD links as in [10]. We will focus on link GF.

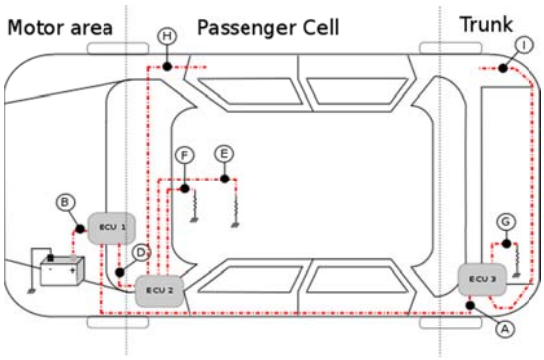

Figure 5. TX/RX VPLC platform

We perform point to point transmission, like from G point to H point. Two scenarios are considered: motor OFF and motor ON. They have been studied in the previous paper [10] with HPAV modified modems.

B. VPLC results

In Figure 6, we can observe the spectrum of the LFTX daughterboard output with a DSP of -80dBm/Hz. The bandwidth [2-12.5] MHz is used. We can observe there are notches compared to HPAV standard.

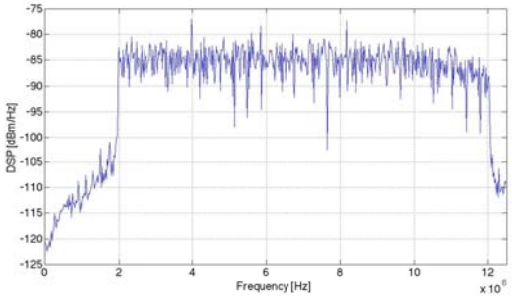

Figure 6. LFTX output spectrum

Before using the VPLC platform for BER measurements, it can be used first as a channel sounder. A sounder enables to point out all the propagation problems and will allow us to optimize the PHY parameters. We first observe the signal to noise ratio for each sub-carrier in the [2-12.5]MHz bandwidth. As the channel is considered as time invariant, the bit loading algorithm will allocate the bits on each sub-carriers at the TX side. Taking into account a referred bit error rate of 10^{-3}, a transmitted power of -80dBm/Hz, the channel capacity definition given in [13], the parameters given in TABLE I and the frame defined in Figure 3, we can achieve a data rate of about 30 Mbps/s.
Then, we performed data transmission according to the frame defined in Figure 3. In this frame, the first two DMT-S1 and DMT-S2 are the estimation symbols we use to equalize the received signal. A ZF equalizer at the receiver compensates the phase rotation due to timing error of the FFT window. However, as the PLC channel is noisy, especially when the motor is ON, the DMT symbols will be corrupted by the impulsive noises and results in false frame detection and bit errors. The SNR is also lower. In this case, the data rate falls down to 7 Mbps. Figure 7 illustrates the received signal during OFDM transmission when motor is ON.

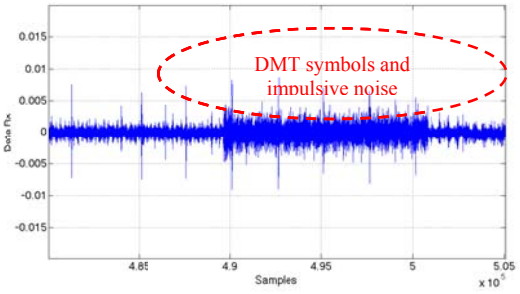

Figure 7. DMT transmission with impulsive noise

With these first results, it is possible to analyze the different combinations proposed in TABLE I.

C. SDR implementation aspects

The VPLC paltform can be used to experiment different PHY parameters using the same hardware.

We have first focus on the CP. During the simulation, we have analyse the CP length according to the link and the FFT size. Results in figure 8 show that the there is an optimum value for the CP according to the FFT size and according to the SNR. It is not necessary to extend the CP with the FFT size. Furthermore, we can adjust the CP according to the point to point communication. Three FFT sizes (256,512,1024) have been experimentend on the VPLC board. We can then generate DMT symbols and frames optimized to the link.

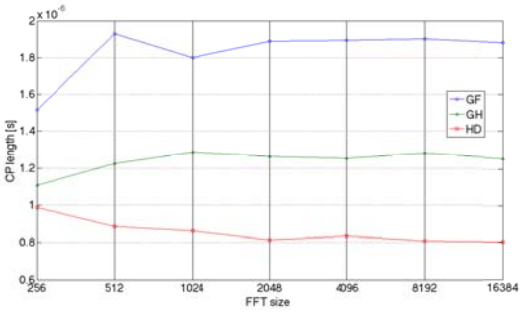

Figure 8. CP length according to FFT length

Additionnaly, the number of used sub-carriers can be modified by introducing notches in sofware. Notches can be introduced when the noise level is very important resulting in no bits allocation. The can be introduced to reduce the transmission bandwidth (upper or lower part) without modifying the analog part. In Section II, we have shown the PHY frame. In this one, it is possible to extend the number of DMT data symbols if the channel is not noisy. If the channel does not change in time, we can estimate it less often and it leads to an increased data rate. Once again, the parameters are software modified. We see that this with SDR approach multiple configurations can be tested in a real system rapidly using the same board.

If we focus on the analog part, it is possible to extend the bandwidth transmission up to 25 MHz by introducing external mixer linked to the outputs (I and Q) of the daughter boards. This work is currently in progress. Figure 9 illustrates the VPLC platform with the software and generic hardware parts.

However, the VPLC is not real time as the received signal is processed “off-line” with MATLAB. It could be possible tu use the GNU-radio interface both to generate the waveform and to configure the board.

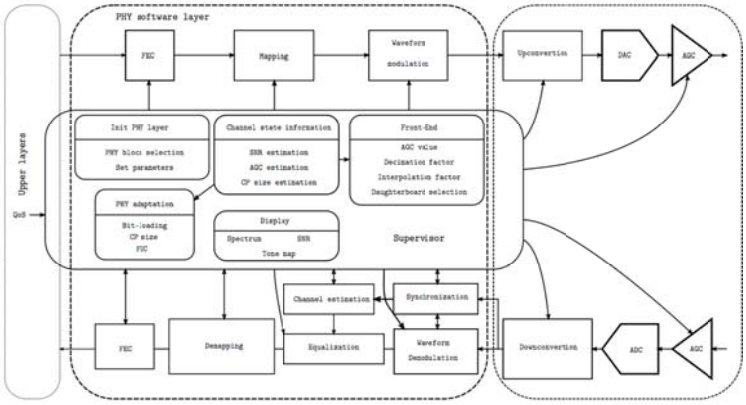

Figure 9. VPLC platform

V. CONCLUSION

We have studied a VPLC platform with USRP2 boards for PLC vehicle channels. Different experimental measurements show the entire possibilities offered by this kind of rapid prototyping. We performed PLC transmissions on real in-vehicle channels. In future work, the bandwidth could be extended and the software waveform generation will be enhanced in order to perform test in real time.

VI. REFERENCES

[1] J. Mitola, “The Software Radio Architecture,” *IEEE Communications Magazine,* vol. 33, n°5, May 95

[2] Michael Joseph Leferman. Rapid prototoyping interface for software defined radio experimentation. Master’s thesis, Worcester polytechnic institute, 2010.

[3] Praho, B.; Tlich, M.; Moulin, F.; Zeddam, A.; Nouvel, F.; , "PLC coupling effect on VDSL2," Power Line Communications and Its Applications (ISPLC), 2011 IEEE International Symposium on , vol., no., pp.317-322, 3-6 April 2011

[4] ITU http://www.itu.int/newsroom/press_releases/2009/46.html

[5] Home Grid Forum [Online]. Available : http://www.homegridforum.org/

[6] “Ettus research, llc.” [Online]. Available: http://www.ettus.com/

[7] “Gnuradio project.” [Online]. Available: http://gnuradio.org/

[8] A. Pinomaa, H. Baumgartner, J. Ahola, and A. Kosonen, “Utilization of software-defined radio in power line communication between motor and frequency converter,” in Power Line Communications and Its Applications (ISPLC),

2010 IEEE International Symposium on, march 2010, pp. 172 – 177.

[9] “Hd-plc standard”. [Online]. Available: http://www.hd-plc.org/

[10] P. Tanguy, F. Nouvel, and P. Maziéro, “Power line communication standards for in-vehicule networks,” in Intelligent Transport Systems Telecommunications,(ITST), 2009 9th International Conference on, 20-22 2009, pp. 533 –537.

[11] P. Tanguy, F. Nouvel , "In-Vehicle PLC Simulator based on Channel Measurements", in Intelligent Transport Systems Telecommunications ITST2010, 6 pages, 9-11 novembre 2010, Kyoto, Japon.

[12] Hlaing Minn, V.K Bhargava, "A robust timing and frequency synchronization for OFDM systems", IEEE Wireless Transactions on, vol. 2, no. 4, pp. 822 –839, july 2003.

[13] Hao Lin and P. Siohan. Capacity analysis for indoor plc using different multi-carrier modulation schemes. Power Delivery, IEEE Transactions on, 25(1) :113 –124, jan. 2010