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OQPSK COGNITIVE MODULATOR FULLY FPGA-IMPLEMENTED VIA DYNAMIC PARTIAL RECONFIGURATION AND RAPID PROTOTYPING TOOLS

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INTRODUCTION

- Requirements to be met by communication systems:
  - ➢ High data rate, heterogeneous communication standard compatibility, reliable communications, high battery life, small size, low price...
- Technological answer:
  - ➢ Software Defined Radios (Ability to change)
  - ➢ Cognitive Radios (Ability to sense)
  - ➢ Intelligent Radios (Ability to learn)

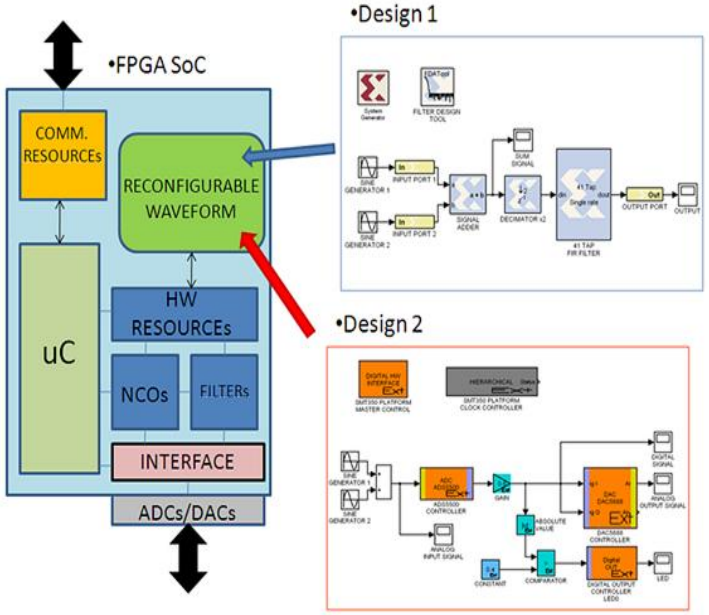
- SDR design environment:

Rapid prototyping tools

· Graphical programming, no code writing.

· Early functional simulations

·Easy debugging



- Communication system where a single piece of hardware has different functionalities in different times

Fit perfectly

FPGA partial reconfiguration (PR)

· Design flexibility

· Hardware reuse.

· Power save

Introduction (2 of 3)

- Proposed application
  - Cognitive Radios in wireless industrial communications
- Proposed implementation
  - OQPSK modulator (WirelessHART/IEEE802.11.4)
  - Channel sensing
  - Transmission in free channel

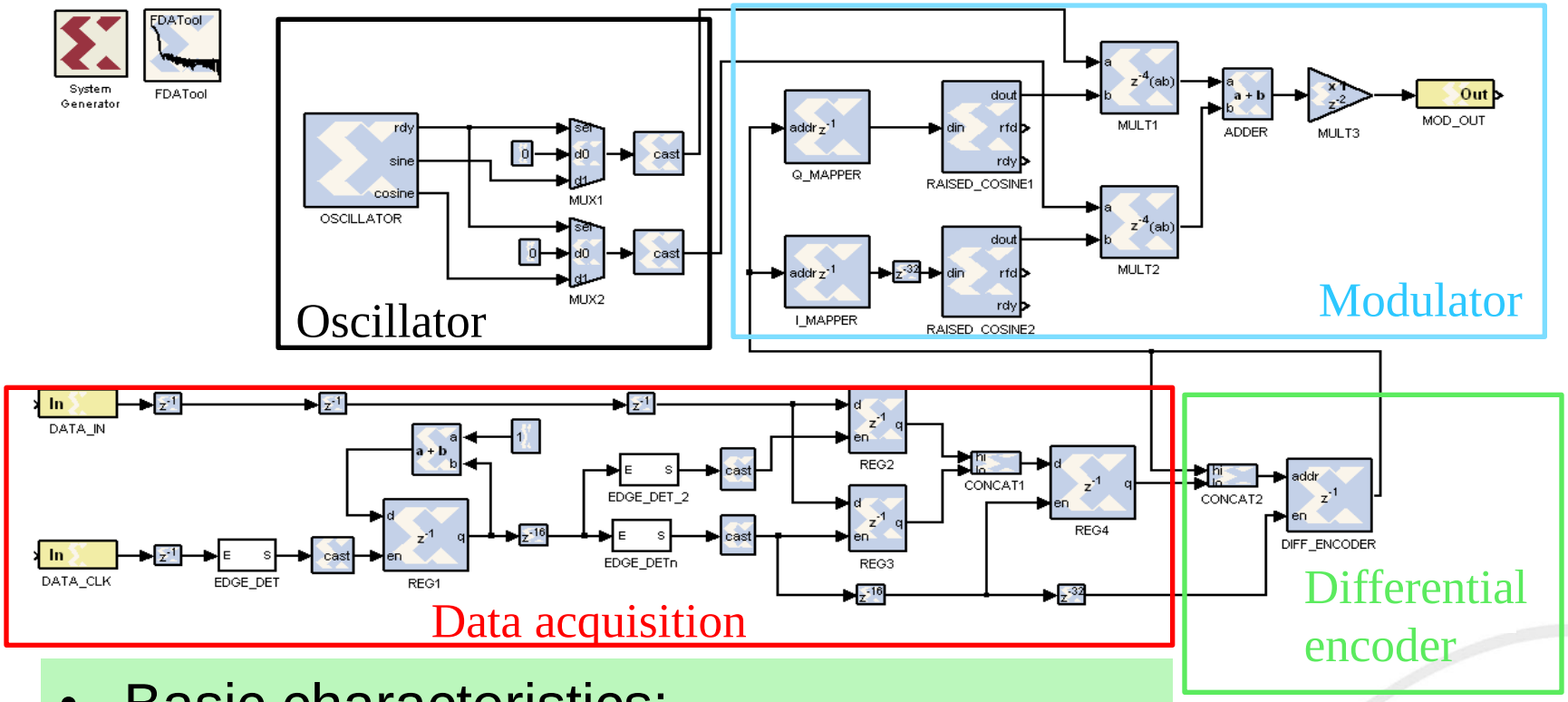
IMPLEMENTATION

- Two signal processing tasks
  - OQPSK modulator
  - Power Spectral Density estimator
- Chosen rapid prototyping tool
  - Xilinx's System Generator

XILINX SYSTEM GENERATOR™ For DSP

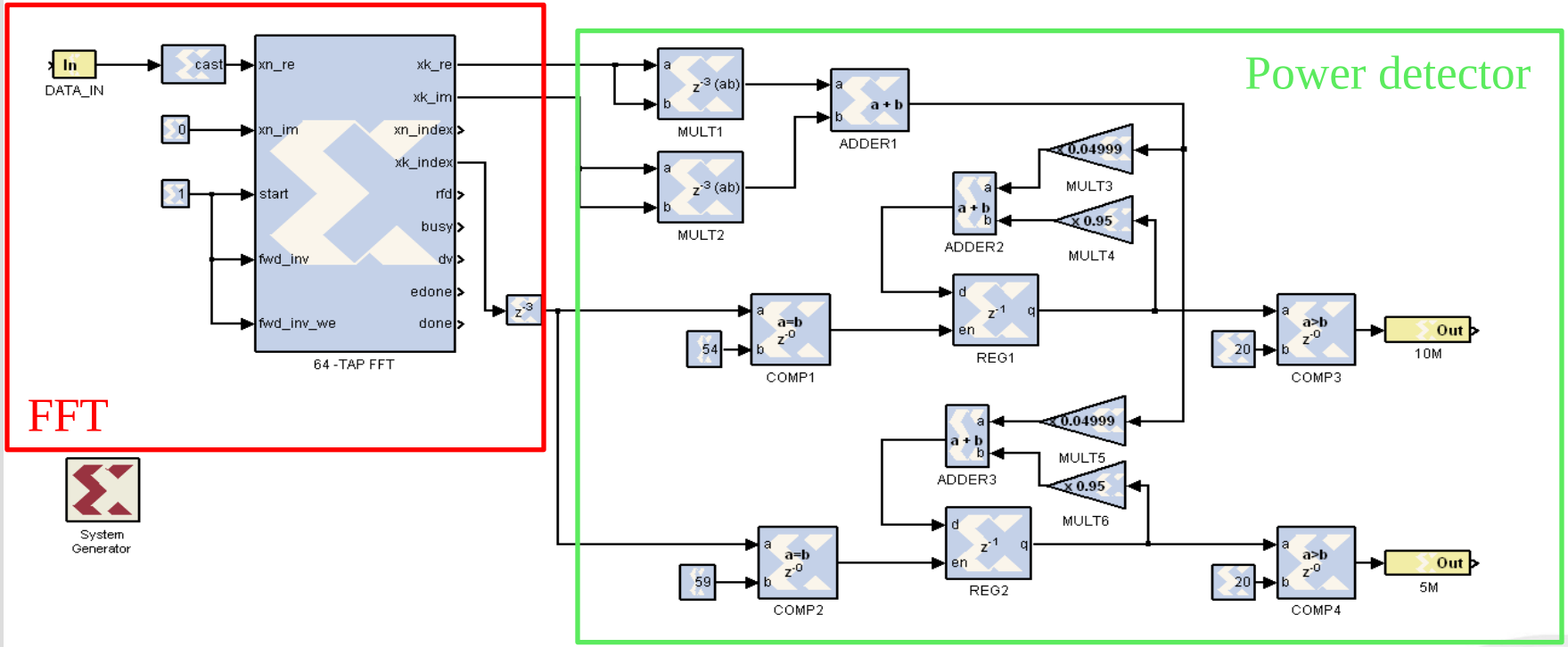
Implementation (1 of 7)

- OQPSK modulator implementation



- Basic characteristics:
  - 2 Mbps
  - FI: 5-10 MHz (PR implemented)
  - Output filter: 64 tap, 0.25 roll-off

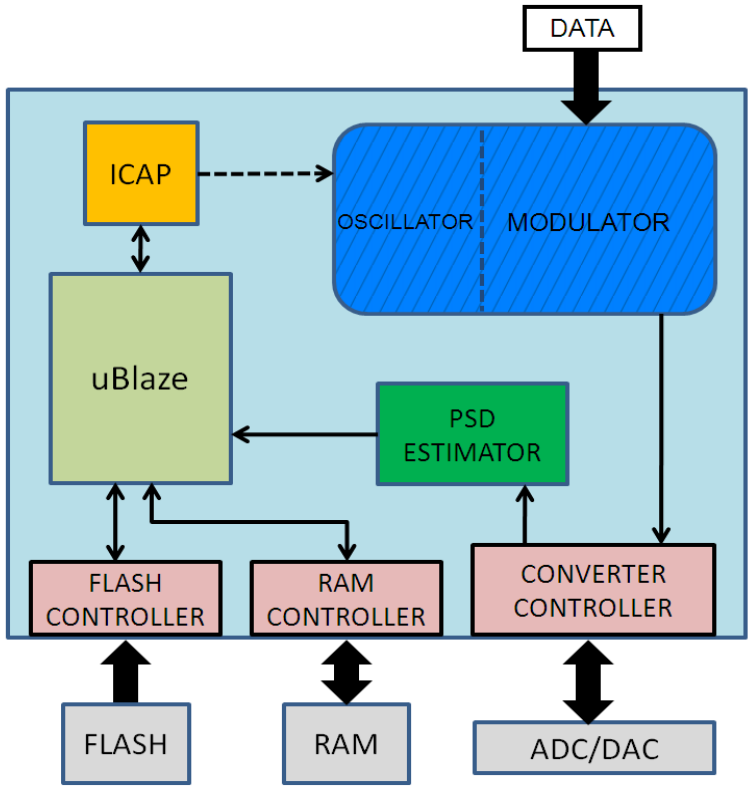
- PSD estimator implementation



- Basic characteristics:
  - FFT: 64 tap
  - Fs: 61.44 MHz
  - Resolution: 1 MHz

Implementation (3 of 7)

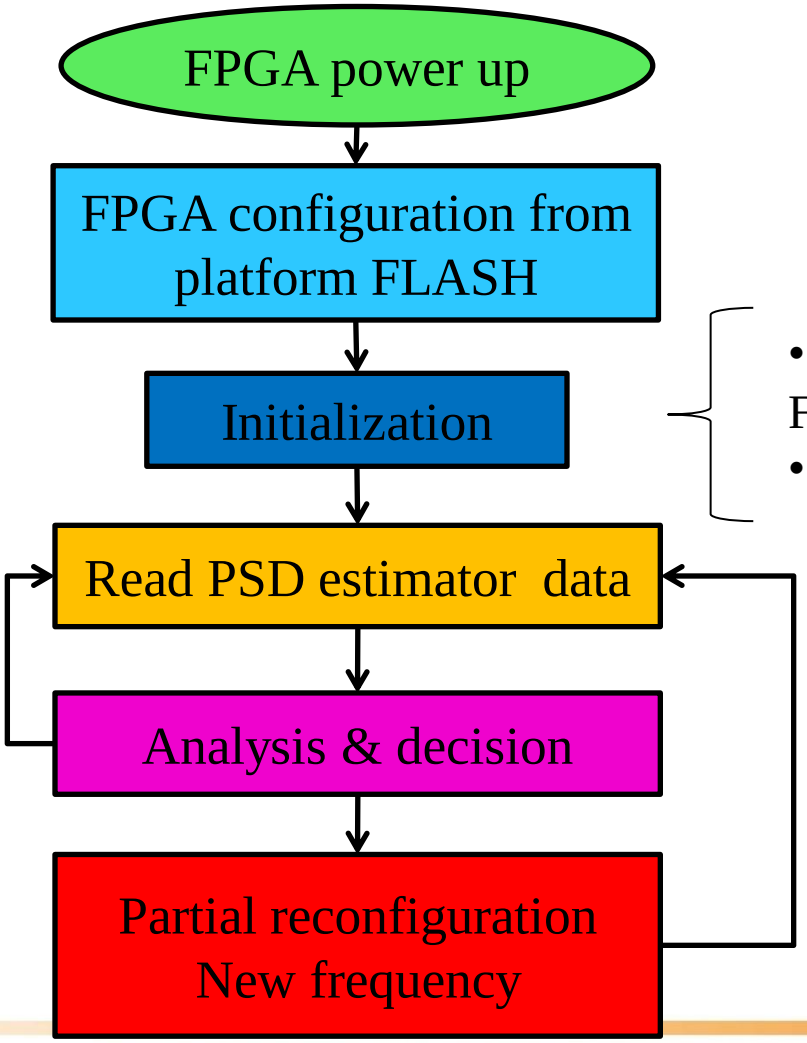
- PR architecture



- Basic characteristics:
  - PR controlled by uBlaze
  - VHDL coded memory and ADC/DAC controllers.
  - ICAP internal access port
  - 2 PR implementations

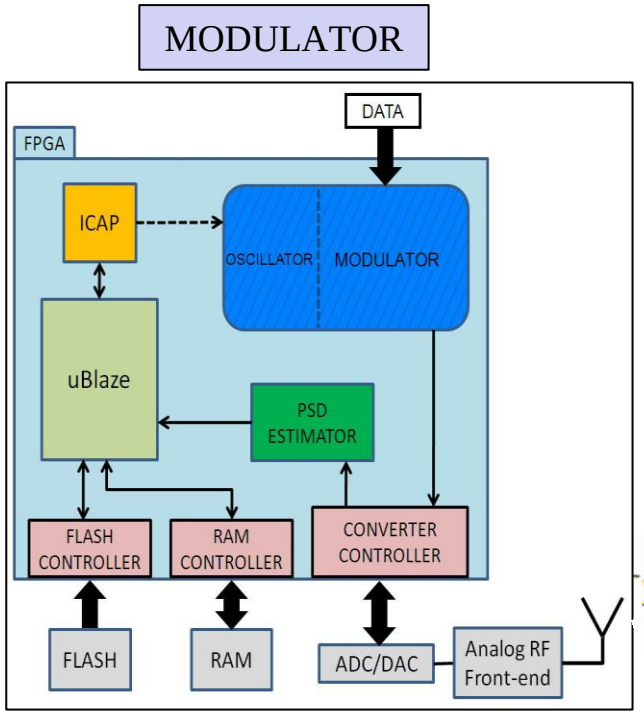
- FPGA partial reconfiguration and rapid prototyping tools
  - ➢ Not a standardized procedure
  - ➢ Possible but potentially dangerous
  - ➢ Necessary steps
    - ✓ Extraction of the non-reconfigurable FPGA resources (DCM, BUFG...)
    - ✓ Static and reconfigurable port concordance
    - ✓ Manage properly data exchanges

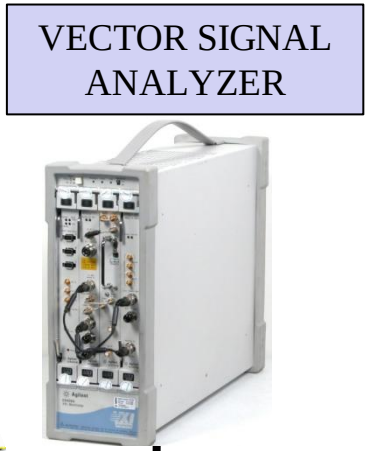
- Working Algorithm

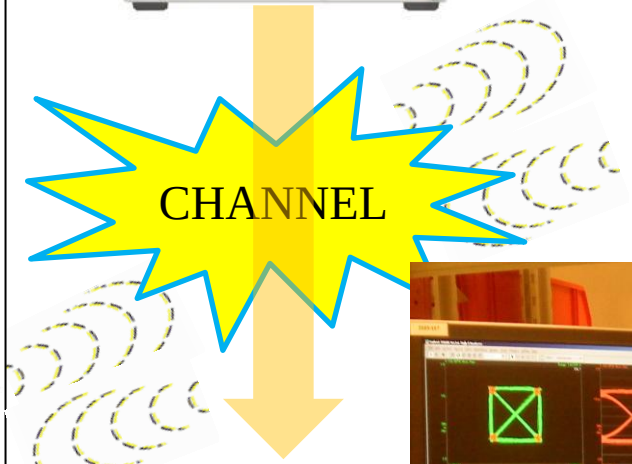


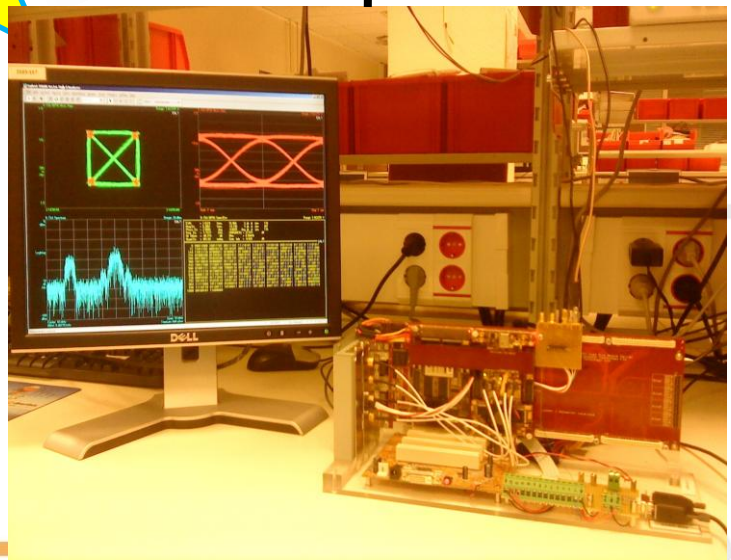
- Partial bitstream copy from FLASH to RAM/BRAM
- ICAP initialization

- Test framework









Implementation (7 of 7)

- Resource measurements

FPGA resource utilization										
	SLICES		FF		LUT		BRAM		Emb. Mults (DSP48)	
-	Available	Used	Available	Used	Available	Used	Available	Used	Available	Used
Modulator	15360	548 (4%)	30720	644 (2%)	30720	813 (3%)	192	3 (2%)	192	70 (36%)
Oscillator	15360	51 (<1%)	30720	61 (<1%)	30720	79 (<1%)	192	1 (<1%)	192	0 (0%)
PSD estimator	15360	1547 (10%)	30720	1955 (6%)	30720	2089 (7%)	192	3 (2%)	192	32 (17%)
ADC/DAC Controller	15360	169 (1%)	30720	181 (<1%)	30720	222 (<1%)	192	0 (0%)	192	0 (0%)
uBlaze system	15360	2905 (19%)	30720	2823 (9%)	30720	3718 (12%)	192	33 (17%)	192	3 (2%)
Full design	15360	5432 (35%)	30720	5679 (18%)	30720	6881 (22%)	192	40 (21%)	192	105 (55%)

- Small form factor (<35%)
- PSD estimator, main resource consumer (data processing) – 10%
- uBlaze system, main resource consumer (overall) – 19%

Measurements (1 of 2)

- Reconfiguration time measurements

Reconfiguration time			
	Partial bitstream size	Bitstream storage	
Reconfigurable area	-	RAM	BRAM
Whole modulator	267 KBytes	60 ms	-
Oscillator only	24 KBytes	4,5 ms	3 ms

- ICAP theoretical speed: 400 MBps
- Measured speed: 4.5 – 8 MBps
- Suboptimal ICAP implementation
- Theoretical reconfiguration times below the millisecond

CONCLUSIONS AND FUTURE WORK

- Conclusions
  - Simple application but valid as a proof-of-concept
  - Benefits: resource and power reduction, reliable communications and easy design
  - Main drawback: reconfiguration time and hand made operations

- Future work
  - Develop an optimized own ICAP
  - Develop a design methodology- reconfigurable function analysis
  - Framework appliance to a multi-standard modulator

QUESTIONS