SAMPLE CLOCK OFFSET DETECTION AND CORRECTION IN THE LTE DOWNLINK RECEIVER

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ABSTRACT

The narrow subcarrier spacing and wide bandwidth arrangement in the LTE downlink produce a vulnerability to sample clock mismatch between the transmitting and receiving data converters. Without two high precision clocks, a high level of inter-carrier interference (ICI) is introduced, yielding undesirable performance. In this paper, a method to jointly estimate and correct sampling frequency mismatch and FFT window timing is proposed. The proposed method operates strictly in the time domain and does not require the aid of pilot symbols or other frequency domain information. The method allows clocks with lower precision to be used with minimal performance degradation. Results are presented using MATLAB simulation as well as an FPGA hardware implementation.

1. INTRODUCTION

Orthogonal frequency division multiplexing (OFDM) has been chosen as the air interface for LTE, the next generation cellular standard. In any OFDM system, as the subcarrier spacing is reduced and the number of subcarriers is increased, small amounts of Sample Clock Offset (SCO) result in high inter-carrier interference (ICI), severely degrading the effective signal-to-noise ratio (SNR) at the outer subcarrier positions. The 3GPP Long Term Evolution (LTE) standard supports up to 1,200 subcarriers, with a subcarrier spacing of only 15 kHz. In this configuration, modest amounts of sample clock offset produce severe SNR degradation in the outer subcarriers.

When SCO is present, each ideal symbol and the measured actual symbol differ in length by some fractional amount. If the receiver clock is faster (slower) than the transmitter clock, then a fractional additional (missing) symbol is measured. Over time, any accumulated positive (negative) fractional samples sum to an integer sample and the integer FFT timing window offset is shifted later (earlier). Over time, direction and rate of motion of the FFT window position directly reflects the magnitude and sign of the present SCO. If the receiver simply shifts the FFT window by integer sample offsets, the time-domain signal contained in each window position contains fractional samples, resulting in ICI and degraded SNR. In order to eliminate ICI caused by SCO, the signal must first be resampled so that each FFT window contains exactly the correct integer number of samples.

To determine the resampling rate, the receiver must estimate the amount of SCO present. The rate and direction of FFT window drift indicate the appropriate resampling ratio that will eliminate the excess fractional samples from each FFT window duration. If the resampling ratio is determined correctly, the FFT window position will remain stationary as if no SCO was present. The resulting signal will now be free of SCO-related ICI and SNR degradation.

Here, each FFT timing window position is estimated using a Maximum-Likelihood (ML) algorithm [1] without the modifications performed in [2]. This estimator relies on the correlation of each symbol and its cyclic prefix (CP), as well as knowledge of the SNR. To control the resampling process, each estimate will be used in a closed-loop control system, using each window position estimate to adjust the resampling ratio until the estimated FFT window position remains constant over each symbol.

Further discussion will begin with the introduction of a general OFDM system model, followed by a discussion about the effects of SCO in an OFDM system. Next, a time-domain method to measure SCO will be introduced, followed by a method that corrects SCO by resampling the affected signal. Finally, a full receiver architecture will be proposed, followed by MATLAB and FPGA hardware test results.

2. SYSTEM MODEL

Consider an OFDM system where N_{CP} indicates the number of samples included in each cyclic prefix and N_{FFT} indicates the FFT size, as well as the number of samples in each symbol duration. The total number of samples for each symbol duration $P = N_{CP} + N_{FFT}$. In the LTE standard, the extended cyclic prefix length is $N_{CP} = N_{FFT}/4$ [3]. Here, it will be assumed that $N_{FFT} = 2048$. In this configuration, the sample rate of the system is 30.72 MHz,

making each ideal sample duration $T_s = 1/(30.72\times10^6)$ seconds. Each ideal symbol duration is $PT_s \cong 83.33\,\mu s$.

In this LTE configuration, each OFDM symbol is modulated at the transmitter from the frequency domain to the time domain according to

$$y = F^H Y, \tag{1}$$

where F is the $N_{FFT}\times N_{FFT}$ DFT matrix defined by

$$F = \begin{bmatrix} W_{N_{FFT}}^{00} & \cdots & W_{N_{FFT}}^{0(N_{FFT}-1)} \\ \vdots & \ddots & \vdots \\ W_{N_{FFT}}^{(N_{FFT}-1)0} & \cdots & W_{N_{FFT}}^{(N_{FFT}-1)(N_{FFT}-1)} \end{bmatrix}, \tag{2}$$

where

$$W_{N_{FFT}}^{nk} = \frac{1}{\sqrt{N_{FFT}}} e^{-j2\pi\frac{nk}{N_{FFT}}}. \tag{3}$$

Here, the DFT matrix F is the orthonormal DFT matrix, where $F^H F = I$. The vector Y is of size $N_{FFT}\times1$ and contains 1,200 complex QAM symbols occupying the DFT bin indices given by $l \in \{2,3,...601,1449,1450,...,2048\}$. Any indices $\notin l$ contain zeros, such that no power is transmitted [3]. Finally, the vector y is cyclically extended to length $P\times1$ by prepending the samples $[y[N_{FFT}-N_{CP}+1], y[N_{FFT}-N_{CP}],\ldots, y[N_{FFT}]]^T$ onto the existing y vector.

The y vector is transmitted through an AWGN channel to the receiver. The receiver estimates the appropriate FFT window, which ideally contains the y vector with additive noise. After FFT window synchronization, the vector $x[n]$ contains the following signal. $x[n] = [y[N_{CP}+1], y[N_{CP}+2],\ldots, y[N_{FFT}]]^T + w(n)$, where $1 \le n \le N_{FFT}$. The receiver then performs OFDM demodulation by multiplying x with the DFT matrix.

$$X = Fx \tag{4}$$

Here, the receiver transforms the time-domain x vector of size $N_{FFT}\times1$ into the frequency domain vector X. The receiver then discards the unoccupied subcarrier indices leaving only $X[n], n \in l$. The resulting X is of size $1{,}200\times1$.

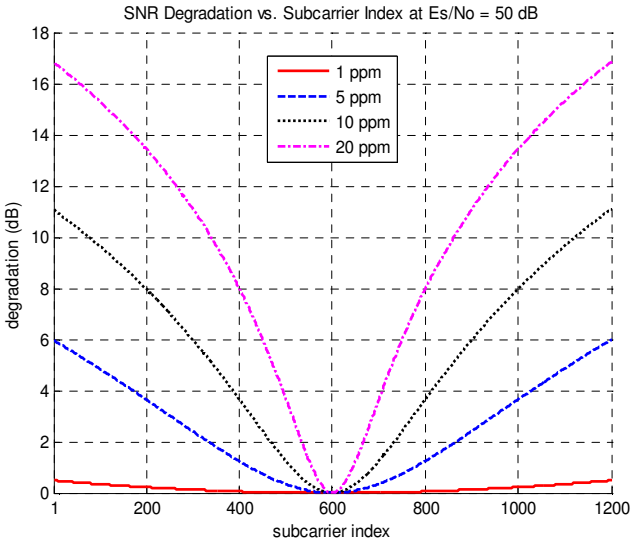

Figure 1: SNR Degradation vs. Subcarrier Index

3. EFFECTS OF SCO IN AN OFDM SYSTEM

In LTE or any other communications system, any reduction in SNR increases the likelihood of bit-errors at the receiver. In an OFDM system, SCO causes loss of orthogonality, which introduces ICI. Energy leakages from ICI are distributed among the subcarrier bins and cause interference. If each constellation symbol is equally probable at every subcarrier location, the leaked energy appears as additive uncorrelated noise. Because the leaked energy is uncorrelated with each subcarrier, it can be modeled as SNR degradation, where the noise energy term includes leaked energy and AWGN from the channel.

The effect of SNR degradation caused by SCO has been studied in [4]. From [4], the degradation of SNR in dB on the received vector X for each nth subcarrier index is defined by

$$D_n \approx 10\log_{10}\left(1+\frac{1}{3}\frac{E_s}{N_o}\left(\pi n 10^{-6}\Delta f_s\right)^2\right), \tag{5}$$

where Δf_s is the sample clock mismatch observed at the receiver in parts-per-million (ppm), and E_s and N_o are the received symbol energy and noise energy, respectively.

Figure 1 shows that for high E_s/N_o, signal quality is adversely affected by even small amounts of sample clock offset. For user equipment (UE) to provide acceptable performance, the sampling clocks must have a very low frequency offset tolerance, which increases cost. Note that in Figure 1 and 2, the observed SCO at the receiver is double (worst-case) the sample clock tolerance of each individual sample clock source. If a transmitter and receiver clock both have ±20 ppm error tolerances, the worst-case

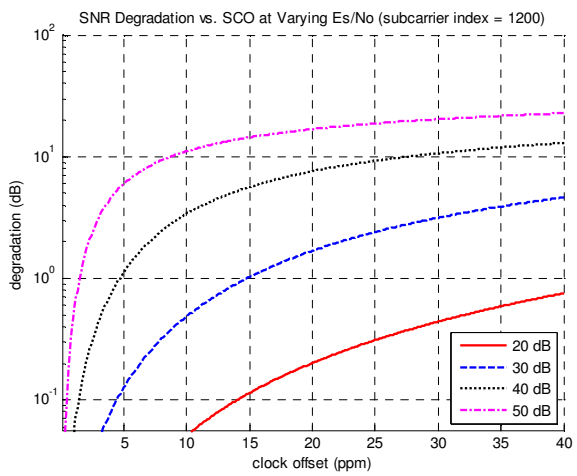

Figure 2: SNR Degradation vs. SCO vs. Es/No

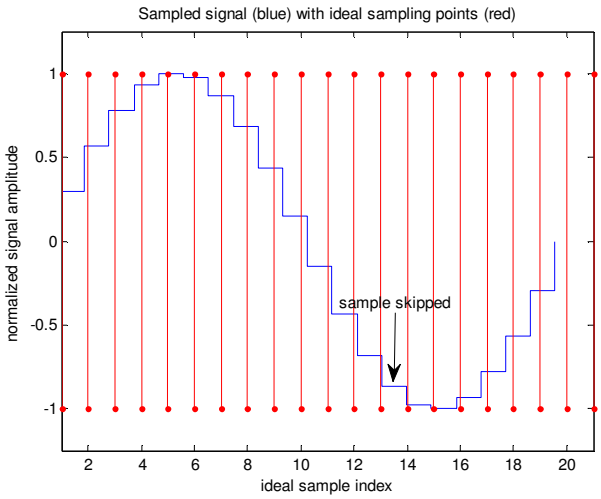

Figure 3: Received Signal Overlaid With Ideal Sample Positions

clock error observed at the receiver will be 40 ppm. It is assumed however, that the LTE downlink transmitter (eNodeB) will have a high-quality clock source to be approximated as 0 ppm.

Figure 2 illustrates the worst-case SNR degradation (at subcarrier position 1 or 1200) for various values of E_s/N_o and SCO. The lower SNR signals are less affected, but they still incur degradation values on the order of .1-1 dB for sample clock errors above 14 ppm with $E_s/N_o = 20\,\text{dB}$.

4. SCO MEASUREMENT

When SCO is present at the receiver, additional samples are added or subtracted to the nominal sample count in any fixed time interval. A +100 (-100) Hz offset, will produce 100 additional (fewer) samples in each second. In an LTE system using the described system model, a +100 Hz offset will add $8.3\text{x}10^{-3}$ samples to each symbol duration. One additional full sample will be accumulated after 120 symbols. Over time, SCO will cause the FFT window to continue to drift at this rate.

Any OFDM system must synchronize its FFT window with the incoming symbol timing. Here, the algorithm presented in [1] is used to provide ML timing window estimates. Each window position ranges between 1 and P, representing P offset. Over time, SCO causes the modulus timing offset to drift. From this drift, the receiver can determine the resampling rate required to correct the SCO.

5. SCO CORRECTION BY RESAMPLING

To correct SCO, an additional fractional number of samples must be added or removed to each symbol duration so that every symbol period contains the nominal number of samples. After the signal has been resampled at the correct rate, the FFT window will remain stationary and ICI caused by SCO will be eliminated. After resampling, each OFDM symbol will contain P samples.

Here, resampling will be performed by the modulation of a fractional delay filter. An ideal fractional delay filter is capable of producing delays of any continuous value. If the fractional delay value of the filter is continuously varied, the signal will be resampled at a rate controlled by the variation. Consider the example in section 4, where the receiver experiences an SCO of +100 Hz. If the signal is passed through a fractional delay filter where the delay is continuously reduced by $8.3\times10^{-3}/P = 3.2442\times10^{-6}$ samples, the additional fractional samples will be removed from each OFDM symbol, and the SCO will be corrected.

In a practical system, the ideal fractional delay filter does not exist. The available delay values are finite in precision and are upper-bounded. For reasons of practicality, we will consider a fractional delay filter capable of producing delay values between 0 and 1. As the delay is continuously increased or decreased, the delay will eventually exceed one of these bounds, requiring additional delay correction of one integral sample by components outside the fractional delay filter.

If the sample clock at the receiver is too fast, the fractional delay must be continuously incremented to correct the additional positive samples that are added by the offset. Upon overflow of the fractional delay, the filter must process a delay of approximately 1, followed by a positive delay of approximately zero. This process is shown in Figure 3. For this case, a component after the filter must discard the sample, so that it is not included in the output sequence. This process effectively removes the extra samples caused by the SCO. Conversely, in the case where the sample clock at the receiver is too slow, to correct the clock error, the receiver must continuously decrement

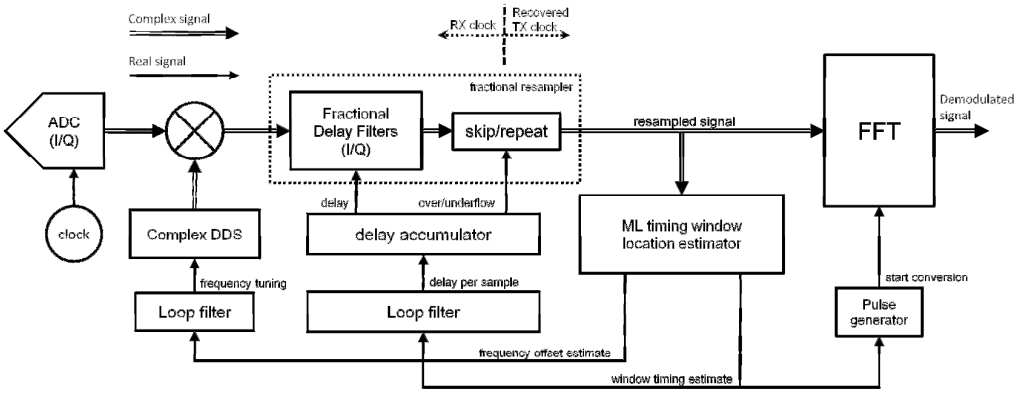

Figure 4: Proposed OFDM receiver architecture

the fractional delay, which causing an underflow of the delay value. Upon underflow, the receiver is requested to process the same sample at a positive delay of approximately zero, and a delay less than, but approximately 1. Ideally, the fractional delay filter must process the same filter state (samples stored in the memory of the filter are held in place) for two separate fractional delay values. Some simplifying alternatives exist. The filter could simply repeat the output of the small fractional delay value for the second sample, or it could produce an output with a delay value of zero. By repeating the sample or bypassing the filter for the second sample, a small error occurs. The error is negligible for small SCO mismatches and saves the complexity of controlling the filter state reprocessing.

In each case, if the fractional delay is correctly varied and the overflow (underflow) symbols are discarded (repeated), each symbol will contain the ideal number of samples per symbol duration. If SCO is not properly compensated and the FFT window drifts, then the variation rate of the fractional delay must be adjusted so that the timing window drift is cancelled.

6. PROPOSED RECEIVER ARCHITECHTURE

The proposed receiver architecture shown in Figure 4, includes both timing and frequency offset correction. Here, the information produced by the ML estimator [1] is used to correct window timing, sample clock offset and frequency offset, completing the necessary synchronization requirements for OFDM reception in a mobile wireless receiver (asynchronous operation between transmitter and receiver).

In figure 4, the fractional delay filters (one for I and Q, each), combined with the skip/repeat component complete the fractional resampler. Here, each window timing estimate, given once per symbol duration, is used by the loop filter to determine the amount of observed delay-change per unit sample from SCO. The loop filter has enough memory to consider many timing window estimates, so that SCO can be more accurately measured. The loop filter produces a control signal that indicates the estimated SCO in units of fractional delay per sample. The loop filter output is accumulated at the sampling rate to modulate the fractional delay filter, updating the delay value for every input sample. When the delay accumulator underflows (overflows), a sample is repeated (skipped) by the skip/repeat component. The resampled signal passes into the ML timing estimator component so that the new timing window can be determined, thus completing a feedback-control loop that continuously adjusts the system to a zero steady-state SCO without modifying the ADC clock. The resampled signal also passes directly into the FFT component, where OFDM demodulation occurs. In figure 4, the pulse generator block issues a one-cycle pulse that indicates the beginning of each FFT window. The cyclic prefix is effectively removed by generating the pulse on the trailing edge of the estimated CP boundary of each symbol.

One advantage of this architecture is that it does not constrain the receiver to use any particular timing window estimation algorithm. If an FFT window timing estimator does not produce a new estimate for every symbol, the only necessary modifications are to the loop filter component. To properly resample the incoming signal, the loop filter must always provide the observed timing window drift in units of fractional delay per sample to the delay accumulator. For instance, in an LTE system, the designer can gather timing information from primary synchronization signal correlation, which is provided every 5 ms, and still make use of the proposed resampling architecture.

7. RESULTS

Performance tests of the proposed receiver architecture are carried out for both MATLAB and in FPGA hardware implementations. For testing, LTE signals impaired by SCO and AWGN are generated in MATLAB. For hardware tests, to better simulate real-world conditions, the sample clocks

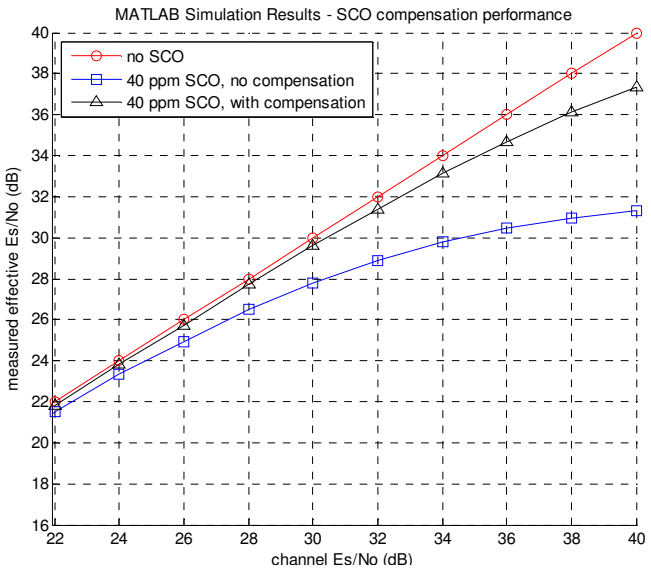

Figure 5: MATLAB SCO compensation performance

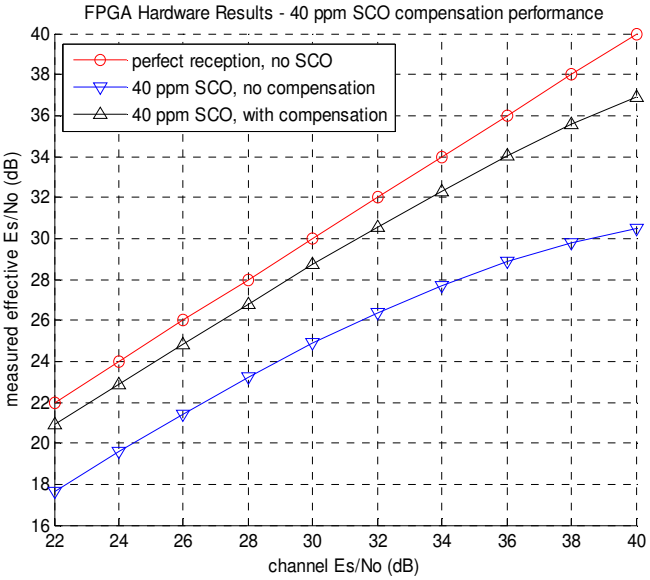

Figure 6: FPGA Hardware Test: 40 ppm SCO compensation performance

from the transmitter and receiver are separated and only AWGN impairments are applied.

7.1. MATLAB Implementation Testing

The first test, shown in figure 5, compares a signal impaired with varying levels of AWGN with the same signal corrupted by a 40 ppm SCO. The 40 ppm error is observed at the receiver after the ADC, simulating worst case for transmitter and receiver clocks with ±20 ppm error tolerances. The measured SNR in figure 5 is averaged over all subcarrier positions for each symbol. Note that figure 1 shows the SNR degradation for each subcarrier position, and figure 2 shows the worst-case degradation for varying levels of SCO. In this test, the signals impaired by SCO are phase-corrected, so that only the leaked energy from ICI is present, which reduces the effective SNR. The MATLAB implementation first measures the SCO based on the timing window motion, then performs correction using a fractional delay filter. The response of the fractional delay filter is not ideal. The filter itself adds some non-ideal magnitude and phase distortion, which contribute to the SNR loss. A finite amount of error also exists in the SCO measurement. This test considers 120 estimates taken from one LTE frame in the extended cyclic prefix mode. To estimate the SCO, the window motion is averaged over all estimates in the frame.

Figure 5 clearly shows that the proposed SCO compensation method provides better improvement in SNR at higher levels of Es/No. The resulting benefit will be a reduction in bit-errors, particularly for higher order constellations such as 64-QAM.

7.2. FPGA Implementation Testing

FPGA hardware tests were carried out using X5-TX and X5-400M FPGA boards from Innovative Integration, Inc. The X5-TX is used to continuously output MATLAB-generated, baseband time-domain LTE signals, simulating the constant transmission of the eNodeB. The proposed receiver architecture has been implemented in the X5-400M FPGA board. The receiver processes the received signals in real-time and stores the FFT result to the hard-disk on the host computer. The signal is then analyzed in MATLAB. The two offset clock sources are produced by Agilent E4433B signal generators. The two clock frequencies are separated and measured to test both 40 and 100 ppm error conditions (observed at the receiver). A Bessel reconstruction filter is applied to the baseband signal generated by the X5-TX to eliminate spectral copies produced by the DAC. The base-band signal is upsampled by a factor of 8 so that all spectral copies are adequately attenuated by the reconstruction filter. Two receiver designs are used for each test. In one receiver, the SCO correction components have been included, allowing the receiver to measure SCO and resample the incoming signal accordingly. The other receiver is not equipped with any SCO correction. The receiver without SCO correction tracks the FFT window as it drifts, but it does not perform resampling. This test provides a comparison between a receiver with and without SCO correction.

The results of the 40 ppm SCO test are shown in Figure 6. The receiver with SCO correction provides a minimum of 2.4 dB better SNR performance than the non-correcting

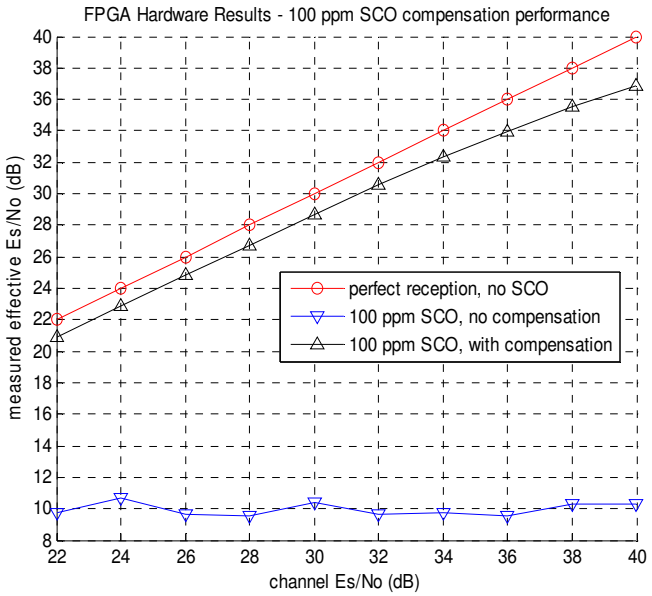

Figure 7: FPGA Hardware Test: 100 ppm SCO compensation performance

receiver design. Unlike the MATLAB simulation, the performance gain extends to the lower SNR values. This test shows that a transmitter and receiver equipped with low-cost ±20 ppm sample clock sources can greatly benefit from the proposed SCO correction technique.

The results of the 100 ppm SCO test are shown in Figure 7. This test illustrates even high SCO levels can be corrected with little SNR degradation. Because of the high SCO, the receiver without SCO correction is not able to maintain reliable synchronization, and it fails even when the received signal has a high SNR. Under the same conditions, the proposed SCO compensation algorithm tracks the clock offset and resamples the signal well enough to allow reliable timing estimation. The resulting SNR from the 100 ppm test are only fractions of a dB lower than the SNR resulting from the 40 ppm test. When using the proposed SCO compensation, the designer can use lower tolerance clocks to save cost, while maintaining a high level of performance. This test illustrates that, when using the proposed SCO compensation method, successful reception can still take place even when the transmitter and receiver are equipped with ±50 ppm clock sources.

8. CONCLUSIONS

The proposed method for sample clock offset correction is shown to provide a significant improvement in SNR in receivers using less precise sample clocks. For the downlink receiver in the LTE user equipment, cost can be greatly reduced by relaxing the sample clock tolerance restriction. The proposed method is compatible with any OFDM system, as it does not rely on any particular time or frequency domain signal characteristics. The designer has the freedom to choose any specific timing synchronization algorithm with little necessary modification to the proposed architecture.

9. ACKNOWLEGEMENTS

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