PORTING OF AN FPGA BASED HIGH DATA RATE DVB-S2 MODULATOR

Chayil Timmerman (MIT Lincoln Laboratory, Lexington MA, USA); Ivan Corretjer (Naval Research Laboratory, Washington DC, USA); John Glancy (Naval Research Laboratory, Washington DC, USA); Michael Rupar (Naval Research Laboratory, Washington DC, USA); Andrew Miller (MIT Lincoln Laboratory, Lexington MA, USA)

ABSTRACT

This paper covers a high data rate (HDR) DVB-S2 (Digital Video Broadcasting – Second Generation Satellite) modulator implementation that was designed to allow for rapid porting across a multitude of different software defined radio (SDR) platforms and scale accordingly to each platforms capabilities and limitations[1]. The Naval Research Laboratory's (NRL) basic digital radio - one (BDR-1) SDR platform was chosen as a good candidate SDR platform to demonstrate the portability and scalability of the modulator implementation. The BDR-1 provided a significantly smaller form factor than the platform originally used to develop the HDR DVB-S2 modulator. It already had successfully demonstrated an NRL develop HDR waveform implementation, introduced in previous papers, which made it an ideal candidate. This paper will discuss the coding and architectural techniques used in order to increase the portability and scalability of the waveform; the steps taken to port the waveform to the BDR-1; and the end results.

1. INTRODUCTION

One of the foundations of the SDR methodology is to reduce the cost of fielding the same waveform onto multiple different platforms. A number of different approaches have been identified to aid the developers in this endeavor. These approaches range in complexity and have not necessarily been shown to reduce the cost and complexity of porting. In this paper the authors will discuss the porting of an independently developed waveform, which capitalizes on a commercial standard, to an independently developed platform with a pre-existing waveform already in residence. It will be shown, through the application of commonsense procedures and by leveraging pre-existing investments by
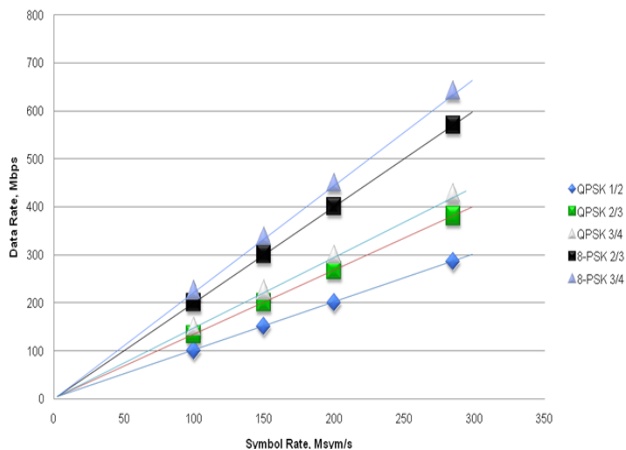
Figure 1 HDR DVB-S2 Waveform Data Rates

industry, that the porting costs can in fact be lowered while increasing interoperability.

2. HDR DVB-S2 WAVEFORM

DVB-S2 is a next generation satellite communications standard that was originally intended for the broadcast satellite market. The physical layer is detailed in the ETSI EN 302 307 V 1.1.2 (2006-06) standard. The waveform has seen broad adoption and deployment in both commercial and military communications. Its popularity stems from its versatility of modes and near Shannon limit forward error correction (FEC) codes.   The standard supports the following modulation types:

- QPSK
- 8PSK
- 16APSK
- 32APSK

The standard also supports FEC code rates ranging from 1/4 to 9/10. It is a packet based waveform that supports data types ranging from MPEG 2 video to IP traffic, and it also has provisions for non-packetized streaming data.[1]

The HDR DVB-S2 waveform implementation, discussed in this paper, is a standards-compliant implementation of DVB-S2. However, it does not support all the modes and framing structures outlined in the standard.   The
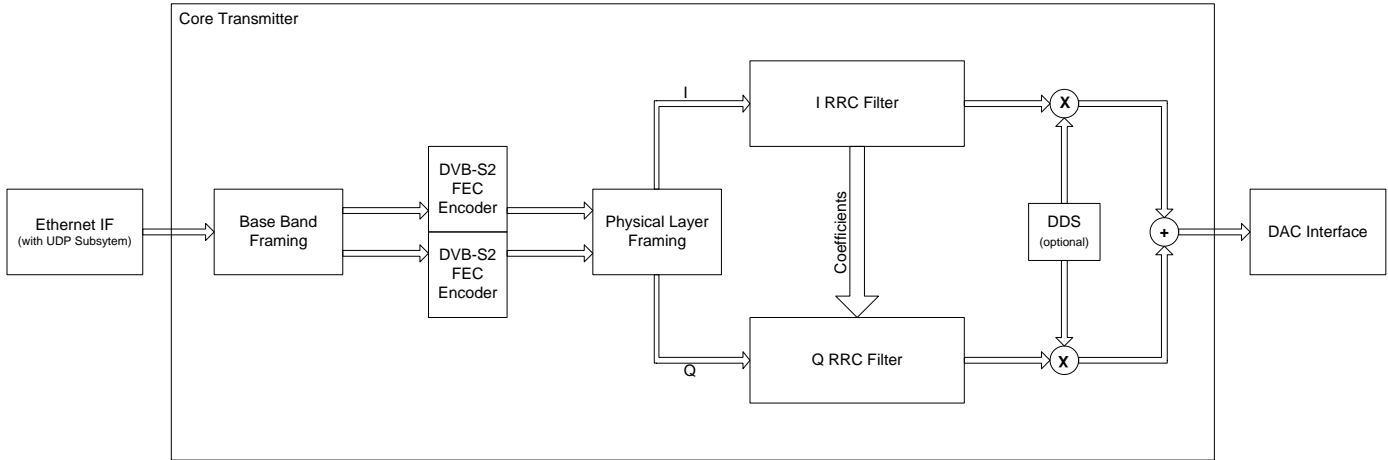
Figure 2 Core Modulator Design

implementation supports the QPSK and 8PSK modulation types and all of the FEC rates, which allows for a large variety of operating points. What differentiates the HDR implementation from other commercially available options is the ability to support symbol rates from 1 to 285 Msym/s; typical commercial implementations only support rates from 1 to approximately 50 Msym/s. Figure 1 shows a sampling of the data rates that are possible with the HDR implementation.

The HDR DVB-S2 implementation was intended to be transferable to multiple platforms and technologies, and as such SDR best practices were employed to ensure maximum portability and scalability. The VHDL and software were partitioned such that all time critical signal processing was handled by the FPGA. It was hoped that this partitioning strategy would simplify the software design and remove all real-time requirements from the host processor. [2]

2.1 The VHDL Design

The HDR DVB-S2 VHDL design was partitioned into small manageable waveform-specific modules and FPGA-specific modules. The intention was to create a core set of modules that implements the waveform functionality without using technology specific functions. The core was then encapsulated by the FPGA specific functions. These functions include clock management, external I/O, host interface, etc. Figure 2 details the HDR DVB-S2 modulator. The portion of the design located within the *Core Transmitter* box represents the waveform-specific modules. The HDR DVB-S2 VHDL design was initially developed on a Virtex 5 SX95T FPGA, but was subsequently ported to a SX240T.

The DVB-S2 FEC encoder used in this implementation is a commercially-acquired core. The HDR DVB-S2 design supports two different vendors' encoders; one from Comtech AHA, which is a technology independent implementation, and one from Xilinx, which is specific to Xilinx FPGAs. The design is not limited to these two vendors. The design documentation provides the necessary information for integrating a different implementation of the encoder.

The modulator implementation supports two types of digital to analog conversion (DAC) schemes. In the first option the RRC filter outputs are passed directly to two DACs in support of an analog I/Q modulator. The second option digitally mixes up the I/Q samples to an intermediate frequency (IF) and passes them to a direct conversion DAC. The *DDS* module, shown in Figure 2, performs the digital mixing to a user defined IF.

Supporting the VHDL design is an extensive set of documentation focusing on two primary areas of interest to future porters: 1.) VHDL module to VHDL module interfaces; 2.) VHDL module to SW interfaces. By providing the module to module interfaces, the porter can determine how to partition the modules across the platforms FPGA(s). It is the opinion of the authors that maintaining a common interface across all modules increases the readability and portability of the design. However, simplicity should not be sacrificed in the name of commonality. Often "standardized" interfaces only increase the complexity without increasing the readability or portability.

The VHDL module to SW interface documentation lists all communication interactions between the hardware and software. It also details the intended order of operation of the software.

2.2 The Software Design

The HDR DVB-S2 software design configures the VHDL design prior to operation; as such the software design does not have a real-time requirement. The design is not SCA-compliant, but it does follow the intent of the SCA. The design is segmented in a series of layers which allows for the rapid porting from one platform to another.

Figure 4 details the different software layers. The user application relies on the WaCoM library which in turn relies on the user-supplied platform-specific driver implementation. The WaCoM Library is a C++ library that abstracts and encapsulates the software/hardware interface. By supplying the WaCoM library, the porting programmer is not required to understand the modulator internals. The driver layer can communicate directly or indirectly with the hardware through additional software, or through operating system layers.

3 THE BDR-1

The Basic Digital Radio (BDR-1) is a small form factor software programmable radio developed for NRL by Fred Harris & Associates shown in Figure 3. The BDR-1 contains: two Xilinx Virtex 5 SX50T FPGAs; a Maxim 19692 DAC; a Maxim Max 108 analog to digital convertor (ADC); and two low-jitter ADF4360 based VCOs. The board also provides fiber and Gigabit Ethernet connectivity to each FPGA. One FPGA is intended to support the required modulation functions while the other FPGA is devoted to the demodulator. The IF input and output signals are filtered with a band pass filter and power control is achieved using a variable gain attenuator/amplifier, controlled by the FPGAs. Figure 5 details the BDR-1 architecture. [3]

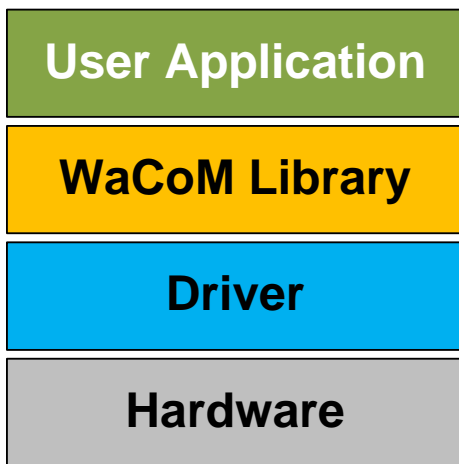The BDR-1 board support package contains a sample

waveform to assist in the porting process. The FPGA

Figure 3 BDR 1

design for both the modulator and demodulator are written in VHDL. The software command and control of the waveform is achieved through the GigE port via MATLAB scripts.

An important aspect of this design is the low-jitter clocking architecture employed for the high-speed ADC and DAC in order to reduce aperture uncertainty and maintain good SNR. The BDR-1 uses a direct digital conversion ADC and DAC scheme. The sample clock of the DAC is provided from the ADF4360 VCO at a rate of 1.75 GHz. There is some tuneability built into the VCO, but the band pass filter is optimized for a sample rate of 1.75 GHz. For different sample clock rates different ADF4360-X VCOs can be substituted. [4]

4 THE HDR DVB-S2 PORT TO THE BDR-1

The following sections discuss the hardware and software porting process used to port the HDR DVB-S2 modulator to the BDR-1.

4.1 The Hardware Port

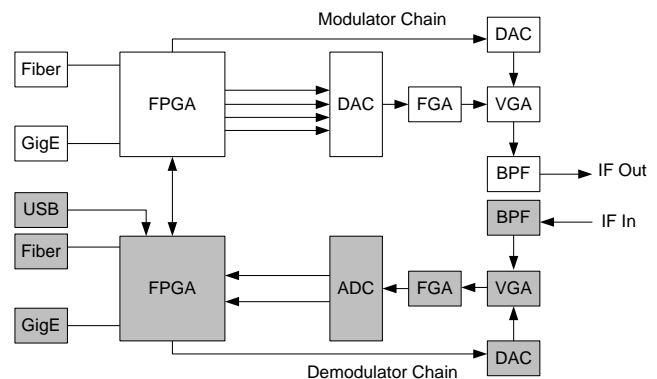The first step of the porting process was to identify the HDR

Figure 4 HDR DVB-S2 Software Layers
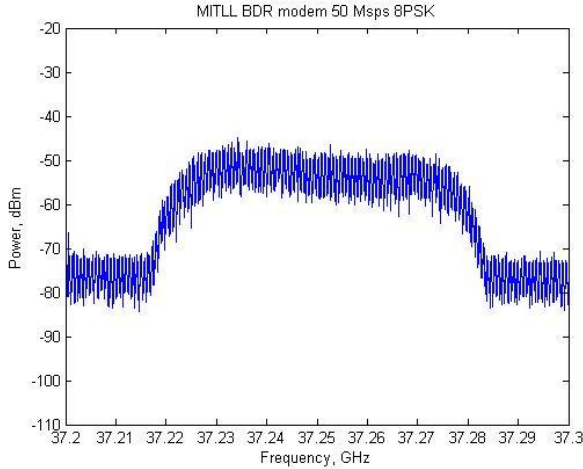

Figure 5 BDR-1 Architecture

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Figure 6 HDR DVB-S2 50 Msym/s Spectrum

DVB-S2 modulator modules that were required to support the waveform on the BDR-1. Since the BDR-1 uses a direct conversion scheme, the *DDS* module was required. The Xilinx DVB-S2 FEC encoder was chosen for this implementation due to the space constraints of the SX50T FPGA; the AHA FEC encoder is considerably larger than the Xilinx implementation. AHA has subsequently released a high-speed version of their encoder, that is comparable to the Xilinx implementation in size and performance, but at the time of this development effort it was not yet available.

The second step of the porting process was to identify the BDR-1 board support modules that were required to support the waveform implementation. The board support package provided the porting team the following interfaces:

- Gigabit Ethernet. for command and control
- High-speed DAC interface
- DAC Clock generation and control
- Power control, for the transmitted signal

All of these modules were reused in support of the porting process. The packaging of these modules with the test waveform, saved the porting team approximately 3 man-months of effort, during the porting process.

Figure 7 details the architecture of the HDR DVB-S2 within the BDR-1 platform. (The shaded regions represent the BDR-1 support modules.) The hardware porting effort, i.e. just the VHDL, took approximately 2 man-months of effort. Table 1 details the FPGA resources used to implement the HDR DVB-S2 waveform, on the reference platform and the BDR-1. The BDR-1 FPGA clock is set to 218.75 MHz. The modulator can support symbol rates from 1 to 218 Msym/s. The symbol rate is lower than the reference implementation, since the reference implementation supports a DAC sample clock of 2.24 GHz.
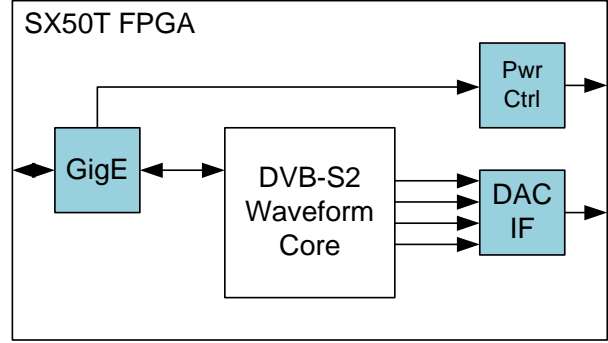

Figure 7 HDR DVB-S2 Waveform with the BDR-1 Support Modules

Table 1 HDR DVB-S2 Waveform FPGA Utilization

Platform	Registers	LUTs	BRAM	DSP48s
Reference (SX240T)	21k	20k	111	20
BDR-1 (SX50T)	26k	22k	122	20

4.2 Software Port

Due to the layered approach of the software architecture, the porting effort for the command and control software was less intensive. The driver layer needed to be adapted to support the slightly different command structure used in the BDR-1. The application layer GUI was updated to add the option of connecting to the BDR-1. All told the porting effort took less than 1 man-week.

5. RESULTS

The HDR DVB-S2 waveform ported to the BDR has subsequently been utilized in over-the-air tests. One such test utilized the HDR DVB-S2 waveform on the BDR as the modem for a 37-38 GHz point-to-point system. The resulting output spectrum for a 50 Msps 8PSK carrier at 37-38 is shown in Figure 6.

Additionally, the HDR DVB-S2 waveform running on the BDR-1 was tested for interoperability at the physical layer against commercial and military DVB-S2 compatible modems. Table 2 lists the results of the interoperability tests. A commercially available modem (Newtec AZ410), a modem developed by ECC/Viasat for the Office of Naval Research, and a modem developed by Avtec Systems for MIT Lincoln Laboratory were able to demodulate the BDR-1's transmitted signal. Additionally, the ECC/Viasat and Avtec modems were able to demodulate up to 200 Msps waveforms generated by the BDR-1.

Table 2 BDR-1 DVB-S2 Interoperability Matrix

Modems	Symbol Rates
Newtec AZ410	45 Msym/s
HIBEAM, Phase 1	50 Msym/s
HIBEAM, Phase 2	200 Msym/s
HDRM	218 Msym/s

6.0 CONCLUSION

In this paper the authors briefly discussed commonsense approaches for packaging a waveform implementation to increase the portability of the design. The design's portability was then demonstrated by the porting to a small but versatile SDR platform, i.e. the BDR-1. It was further shown that leveraging the investment of industry increased the usability and fieldability of the waveform implementation.

7.0 BIBLIOGRAPHY

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