A Software-Defined Radio Prototyping Platform for Cognitive Radio Applications

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Outline

• Motivation
• Platform Overview
• Cognitive Radio System Implementation
• Sensing Results
Motivation

- Multitude of wireless communication systems came up in the last years
- Increasing system complexity (higher-order modulation, sophisticated forward error correction etc.) to increase spectral efficiency
**Motivation**

- The range of usable frequencies is limited
  - Lower frequencies require unworkably large antennas
  - Higher frequencies only propagate over very short distances
- Thus some spectrum bands are more valuable than others
  - Causes an additional squeeze at certain ‘sweet-spot’ frequencies (typically 500 MHz – 5 GHz)
Motivation

- Flexible prototyping platform desirable
- Implementation of arbitrary communication systems
- Cognitive radio capabilities
  - Sense the environment
  - Track the changes
  - React upon findings
- Software-defined radio approach advantageous

UMTS? GSM? WLAN? WiMAX? DVB-T?
Platform Overview – Requirements

- Rapid Prototyping Capability
- Efficient Scheduling
- Elaborate Debugging Functionality
- High Degree of Parallelization Capability
- High Modularity
- Scalability
Platform Overview – DSP

• Prototyping platform eFalcon hosts a powerful triple-core C6474 DSP for top-level scheduling and signal processing with elaborate debugging functionality

• DSP features:
  • 1 GHz system clock
  • 3 MB on-chip RAM
  • EDMA controller
  • Gigabit Ethernet
  • Serial RapidIO (two lanes)
  • Antenna interface (6 full-duplex OBSAI/CPRI links)
  • Turbo and Viterbi decoder
  • …
**Platform Overview – FPGA**

- Xilinx Virtex-5 SX50T FPGA directly attached to the DSP using high-speed serial interconnections (Serial RapidIO, OBSAI, CPRI)

- FPGA features:
  - 52,224 logic cells
  - 4.7 Mbit block RAM
  - 12 digital clock managers (DCM)
  - 12 RocketIO transceivers
  - ...

- FPGA can be used as co-processor dedicated to specific signal processing tasks
Platform Overview – Additional Features

- 256 MB DDR2 RAM directly attached to the DSP
- DDR2 SODIMM connector directly attached to FPGA
- USB 2.0 controller with 8051 microcontroller connected to the FPGA
- 2 Gigabit Ethernet PHYs connected to the DSP and the FPGA
- SD memory card slot
- Avnet Full EXP connectors acting as daughter card interfaces
- Sophisticated clock subsystem
Platform Overview – Block Diagram

**Power Supply Subsystem**

- +12V DC, 5A max

**Platform**

- TMS320 C6474
  - 3-core, 1GHz DSP
- XC5VSX50T
  - Virtex-5 family
- OBSAI (3.072Gbps)
- 256MB DDR2 RAM
  - (64Mx16 DDR2 device)
- SATA connector
- EXP1 connector
- EXP2 connector
- 88E1111 Gigabit Ethernet PHY
- SATA connector
- EXP1 connector
- EXP2 connector
- 88E1111 Gigabit Ethernet PHY
- SATA connector
- SATA connector
- 64 bit DDR2 bus
- 88E1111 Gigabit Ethernet PHY
- SATA connector
- DDR2 SODIMM 200pin connector
- CY7C68013A USB controller
- USB 2.0 Interface
- EEPROM
- 8 bit bus
- Platform Flash
- Reset logic
- USB connector

**Clock Subsystem**

- Reset logic and power monitoring, Including CPLD
- 34 Single-Ended I/Os 19 Differential I/O Pairs 1 Multi-gigabit Lane 2 clock inputs, 2 outputs
- SFCMI
- SFCIO
- SFCIO
- 34 Single-Ended I/Os 19 Differential I/O Pairs 1 Multi-gigabit Lane 2 clock inputs, 2 outputs
- Clock
- Reset logic
Scalability Aspects

• Crucial design constraint during concept phase
• eFalcon provides high-speed intra-board as well as inter-board communication
• Interconnection of multiple platforms with data rates beyond 1 Gbit/s possible
• Realization of multi-antenna systems possible
• Overall clock synchronization possible by coaxial connectors
Platform Realization
Cognitive Radio System Implementation

- Non-occupied frequency ranges in the UHF band (TV white space)
- Can be used for secondary communication systems
- Here:
  - Primary system: CMMB
  - Secondary system: IEEE 802.11
- Sensing approach based on autocorrelation algorithms

CMMB Chinese mobile television and multimedia standard
Cognitive Radio System Implementation

Cognitive Radio Front-End

RF Front-End

Clock Generation & Distribution

A

D

eFalcon

D

A

Clock Generation & Distribution

A

D

LO Synthesizer

I/Q Modulator

IEEE 802.11 Front-End

DGA

LNA

I/Q Demodulator
Cognitive Radio System Flow Diagram

**Initialization**
- Wait for trigger
- Tuner setup
- Sensing operation
- Evaluation & reporting

**IEEE 802.11 operation**
- Initialization
- Trigger sensing engine
- Evaluate sensing results
- Frequency band available?
- (Re-)configure transceiver
- Stop transceiver operation
- Delay
- Start/continue transceiver operation

**Sensing operation**
- Start/continue transceiver operation
- Delay
Sensing Results

![Graph showing sensing results with various performance metrics.](image-url)
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Thank you for your attention!