# Comparison of Processor Architectures for LTE Channel Estimation

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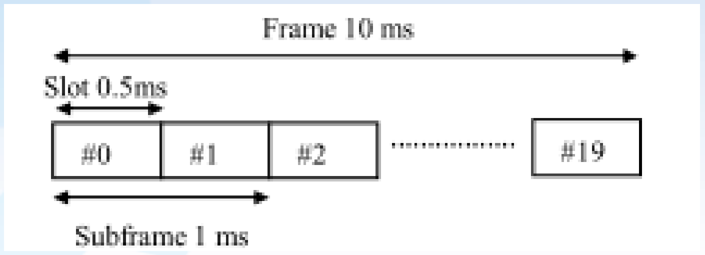
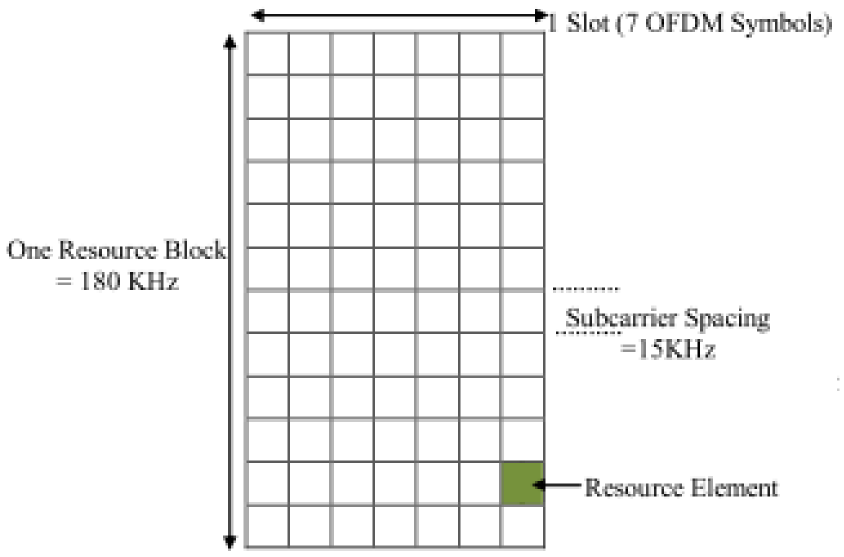
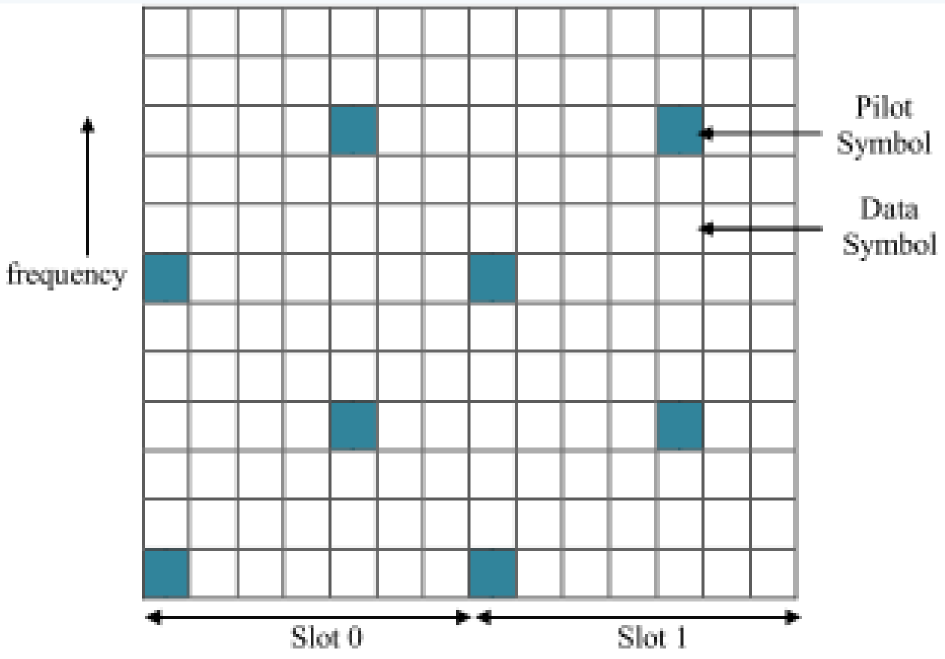
- **Case Study:** Channel Estimation for LTE with 20MHz system Bandwidth
- **Objective:** Comparison of different processor architectures for the case study
- Architectures under consideration:
  - COFFEE RISC
  - Ninesilica NoC with 9 COFFEE RISC Cores
  - TMS320C6416 DSP by Texas Instruments
  - Xentium (Run time recofigurable core by RECORE systems)
  - Transport Triggered Architecture (TTA)

# LTE Frame Structure







# Channel Estimation Algorithm in Brief

- Good estimate of channel is necessary to correctly demodulate the symbols
- Hexagonal grid type reference symbol pattern is used in our case
- First logical step in channel estimation is

$$Hp = Yp / Xp$$

  - Hp, Yp and Xp are channel estimate at pilot symbol, received pilot symbol and original pilot symbol
- Next step is to interpolate the channel estimate at all other symbol positions using the estimates calculated at pilot positions
  - Interpolation technique used in our case is Cubic Interpolation
  - Corresponding equation for cubic interpolation for *k-th* subcarrier is

$$\hat{H}_k = C_1\tilde{H}_{(m-1)D} + C_0\,\tilde{H}_{mD} + C_{-1}\tilde{H}_{(m+1)D} + C_{-2}\tilde{H}_{(m+2)D}$$

where,

$$\begin{cases} C_1 = -(1/3)\mu + (1/2)\,\mu^2 - (1/6)\mu^3 \\ C_0 = 1 - (1/2)\mu - \mu^2 + (1/2)\mu^3 \\ C_{-1} = \mu + (1/2)\mu^2 - (1/2)\mu^3 \\ C_{-2} = -(1/6)\mu + (1/6)\mu^3 \end{cases}$$

Here is an assumption for every *k-th* subcarrier as follows:

$$k/D = m + \mu$$

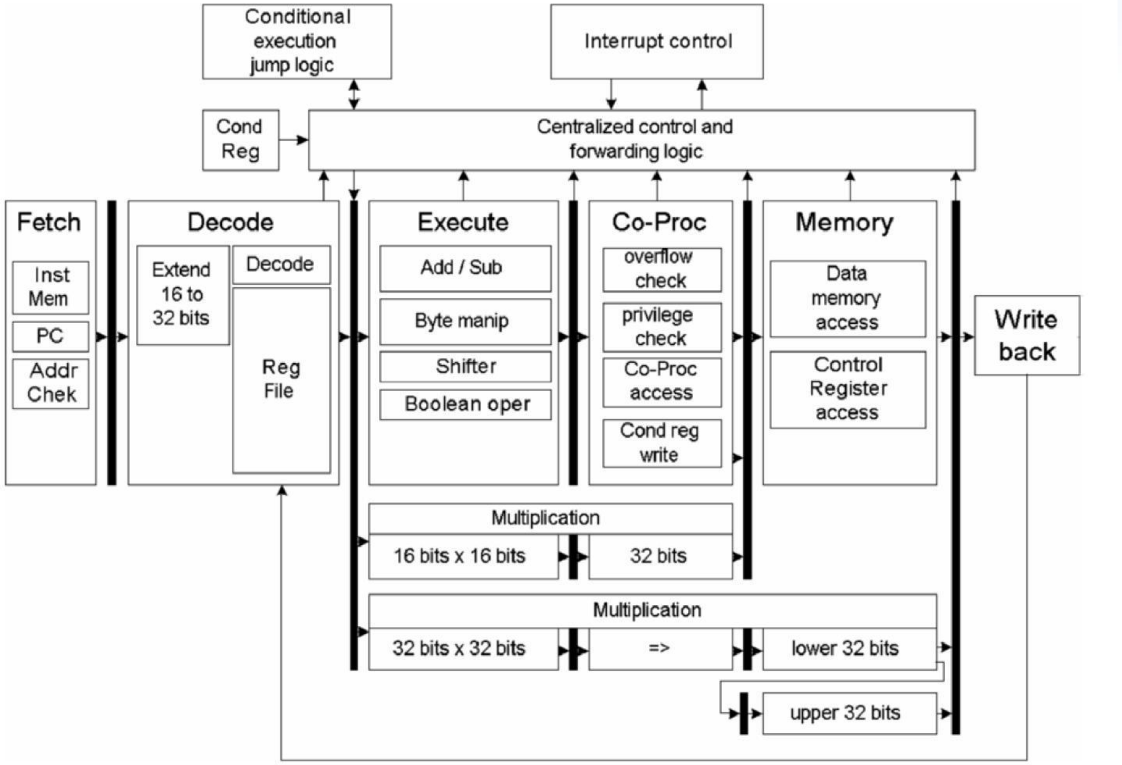
where,

*D* is the adjacent pilot symbol spacing for a subcarrier and *m* is the largest integer smaller than *k/D*

## Implementation made on different processor architectures

# COFFEE RISC

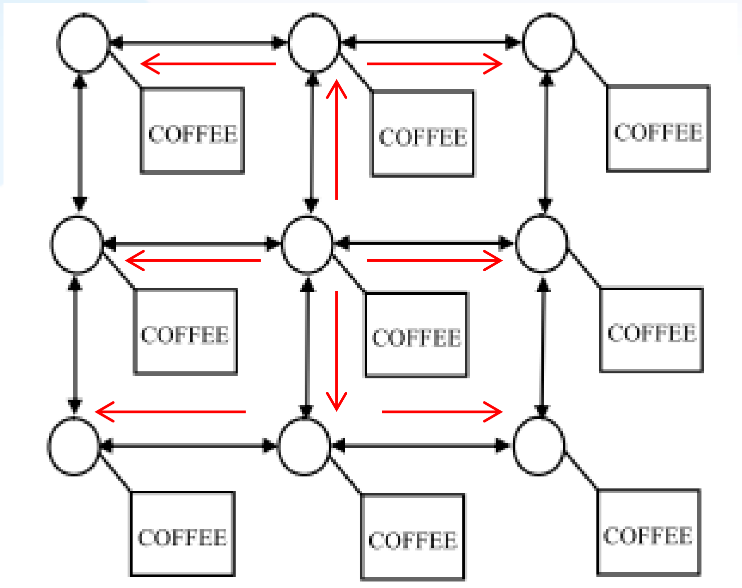
- General purpose embedded processor developed at Tampere University of Technology

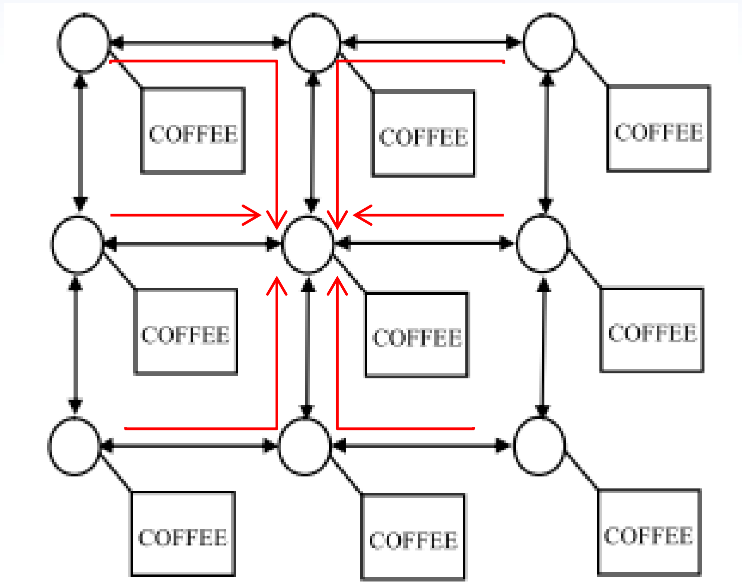


- This core was developed with intention to work in a conventional embedded system for telecommunication and multimedia applications or as a GP node in a NoC.
- To complete our task it took almost 1,657,900 cycles
- Running on Stratix-IV @181Mhz consumed 1.12 mJ
- Adding a hardware logic for division operation could reduce the cycle count to 322000

# Homogeneous MPSoC

- MPSoC based on nine COFFEE cores has been developed at Tampere University of Technology





- Central node behaves as Master
- Master node distributes the data in equal chunks
- Data is processed
- Results are returned back to the master
- Speed up gained as compared to single COFFEE is almost 6x.
- Number of cycles take to complete the task are almost 271577
- Running on Stratix-IV @181Mhz consumed 1.033 mJ

# Xentium by RECORE Systems

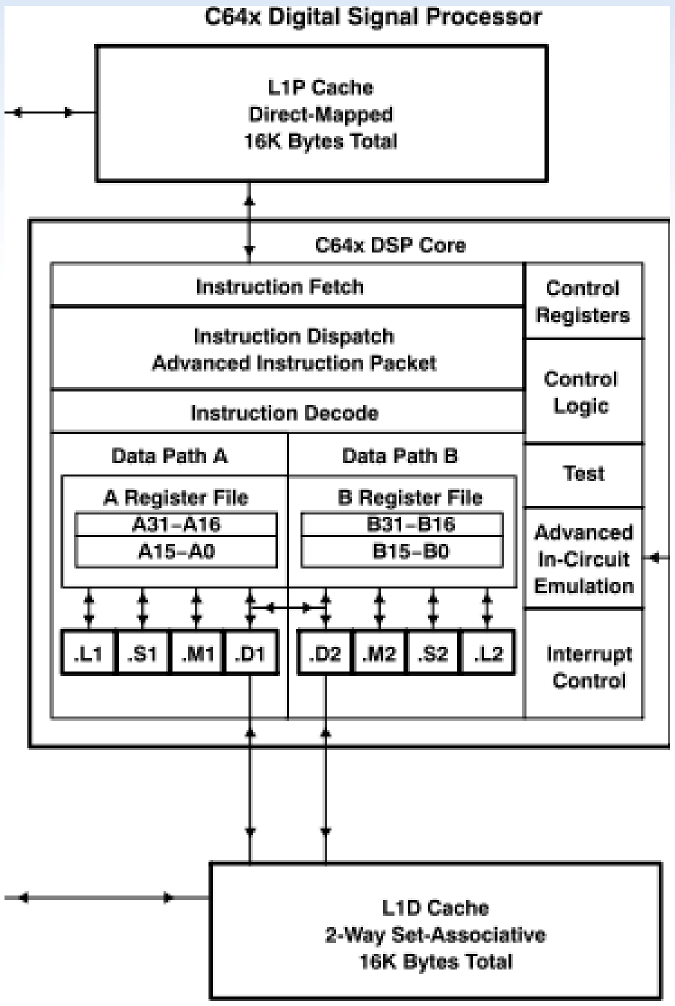
- Xentium is a fixed point VLIW-DSP optimized to perform digital baseband processing tasks
- The datapath consists of 10 functional units that can operate in parallel
- Data memory is organized in parallel memory banks to allow simultaneous access
- Xentium running on 90nm@200 consumes 175 µW/MHz
- It takes almost 495,725 cycles to complete the task and should consume approximately 0.086 mJ

# TI’s TMS320C6416 DSP

- •TI’s fixed point VLIW-DSP processor
- •It accommodates two independent data paths
  - •Four functional units (one multiplier and 3

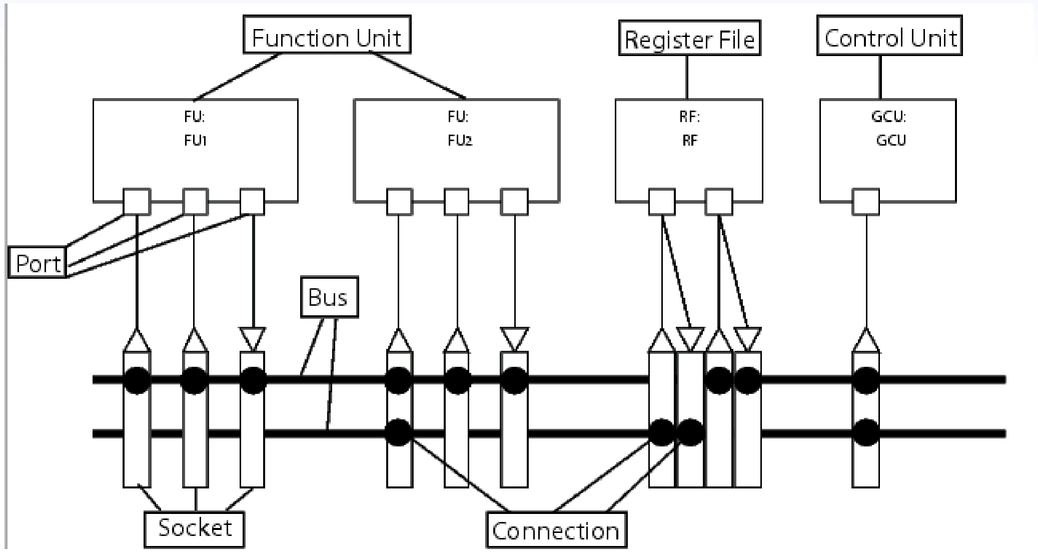
    ALUs) and 32 of 32-bit general purpose registers

    each
  - •Cross communication link between Data Paths
- •Total number of cycles it took are 403,692 cycles
- •Running on 130 nm CMOS@500MHz it should consume approximately 0.161 mJ to complete the task

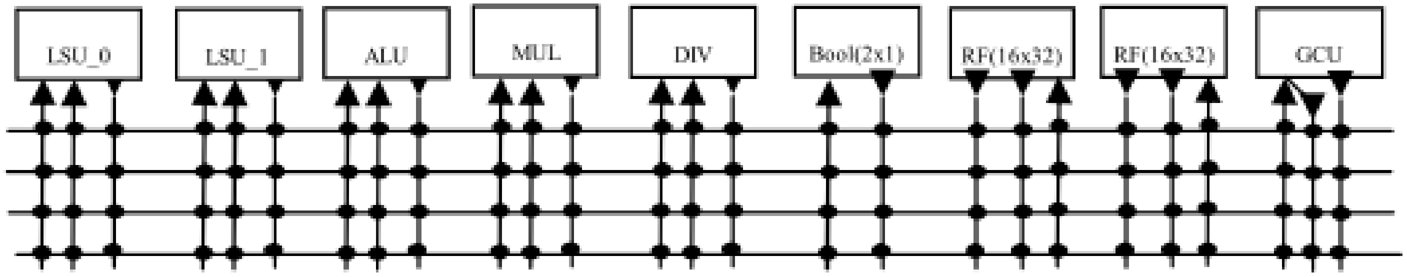


## TTA (Transport Triggered Architecture)

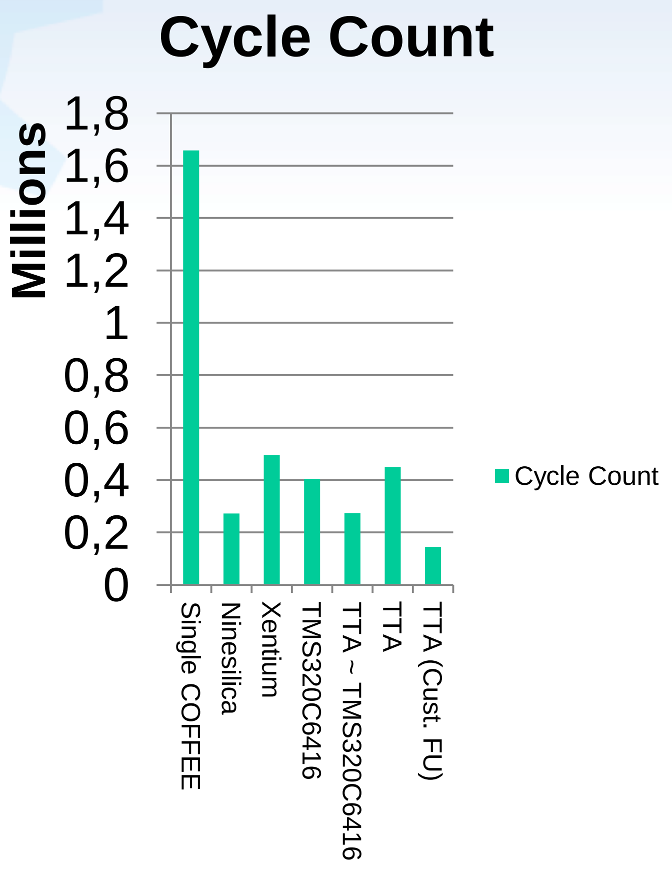
- •No particular instruction set architecture is defined for TTA
- •Based on a single instruction called "MOVE"
- •FU is triggered as soon as the data arrives
- •A typical architecture consists of several number of buses, functional units, register files and load store units
- •More closely resembles to a VLIW architecture
- •Scaling up TTA is much less complex because the functional units and interconnection network are independent of each other.

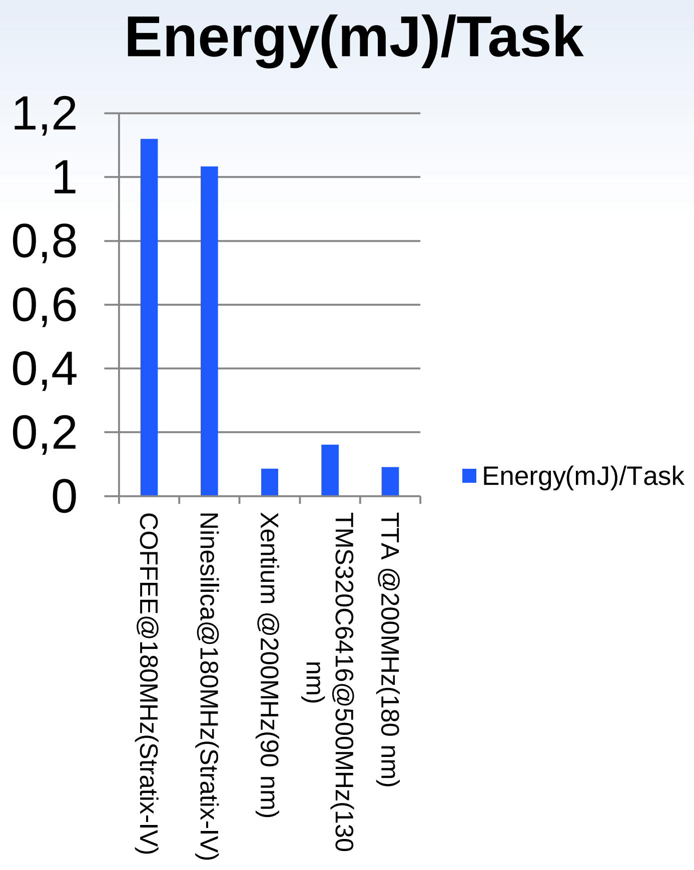


- TTA co-design environment (TCE) allows the TTA architecture to be built and tested gradually according to the application needs
- Trade-off between flexibility and performance can easily be translated by the programmer by making the right choices for the required functional units, their granularity level, other supporting units and the interconnection among the units
- Highly modular structure makes it easy to scale
- The channel estimation task took almost 449,736 cycles
- Adding a functional unit for square root the cycle count was reduced to 144814
- Targeted TTA on 180 nm@200MHz consumes 0.091mJ to complete the task



## Summary of Results





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Thank You !