

COMPLEXITY ANALYSIS OF SOFTWARE DEFINED DVB-T2 PHYSICAL LAYER

Stefan Grönroos
Kristian Nybom
Jerker Björkqvist

What we did

- In progress: Building a GNU Radio-based DVB-T2 modulator and demodulator
- Based on in-house DVB-T2 simulator
- Benchmarked individual signal processing blocks
 - If GNU Radio block had been implemented, it was benchmarked
 - ... or else the simulator block was benchmarked instead

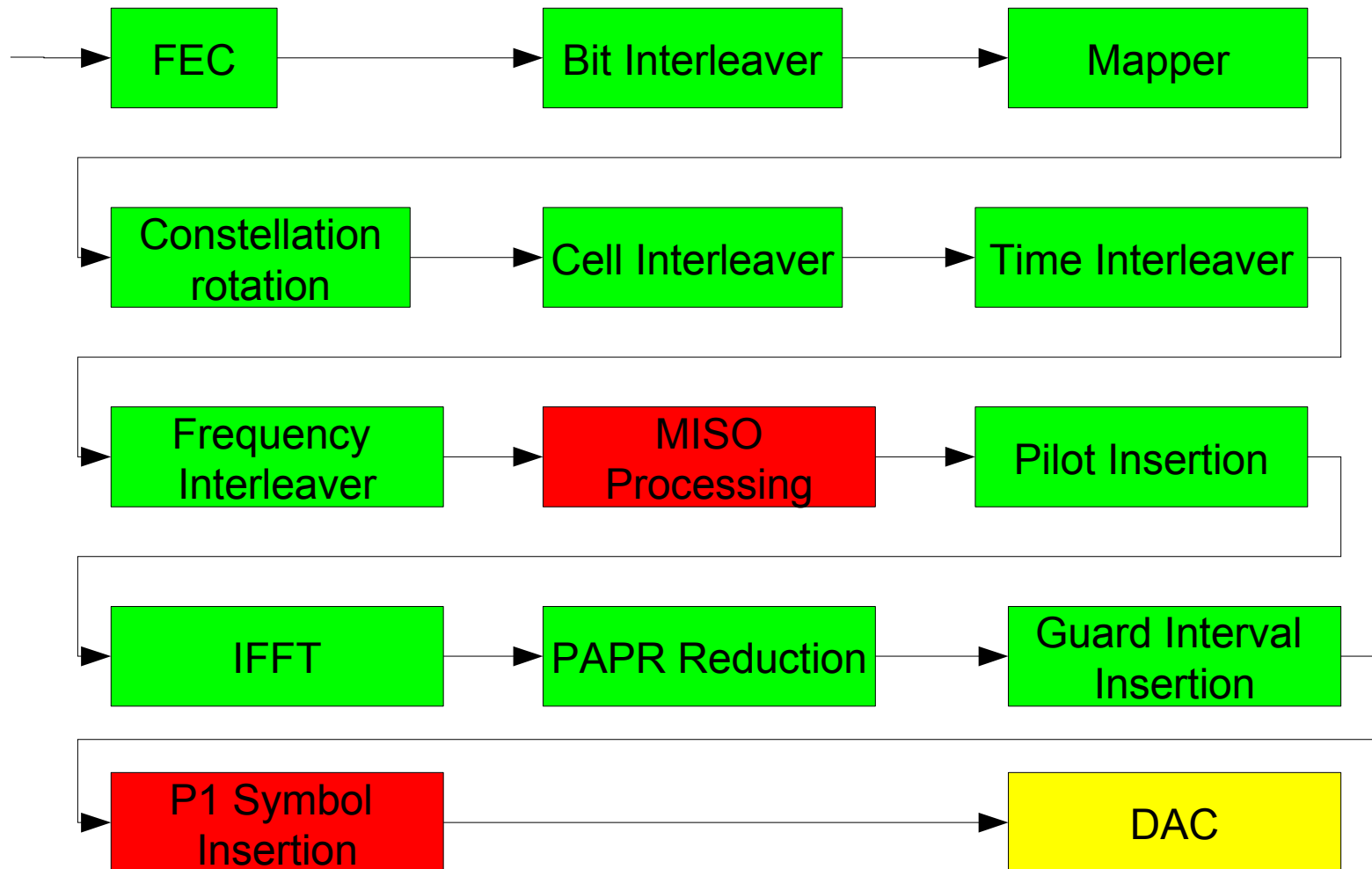
Why?

- Determine the feasibility of a software defined DVB-T2 system running on general purpose hardware
- Identify blocks that may need to be implemented on GPUs, FPGAs, etc.

DVB-T2

- Successor to the DVB-T (Digital Video Broadcasting – Terrestrial) standard
- Capacity increase of typically at least 30% vs. DVB-T
- Near-optimal FEC using BCH and LDPC codes

DVB-T2 Modulator



Benchmarks

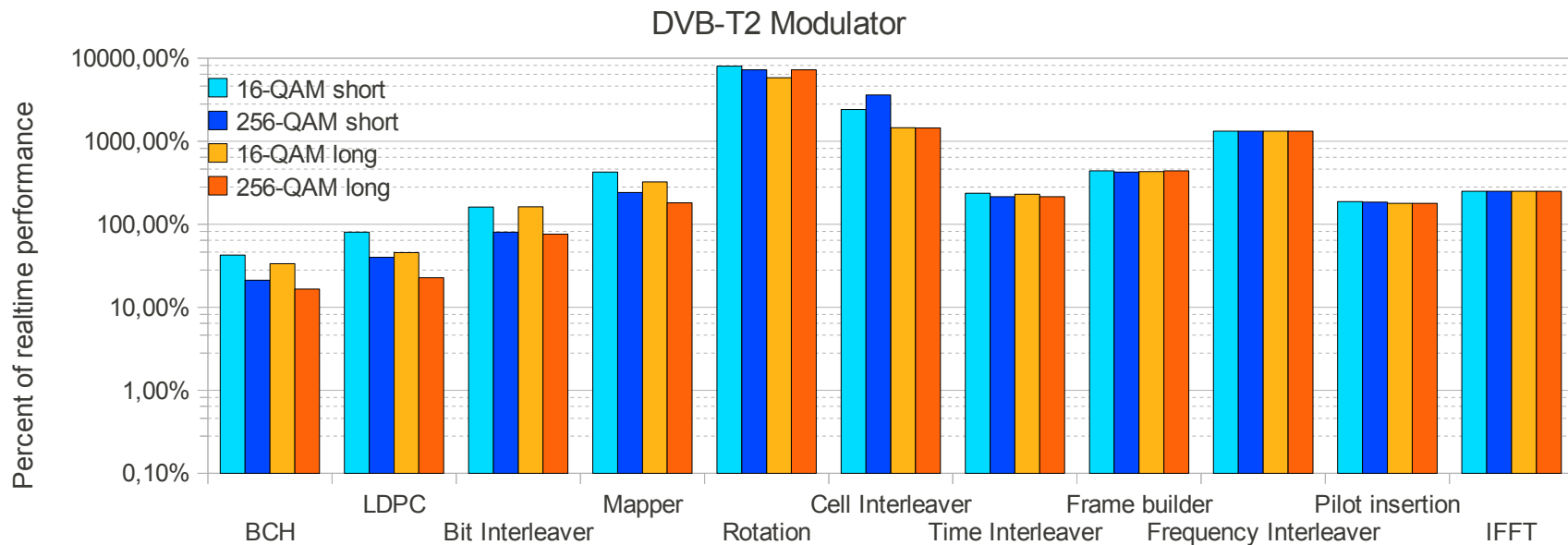
- Timed the execution of the core functionality of each signal processing block
 - Used `clock_gettime()` function in Linux to get time before/after execution
- Each block measured separately
- The size of a FEC block (16200 or 64800 bits) was divided by the execution time to obtain a throughput (Mbps) value
 - “Useful” throughput \approx
obtained throughput * FEC code rate
- 8K FFT

Benchmark setup

- Laptop
- Intel Core 2 Duo @ 1.8 Ghz
 - Only one core used for benchmarking!
- 3 GB DDR2 RAM
- Ubuntu Linux (Kernel 2.6.32)
- Note: Hardware rather old!

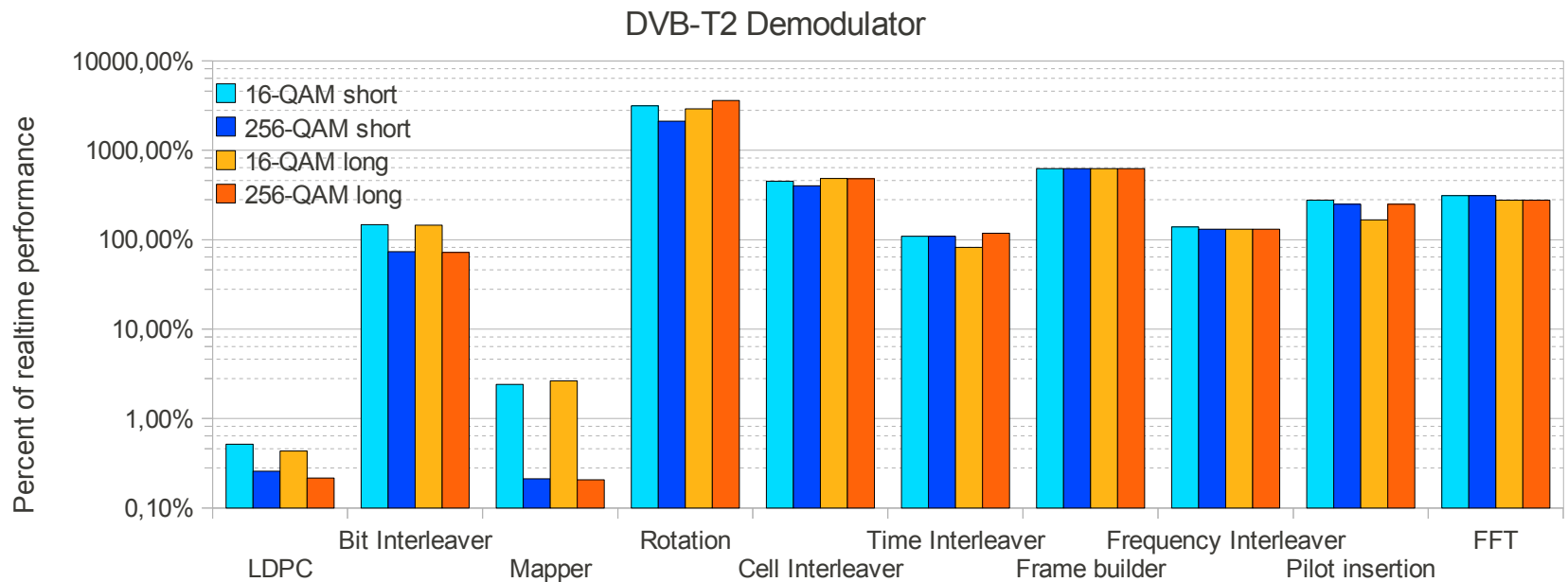
Benchmark results - Modulator

- Shows obtained throughput as a percentage of required throughput for realtime operation
- FEC coding at worst ~20% of realtime
 - Not necessarily a big problem



Benchmark results - Demodulator

- FEC and Demapper are at worst case $\sim 1/500^{\text{th}}$ of realtime performance!
- Note: BCH decoder not implemented



Results discussion

- LDPC algorithm: Sum-Product
 - Min-sum algorithm faster, though worse BER at same SNR
- Demapper complexity increases rapidly with higher order constellations
 - Simplified algorithms might be able to overcome this

GPU and FPGA

- Both demappers and LDPC decoders have been demonstrated on FPGA
- LDPC has been demonstrated to work quite well on GPU in some cases
 - LDPC memory accesses are quite irregular
 - Unclear how well the data structures for long code lengths will fit the limited fast memories of a GPU
- Demapper operations on each received cell value are independent of each other
 - Many values could be processed in parallel on a GPU

Conclusions

- DVB-T2 Modulator seems feasible even on modern general purpose CPUs
- LDPC decoding and demapping in demodulator might require use of alternative hardware

Thank you for listening!