

# Multi-GHz Software and Hardware Platform for Software Defined Radio



BEEcube

# SDR and Cognitive Radio Strategies Challenges

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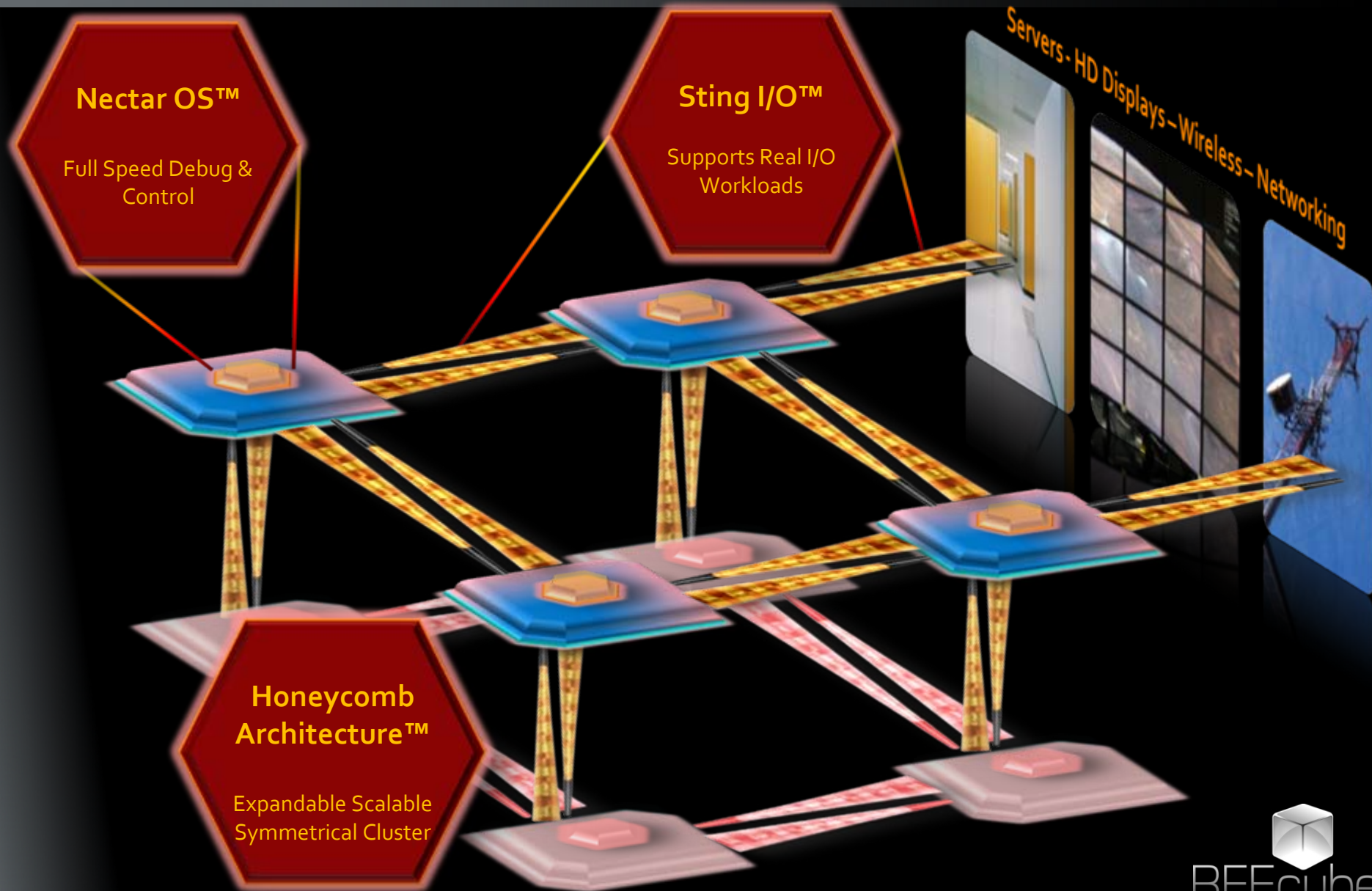
- Meeting “Dynamic” Mission-Critical Communication Needs
- Prototyping New Radio Algorithms in Real Time
- Mixed Signal (Analog and Digital) Designs

# BEE3-W —Digital Communication Design Platform



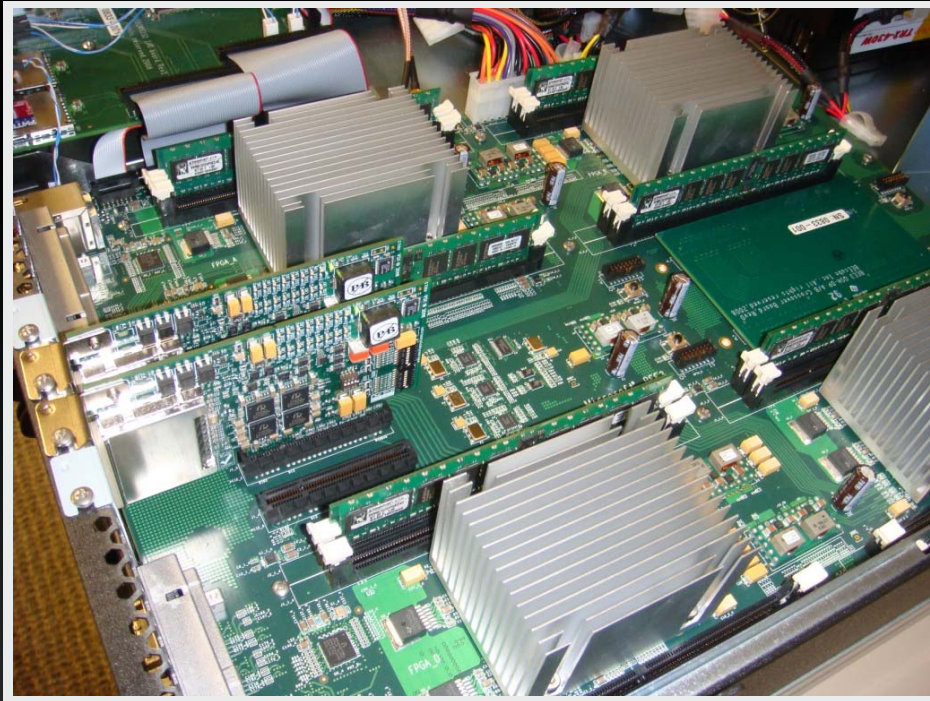
- Signal Intelligence
- Software Defined Radio
- Radar Signal Processing
- Cognitive Radio
- MIMO Communication
- Signal Warfare

# BEEcube Architecture

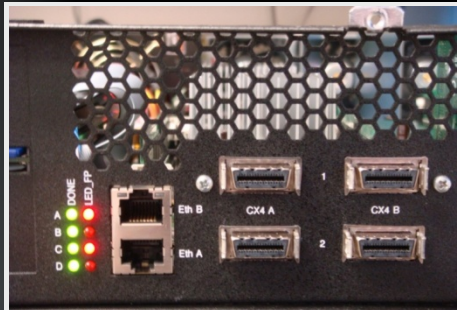




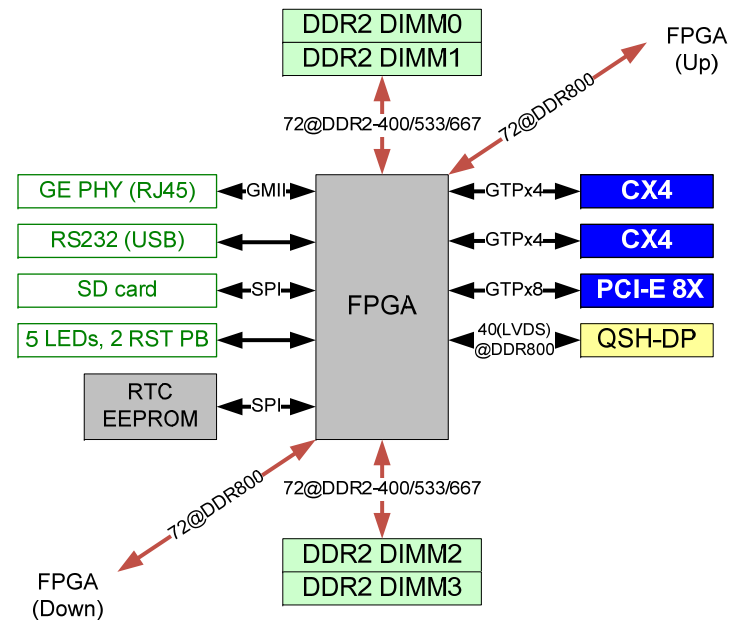
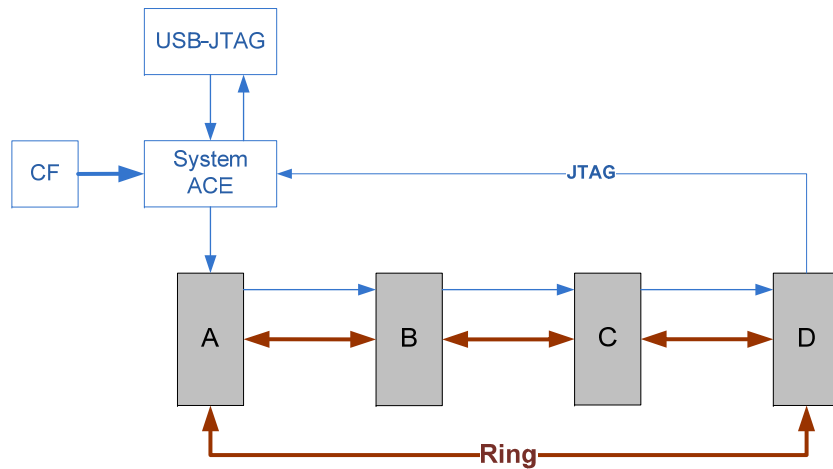
# BEE3 Hardware Platform



- Quad Xilinx Virtex-5 FPGA signal processing
  - 5M gate capacity
  - Integrated DDR800 inter-FPGA ring bus
- 64GB DDR2 ECC DRAM
- Multiple high-speed data interfaces
  - 160 Gbps SERDES I/O
  - Quad x8 PCI Express
  - Quad 1000BASE-T Ethernet
  - Quad 40-pair LVDS QSH expansion slots



# BEE3 Hardware Platform

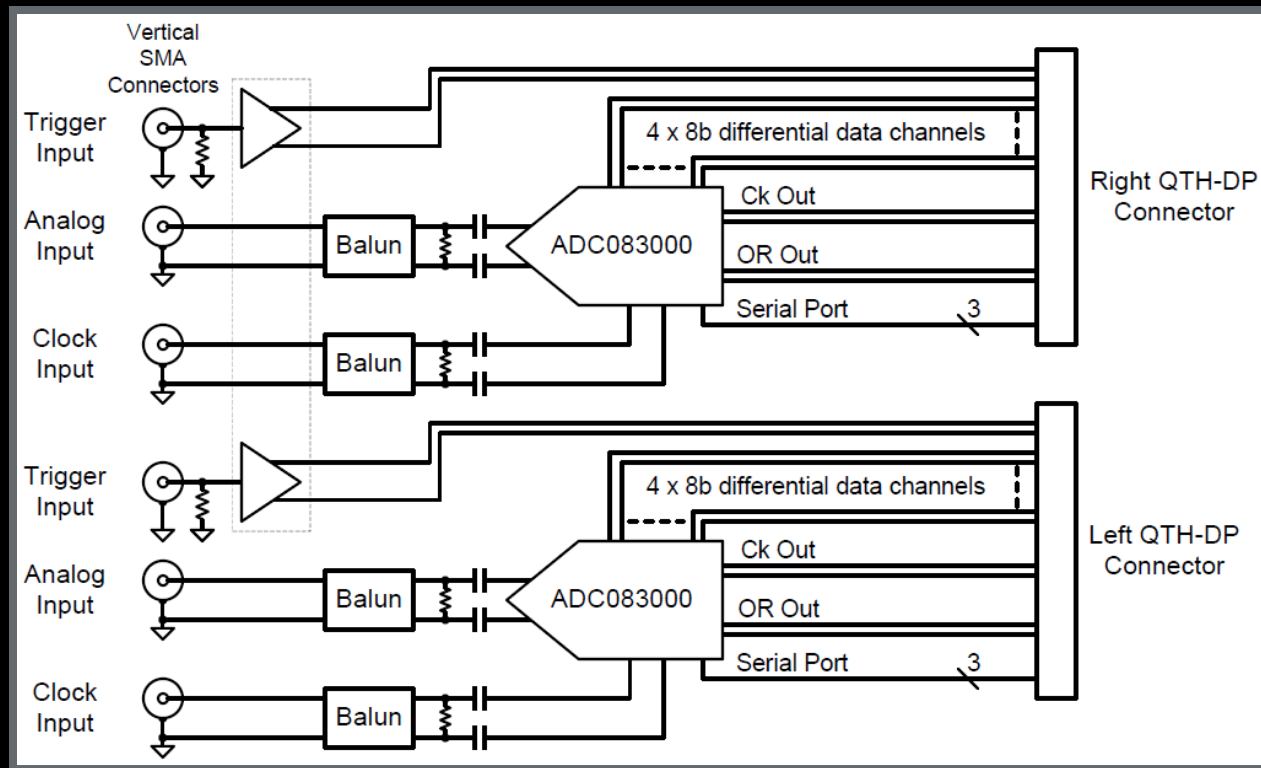


# ADC Expansion Boards for BEE3



- Dual-channel 3 GSps model
  - Two National Semiconductor ADC083000 ADCs
  - Independent clock, data, reset, and trigger SMA inputs for each ADC
- Quad-channel 1.5 GSps model
  - Two National Semiconductor ADC08D1500 ADCs
  - Independent clock, I-data, Q-data, and trigger SMA inputs for each ADC

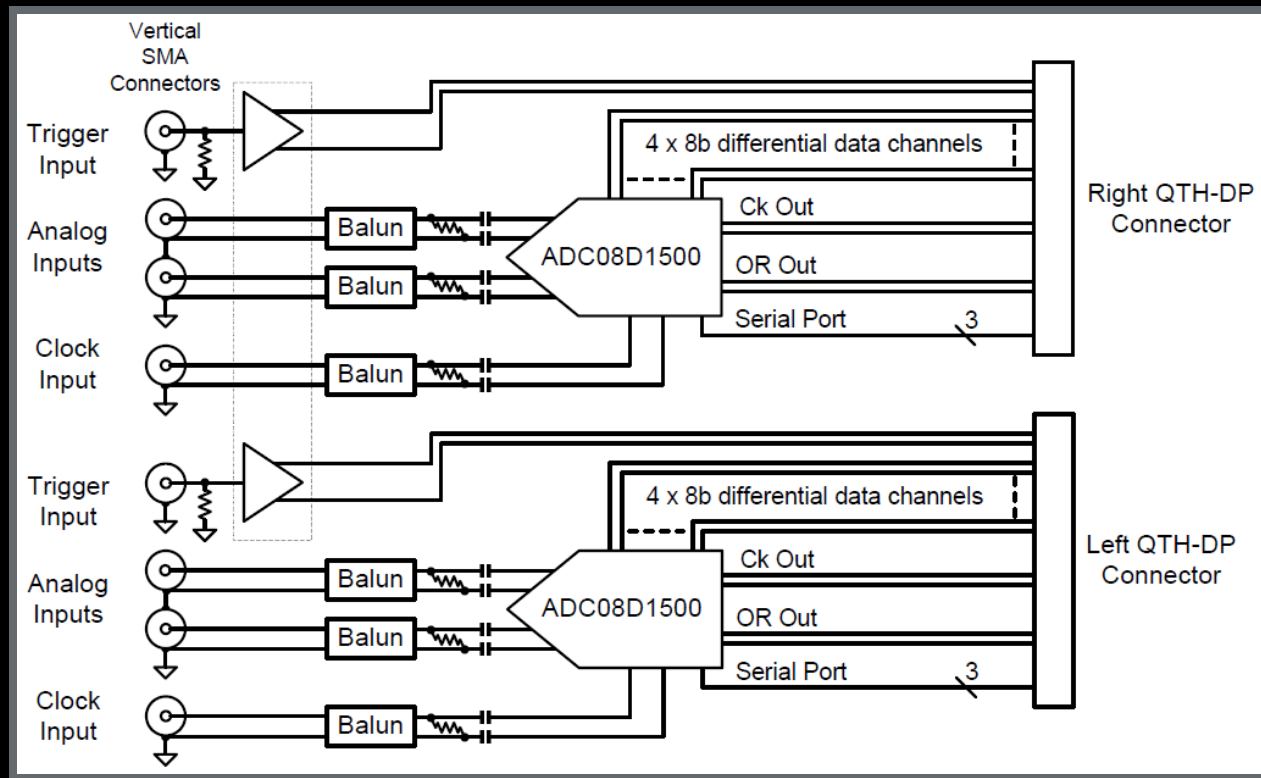
# Dual 3 GSps ADC Board



- 8-bit resolution, one channel per ADC/FPGA
- Analog sample rate 1000-3000 MHz
- Balun input bandwidth 30-1800 MHz

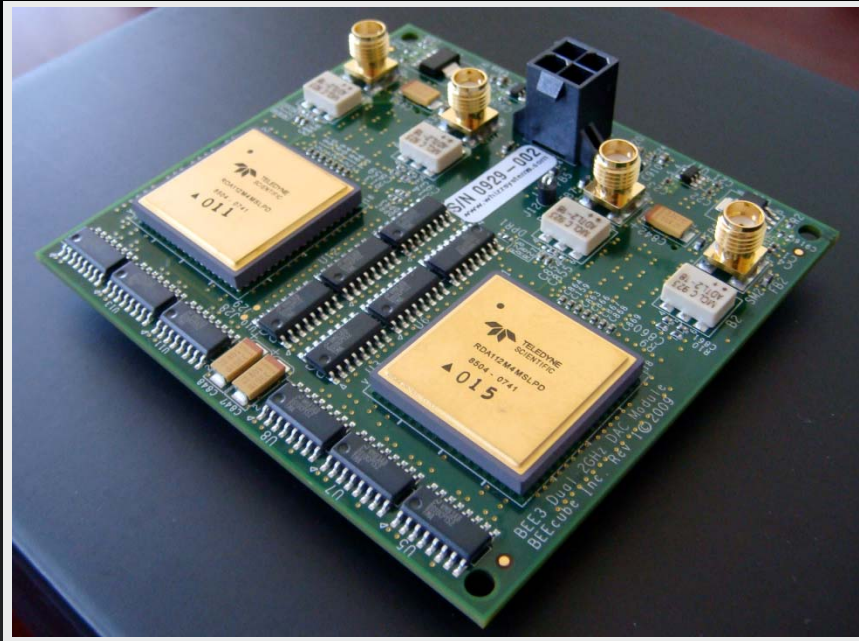


# Quad 1.5 GSps ADC Board



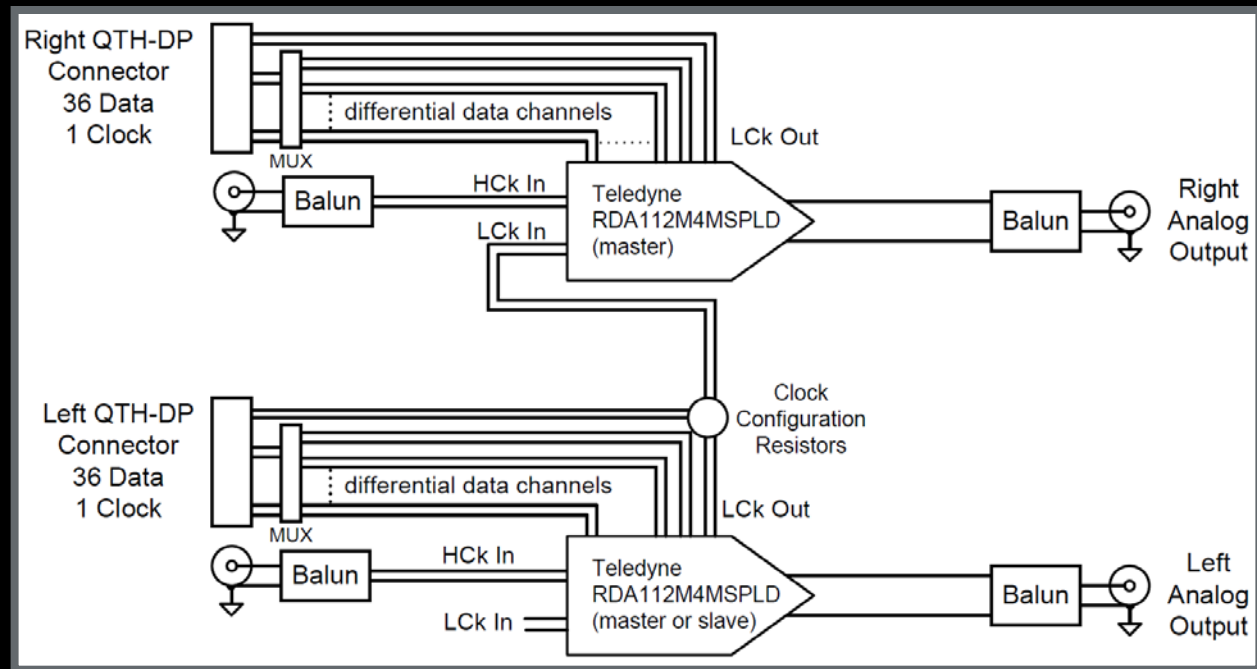
- 8-bit resolution, two channels per ADC/FPGA
- Analog sample rate 200-1500 MHz
- Balun input bandwidth 30-1800 MHz

# DAC Expansion Boards for BEE3



- Dual 2 GSps model
  - Teledyne RDA112M4MSLPD
  - Independent clock inputs and data outputs
- Factory configured in master-slave mode
- User-selectable resolution
  - 9-bit resolution up to 2 GSps (4:1 mux)
  - 12-bit resolution up to 1.5 GSps (2:1 mux)

# Dual 2 GSps DAC Board



- On-board muxes switch between 9-bit (4:1) and 12-bit (2:1) modes
- Nominal output level of 600 mV
- Configured for master-slave mode from factory

# SDR Reference Design

FPGA A

- 2 GSps DAC signal source
  - Carrier tone generated by FPGA-based numerically-controlled oscillator (NCO)
  - Arbitrary modulation pattern up to 16,384 samples contained in FPGA Block RAM (BRAM)

FPGA B

- 3 GSps ADC virtual oscilloscope
  - Data captured into FPGA BRAM in 16,384-sample windows
  - Captured data read via Ethernet or serial port into Matlab for direct analysis

# BEEcube Platform Studio

The screenshot displays the BEEcube Platform Studio interface, which is integrated with MATLAB 7.5.0 (R2007b). The main workspace shows a Simulink model for a BEE3 demo. The model includes blocks for the System Generator, BPS BEE3, MPMC, and ChipScope. The BPS BEE3 block is configured with a depth of 1024. The MPMC block is configured with a depth of 1024. The ChipScope block is configured with a depth of 1024. The model also includes a reset signal and a rising edge trigger. The System Generator Design Name is BEE3\_demo, and the XSG Version is 10.1.3. The ISE Design Flow Choice is Complete Build. The EDK Log is visible. The Run BPS button is highlighted. The Simulink Library Browser is open, showing the Platform Configuration block. The Platform Configuration block is described as: "This block configures the BPS tool flow for all system-level parameters specific to the current design and target platform. Please see the documentation for detailed information on how to tailor these settings to the requirements of your application." The Simulink Library Browser also lists various blocks, including BPS BEE3, ChipScope Configuration, Custom IP Core, Ethernet Interface, GPIO, Memory Controller, MPMC Basic, MPMC Direct, PCI Express Endpoint, Probe, Shared BRAM, and Shared FIFO.

**MATLAB 7.5.0 (R2007b)**

**BEE3\_demo**

File Edit View Simulation Format Tools Help

Shortcuts

Current Direct

All Files

BEE3\_demo

BEE3\_demo

.jpl.zip

load\_dram.i

sawtooth.m

uint32castf

Command Hist

slices

fibone

width2

**BEEcube Platform Studio 3.0**

**System Generator Design Name:** BEE3\_demo

**XSG Version:** 10.1.3

**ISE Design Flow Choice:** Complete Build

EDK Log

**View Report**

**Run BPS**

**Simulink Library Browser**

File Edit View Help

**Platform Configuration**: This block configures the BPS tool flow for all system-level parameters specific to the current design and target platform. Please see the documentation for detailed information on how to tailor these settings to the requirements of your application.

Simulink

BEE3 Blockset

Communications Blockset

Real-Time Workshop

Signal Processing Blockset

Simulink Extras

Stateflow

Virtual Reality Toolbox

Xilinx Blockset

Xilinx Reference Blockset

Xilinx XtremeDSP Kit

BPS BEE3

ChipScope Configuration

Custom IP Core

Ethernet Interface

GPIO

Memory Controller

MPMC Basic

MPMC Direct

PCI Express Endpoint

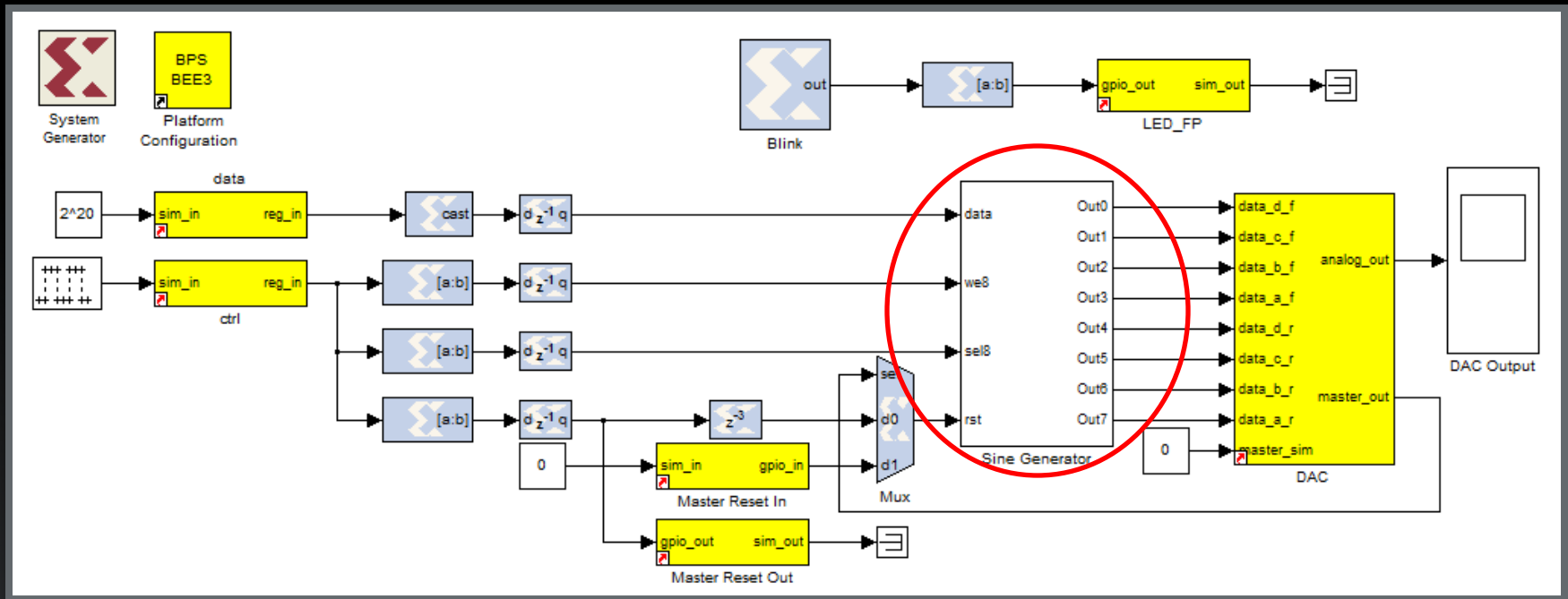
Probe

Shared BRAM

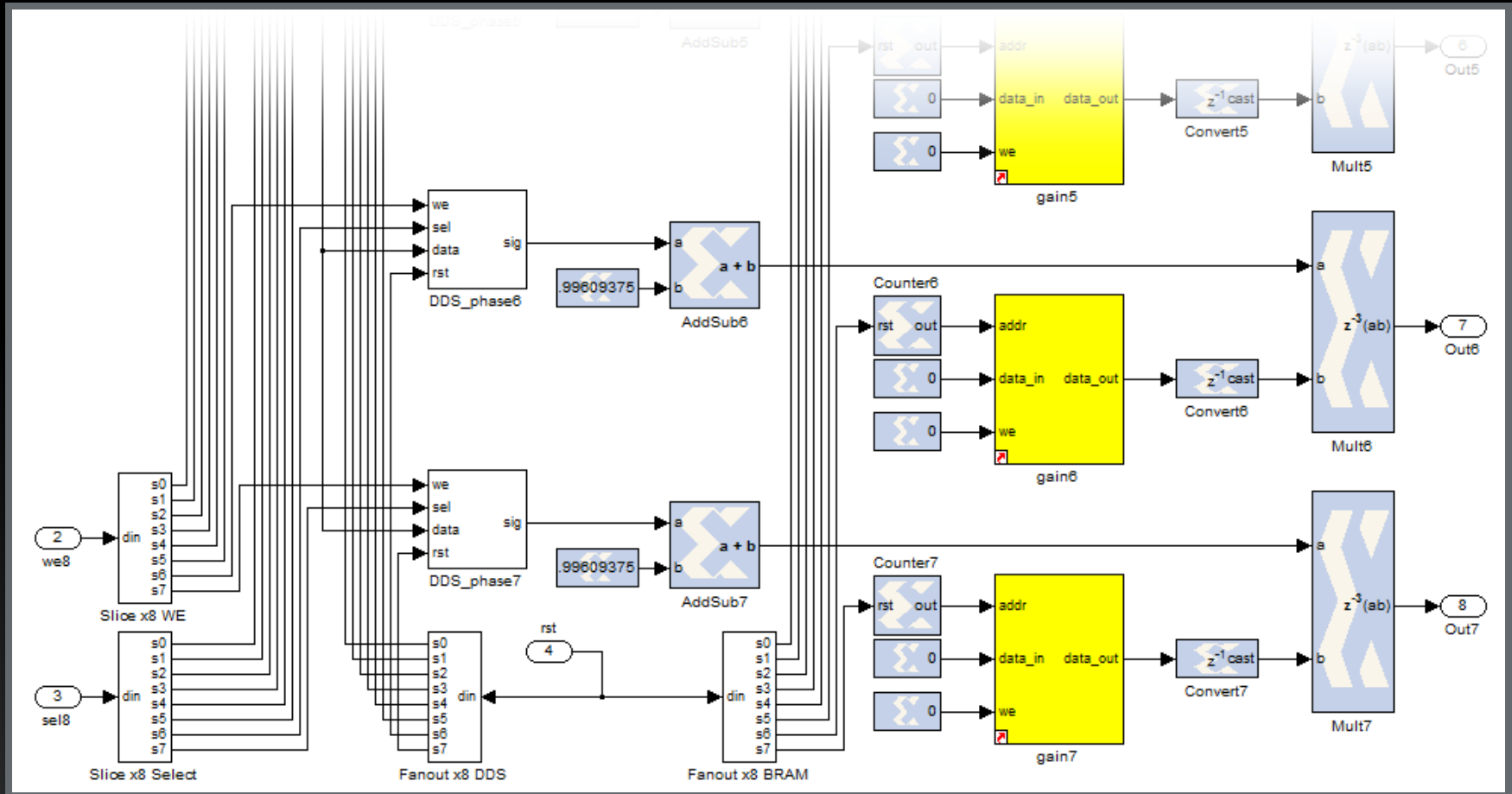
Shared FIFO



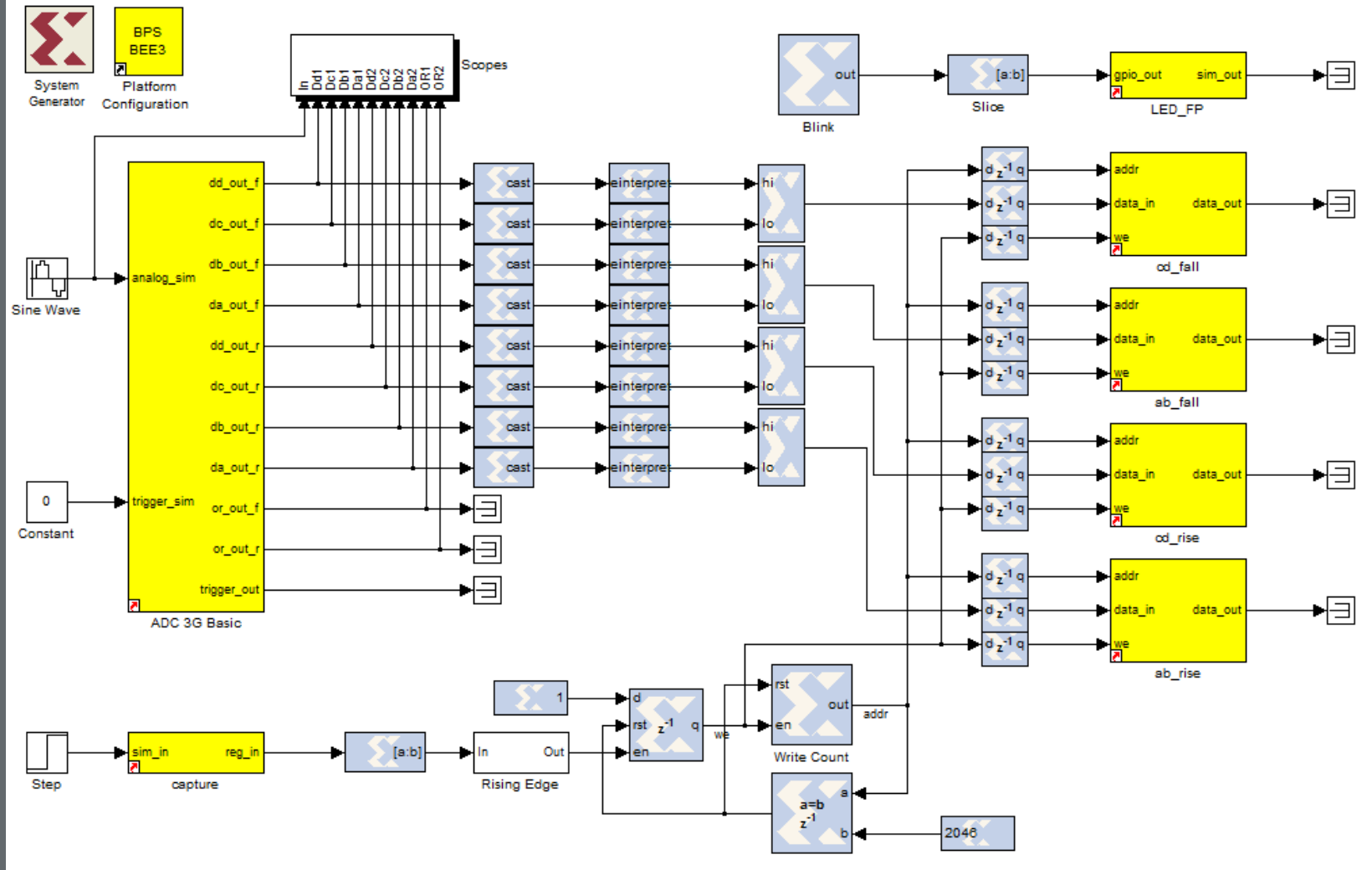
# DAC Signal Source Model



# DAC Signal Source Model



# ADC Virtual Scope Model



# DAC Signal Source Performance

- FPGA system clock runs at 250 MHz
  - Enforced by DAC sample rate of 2 GSps, DDR signaling, and 4:1 mux ratio
- NCO implemented using Xilinx DDS cores
  - CoreGen “DDS Compiler v2.1” specification
  - Up to 20 bits signal output precision, SFDR up to 120 dB,  $\Delta f$  down to 0.02 Hz
- Total device utilization on SX95T:
  - NCO: 9bit output, 1Hz resolution, 54dB SFDR
  - 4% DSP48s, 21% BRAM, 21% Slices

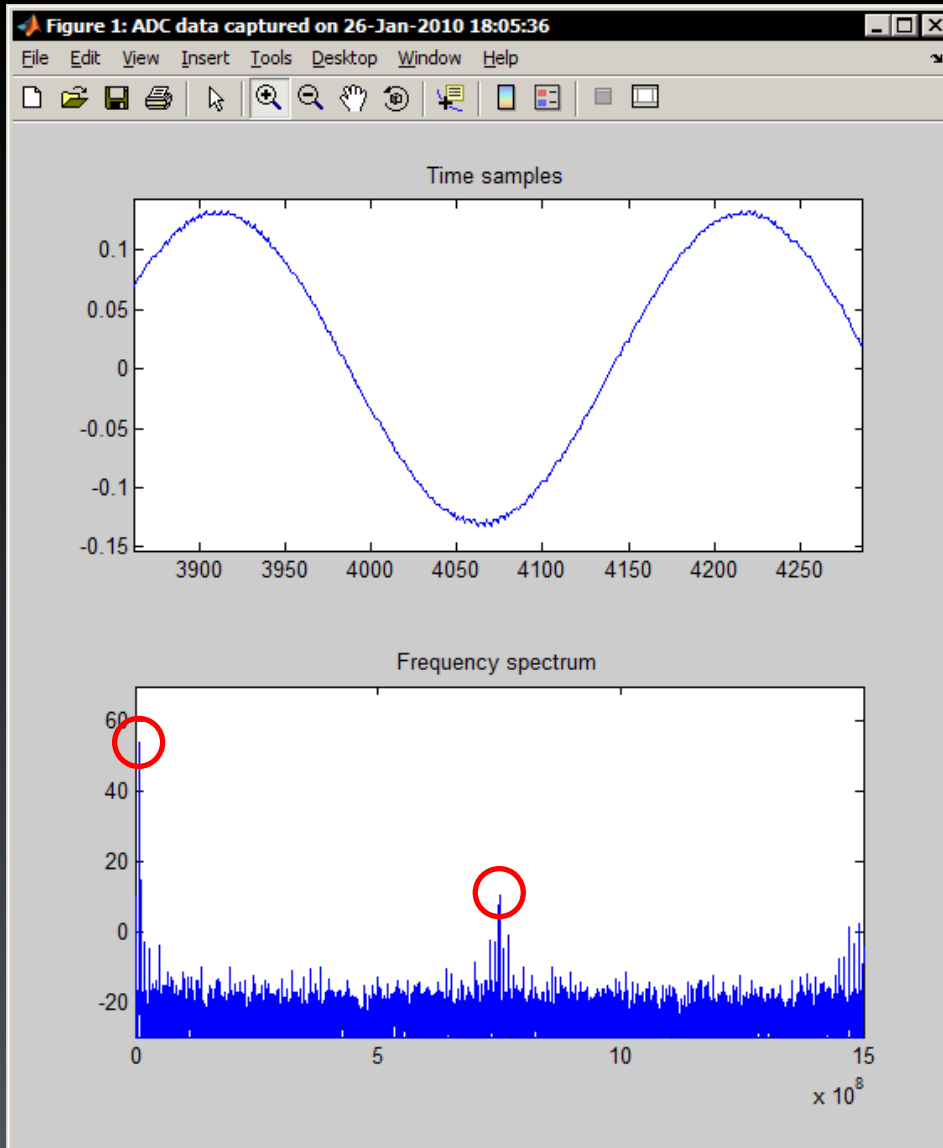
# ADC Virtual Scope Performance

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- FPGA system clock runs at 375 MHz
  - Enforced by ADC sample rate of 3 GSps, DDR signaling, and 4:1 demux ratio
- Total device utilization on SX95T:
  - 1% DSP48s, 16% BRAM, 15% Slices

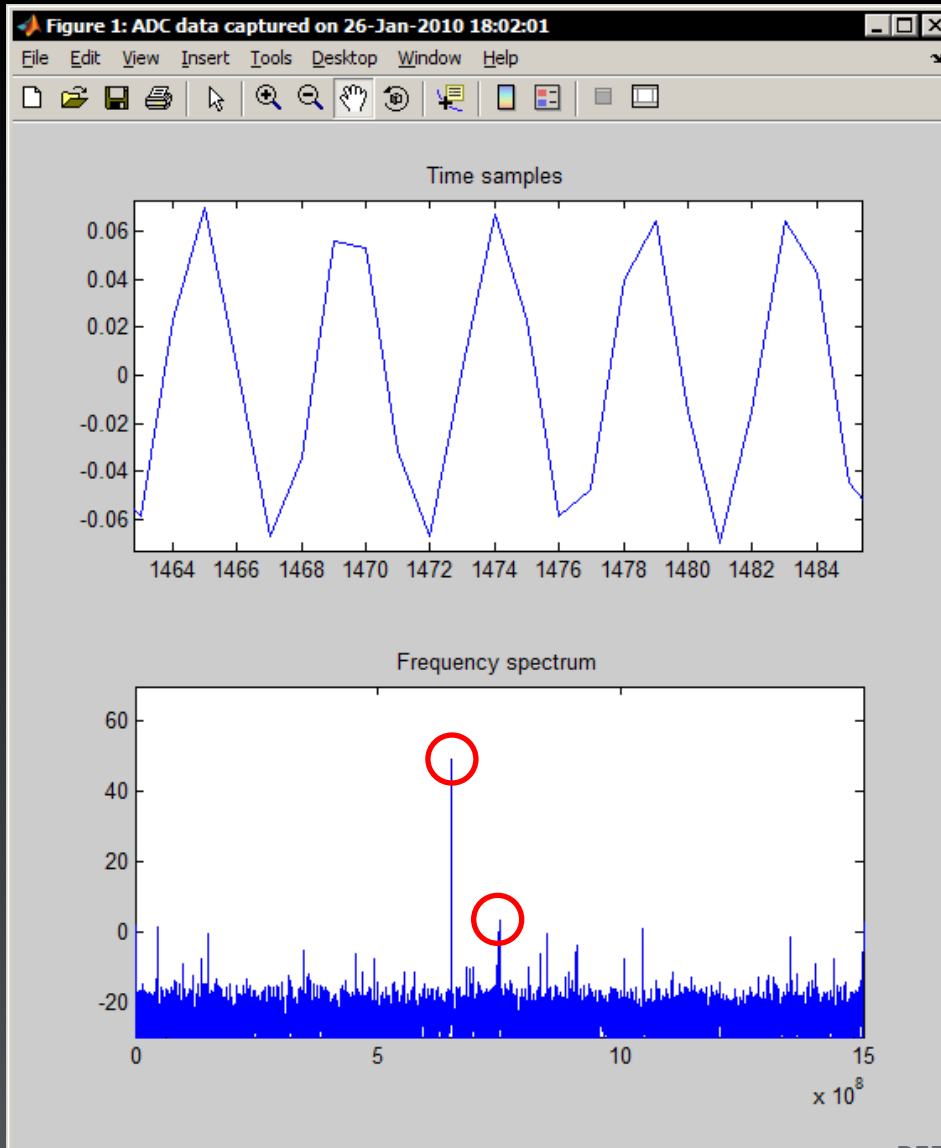


# Overall System Performance



- Results for 10 MHz tone:
  - Carrier peak @ 53.90 dB
  - Largest spur @ 10.64 dB
  - SFDR = 43.26 dB

# Overall System Performance



- Results for 667 MHz tone:
  - Carrier peak @ 49.1 dB
  - Largest spur @ 3.1 dB
  - SFDR = 46.0 dB

# Conclusion

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- Using a Flexible Platform allows Adding “Intelligence” to Signal Handling and Information
- And Can be Applied to:
  - MIMO communication,
  - Radar Applications,
  - Signal Intelligence and Warfare