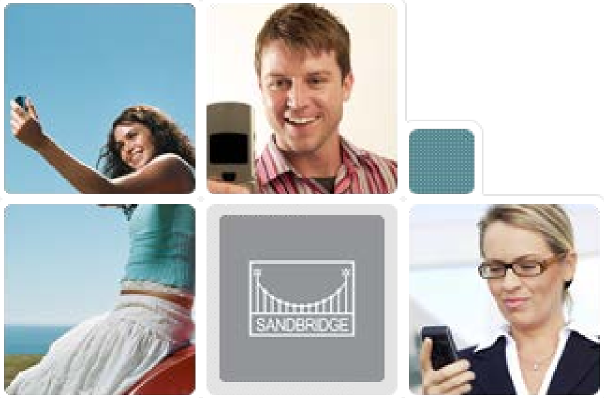


SANDBRIDGE TECHNOLOGIES

Software Solution for IEEE 802.11 g Receiver

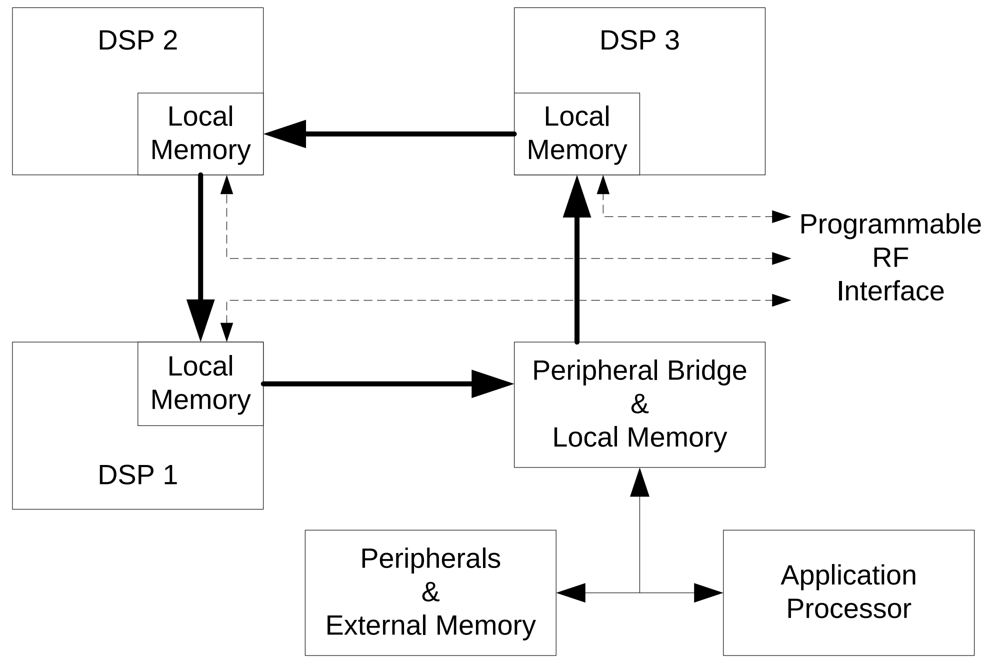
Dr. Meng Yu
mengyu@sandbridgetech.com

Agenda

- Sandbridge Sandblaster® SB3500 SoC
- Wireless LAN IEEE 802.11g
- Equalization for OFDM mode signal
  - Zero forcing equalizer (ZF)
  - Implementation and results
- Equalization for CCK mode signal
  - Linear minimum mean squared error equalizer (LMMSE)
  - Least mean square equalizer (LMS)
  - Decision feedback equalizer (DFE)
  - Equalizer performance comparison
  - Implementation results
- Summary

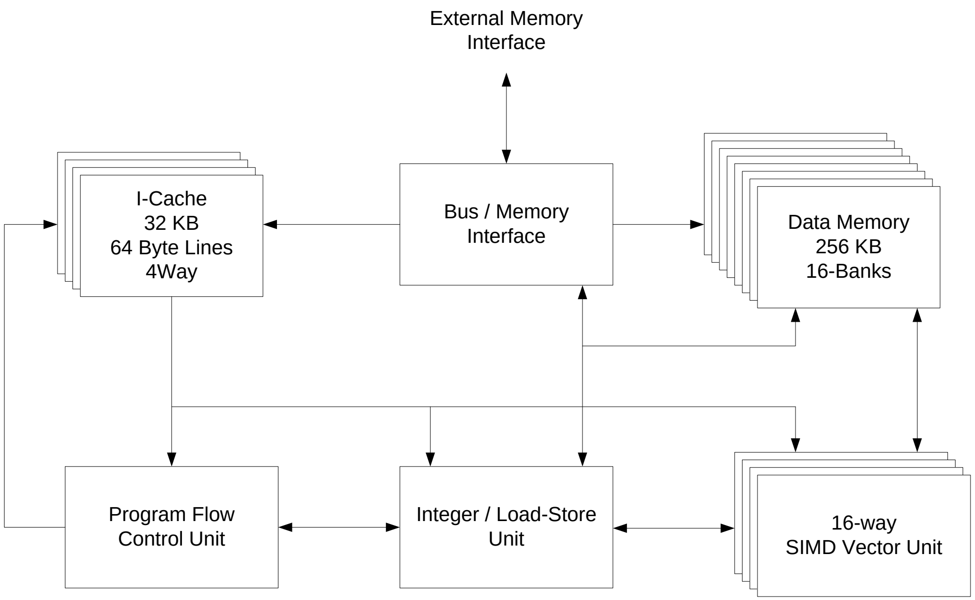
Sandbridge Sandblaster ® SB3500 SoC

- High performance, multi-threaded, low power design for convergence devices
- 3 Sandblaster extended DSP cores
  - Interconnected by uni-directional ring
- Integrated ARM 9 applications processor
- AMBA bus contains external memory, peripherals and application processor
- Programmable RF interface
  - Up to 240 million samples per second
- Integrated device power management
- Peripheral interfaces – LCD, camera, keypad, smartcard, USIM (universal subscriber identity module) , USB



Sandblaster® Extended DSP Core

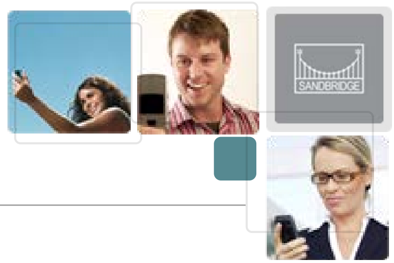
- Unique combination of SIMD vector, parallel reduction and RISC-based integer unit
- 4 hardware thread processing units per DSP – 150 MHz each
- 256KB internal memory, 32KB Instruction cache
- 16-way 16-bit SIMD vector unit and parallel reduction
- Special instructions for FFT, Viterbi, Turbo decoding, Galois field operations
- One DMA engine per thread capable of block, scatter, gather data transfer



Wireless LAN IEEE 802.11g

- Widely used standard for wireless local area networks
- Modes of operation and respective equalization algorithms
  - OFDM mode
    - Zero forcing equalizer in frequency domain
  - Direct Sequence Spread Spectrum mode – DSSS
    - No equalization necessary (not discussed further)
  - Complementary Code Keying mode – CCK
    - LMMSE equalizer
    - LMS equalizer
    - DFE equalizer
- Paper discusses equalization block implementations on SB3500

OFDM Mode Equalization
- Zero Forcing Equalizer



- Frame structure
  - Cyclic prefix transforms linear convolution into circular convolution
  - Cyclic prefix prevents ISI
- Baseband signal model

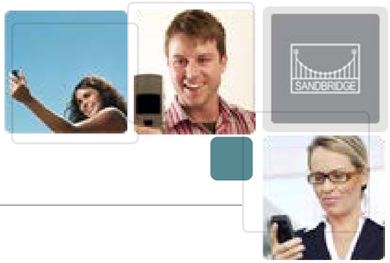
$$y_n = \sum_{l=0}^{L} h_l x_{n-l} + v_n, n = 0,1,2,\ldots$$

$$Y_f = H_f X_f + V_f$$

- Frequency domain zero forcing equalizer

$$Z_f = Y_f / H_f$$

OFDM Mode Receiver
- Implementation & Results



- 5 threads used for WLAN receiver operating at 54 Mbps.
- One thread performs CFO (carrier frequency offset) removal, FFT, channel equalization, de-mapping, de-interleaving

	Number of instructions/symbol (4usec)	MHz
CFO	20	5.00
FFT	90	22.50
Channel equalization	13	3.25
De-mapping	100	25.00
Total	223	55.75

- De-interleaver implemented using scatter DMA, operates in background

CCK Mode Equalization
- LMMSE Equalizer

- LMMSE Equalizer uses preamble to compute linear filter coefficients and then filters the data symbols to reduce the effect of ISI
- Vector form of the baseband signal:

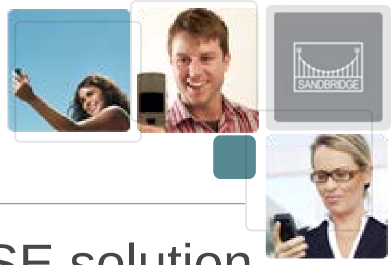
$$\vec{y} = \vec{H}\vec{x} + \vec{v} \qquad \vec{H} = \begin{pmatrix} h_0 & h_1 & \cdots & h_L & & & 0 \\ & h_0 & h_1 & \cdots & h_L & & \\ & & \ddots & & & \ddots & \\ 0 & & & h_0 & h_1 & \cdots & h_L \end{pmatrix}$$

- LMMSE filter model

$$\vec{w}_{\mathrm{LMMSE}} = \arg\min_{w} E\{\|\vec{w}^H \vec{y} - x_n\|\} = (\vec{H}\vec{H}^H + \sigma^2 \vec{I})^{-1} \vec{h}_a$$

- Matrix inversion performed once every frame

CCK Mode Equalization
- LMS Equalizer

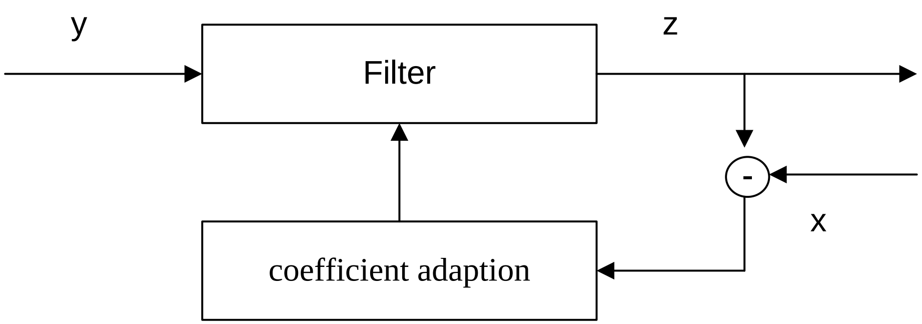


- Uses stochastic gradient algorithm to approximate MMSE solution
- Filter output

$$z_n = \vec{y}^T(n)\vec{w}(n)$$

- Error estimation in adaptation block

$$e_n = x_n - z_n$$

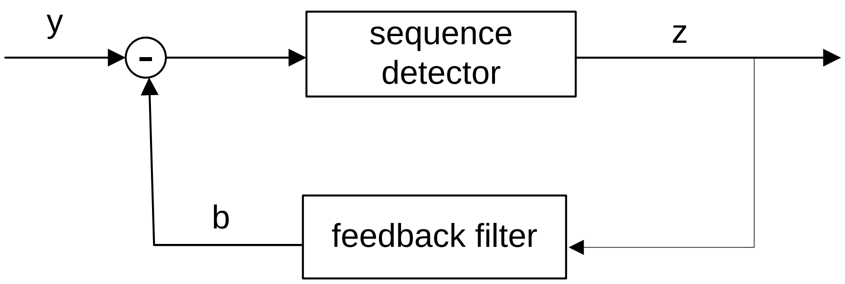


- Coefficient adaptation

$$\vec{w}(n+1) = \vec{w}(n) - \mu e_n \vec{y}(n)$$

CCK Mode Equalization - DFE Equalizer

- Non-linear equalizer removes ISI caused by preceding symbols

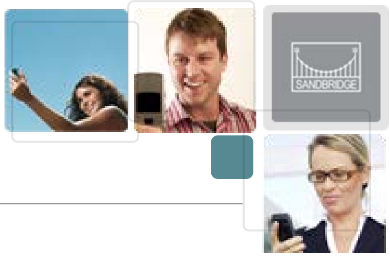


- Sequence detector detects one CCK symbol
- Feedback filter reconstructs ISI of the preceding symbols

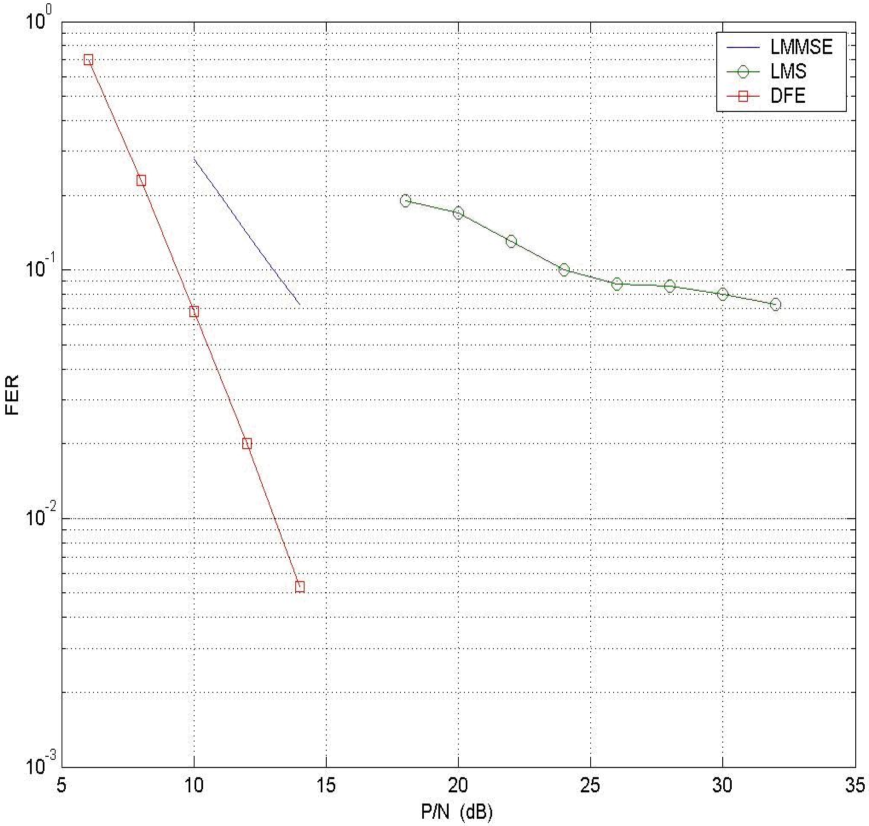
$$b_{k+1} = \sum_{i=1}^{k} z_{k-i} h_{i+1}$$

- Reconstructed ISI removed from received signal before detector

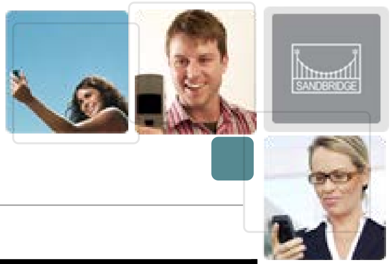
CCK Mode Equalization - Performance Comparison



- Performance of equalizers at data rate of 11 Mbps
- Channel delay profile of 50ns RMS delay
- Convergence of LMS varies with channel conditions



CCK Mode Equalization
- Implementation & Results

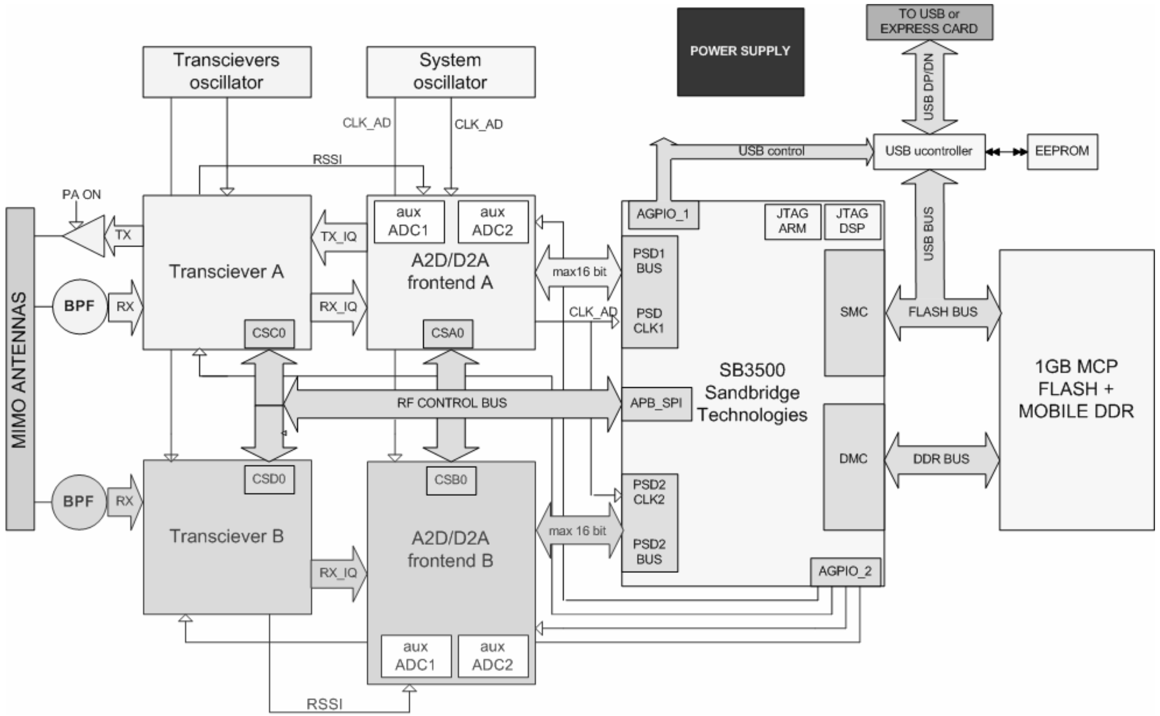


	Number of threads	MHz
LMS	Less than 1 SB3500 thread	56.37
LMMSE	Less than 1 SB3500 thread	56.37*
DFE	Less than 1 SB3500 threads	123.00

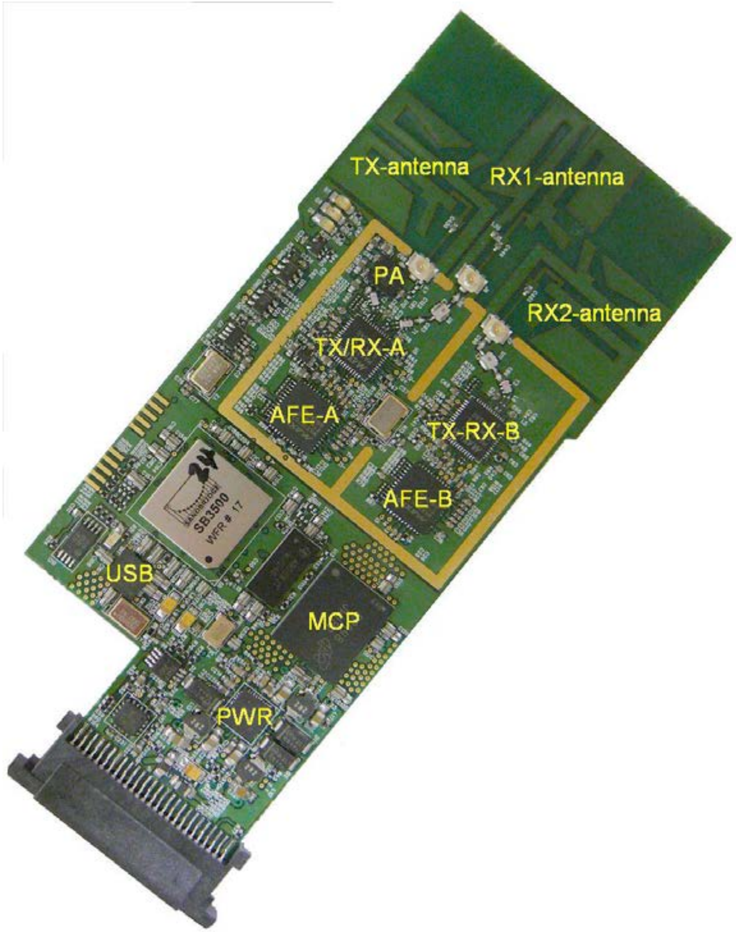
* Computation of LMMSE equalizer coefficients require a 16 x 16 matrix inversion once every frame during preamble and header symbols. (it includes FIR only)

- Overhead of matrix inversion for LMMSE coefficient computation is 537 MHz (requires approx 1 SB3500 DSP core). Needs to be performed only once every frame
- DFE equalizer numbers contain the CCK demodulation

SDR Platform



PCI-E CARD


TX-antenna
RX1-antenna
PA
RX2-antenna
TX/RX-A
AFE-A
TX-RX-B
AFE-B
SB3500
USB
MCP
PWR

Conclusions

- Discussed different IEEE 802.11g equalizer implementations on the Sandblaster SB3500
- IEEE 802.11g physical layer can be implemented with four SB3500 DSP threads (33% utilization on SB3500 chip) for CCK mode
- IEEE 802.11g physical layer can be implemented with five SB3500 DSP threads (42% utilization on SB3500 chip) for OFDM mode
- SB3500 suitable for implementing multi-mode receiver