IMPLEMENTATION OF A 2-FSK CONTINUOUS WAVEFORM USING A SOFTWARE DEFINED RADIO PLATFORM

Departamento de Señales, Sistemas y Radiocomunicaciones

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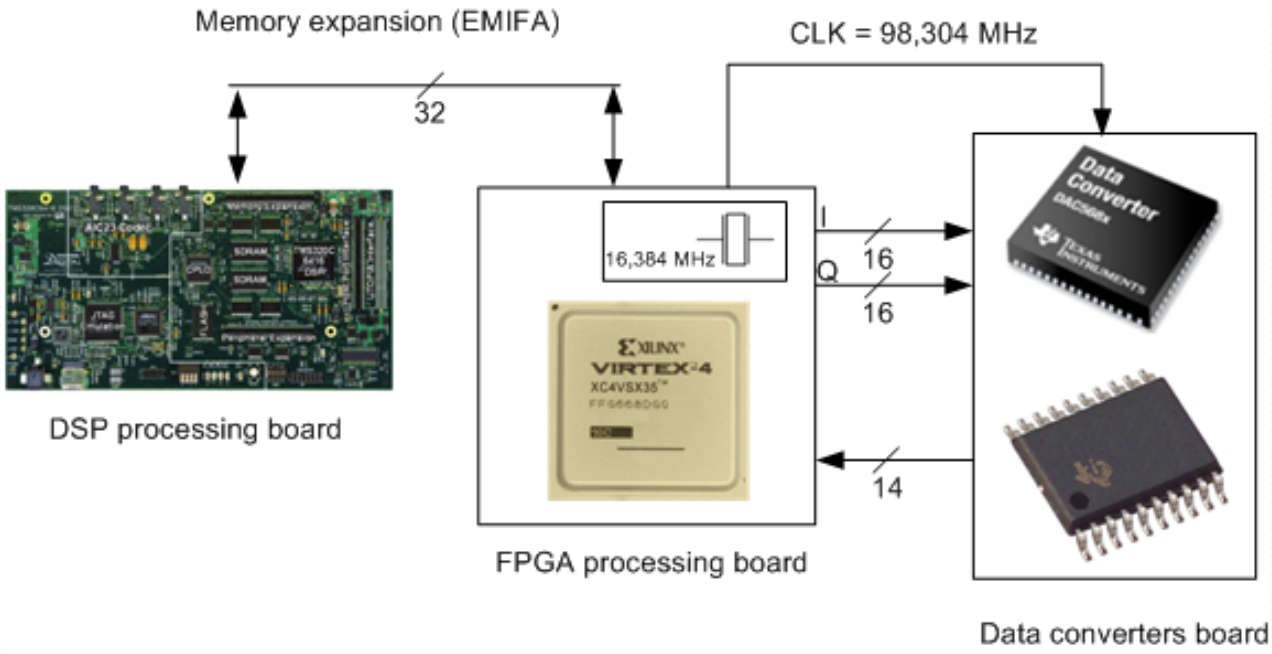
Grupo de Tratamiento Digital de Señales en Comunicaciones

OUTLINE

- SDR Platform Devices
  - DSP
  - FPGA
  - Data Converters
- Transmitter
  - Binary Processing
  - Digital Baseband Modulator
  - Up Conversion
- Receiver
  - Down Conversion
  - Digital Baseband Demodulator
  - Binary Processing
- Conclusions

SDR PLATFORM DEVICES (I)

SDR Platform architecture.



SDR PLATFORM DEVICES (II)

Digital Signal Processor (DSP).

TEXAS INSTRUMENTS

- Texas Instruments
- TMS320C6416T-1000
- Fixed Point DSP
- Frequency 1 GHz
- Peak MMACS 8000
- 2 External Memory Interface (EMIF)
  - EMIF A @ 64 Bits
  - EMIF B @ 16 Bits
- HPI, McBSP Buses.
- Enhanced DMA.
- VCP (Viterbi Co-Processor)

	TMS320C6416T-1000
CPU	1 C64x
Peak MMACS	8000
Frequency(MHz)	1000
On-Chip L1/SRAM	32 KB
On-Chip L2/SRAM	1024 KB
EMIF	1 16-Bit,1 64-Bit
External Memory Type Supported	Async SRAM,SDRAM,SBSRAM
DMA	64-Ch EDMA
PCI	1 32-Bit
HPI	1 32/16-Bit
UTOPIA	1
McBSP	3
Trace Enabled	Yes
Timers	3 32-Bit GP
Hardware Accelerators	VCP,TCP
Core Supply (Volts)	1.2 V
IO Supply (Volts)	3.3 V
Operating Temperature Range (°C)	0 to 90

SDR PLATFORM DEVICES (III)

FPGA.

- Xilinx FPGA Virtex-4 XC4VSX35-10

Xilinx Virtex-4 Family FPGAs

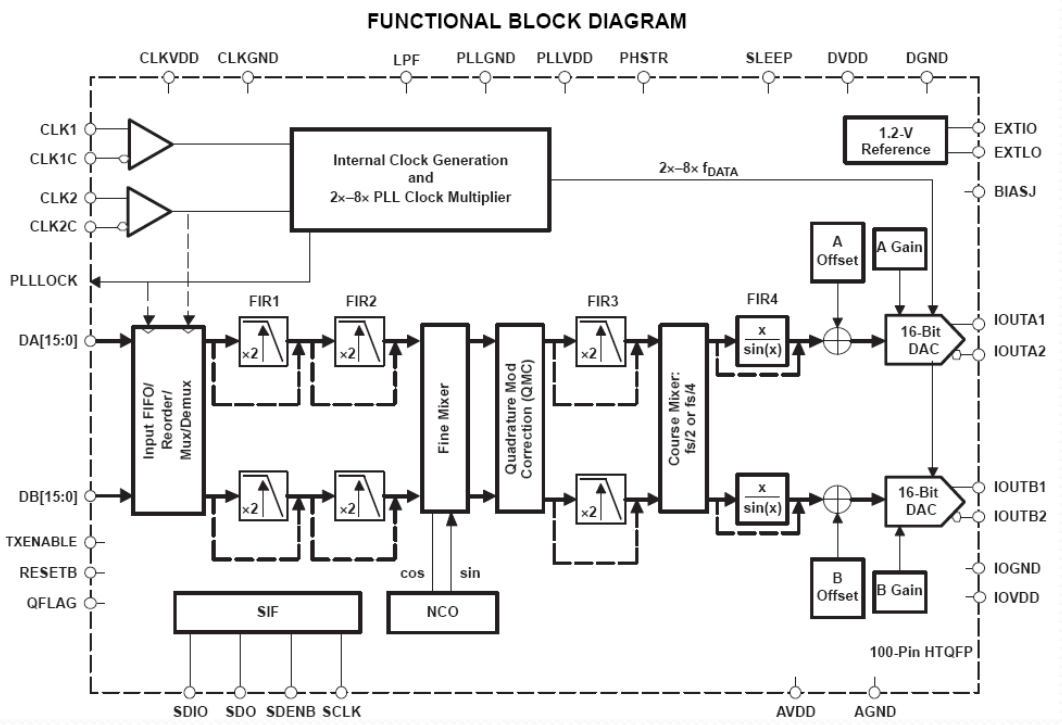
		Virtex-4 LX (Logic)						
		XC4VLX15	XC4VLX25	XC4VLX40	XC4VLX60	XC4VLX80	XC4VLX100	XC4V
CLB Resources	CLB Array (Row x Column)	64 x 24	96 x 28	128 x 36	128 x 52	160 x 56	192 x 64	192
	Slices	6,144	10,752	18,432	26,624	35,840	49,152	67
	Logic Cells	13,824	24,192	41,472	59,904	80,640	110,592	152
	CLB Flip Flops	12,288	21,504	36,864	53,248	71,680	98,304	135
Memory Resources	Max. Distributed RAM Bits	98,304	172,032	294,912	425,984	573,440	786,432	1,08
	Block RAM/FIFO w/ECC (18 kbits each)	48	72	96	160	200	240	2
	Total Block RAM (kbits)	864	1,296	1,728	2,880	3,600	4,320	5,4
Clock Resources	Digital Clock Managers (DCM)	4	8	8	8	12	12	
	Phase-matched Clock Dividers (PMCD)	0	4	4	4	8	8	
I/O Resources	Max Select I/O™	320	448	640	640	768	960	9
	Total I/O Banks	9	11	13	13	15	17	
	Digitally Controlled Impedence	Yes	Yes	Yes	Yes	Yes	Yes	Y
	Max Differential I/O Pairs	160	224	320	320	384	480	4
	I/O Standards	LDT-25, LVDS-25, LVDSEXT-25, BLVDS-25, ULVDS-25, LVPECL-25, LVCMOS25, LVCMOS18, LVCMOS15, PCI						
DSP Resources	XtremeDSP™ Slices	32	48	64	64	80	96	
Embedded Hard IP Resources	PowerPC™ Processor Blocks	—	—	—	—	—	—	
	10/100/1000 Ethernet MAC Blocks	—	—	—	—	—	—	
	RocketIO™ Serial Transceivers	—	—	—	—	—	—	
Speed Grades	Commercial (slowest to fastest)	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -
	Industrial (slowest to fastest)	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-1
	Configuration Memory Bits	4,765,568	7,819,904	12,259,712	17,717,632	23,291,008	30,711,680	40,3
	EasyPath™ Cost Reduction Solutions[1]	—	XCE4VLX25	XCE4VLX40	XCE4VLX60	XCE4VLX80	XCE4VLX100	XCE4

		Virtex-4 SX (Signal Processing)		
		XC4VSX25	XC4VSX35	XC4VSX55
CLB Resources	CLB Array (Row x Column)	64 x 40	96 x 40	128 x 48
	Slices	10,240	15,360	24,576
	Logic Cells	23,040	34,560	55,296
	CLB Flip Flops	20,480	30,720	49,152
Memory Resources	Max. Distributed RAM Bits	163,840	245,760	393,216
	Block RAM/FIFO w/ECC (18 kbits each)	128	192	320
	Total Block RAM (kbits)	2,304	3,456	5,760
Clock Resources	Digital Clock Managers (DCM)	4	8	8
	Phase-matched Clock Dividers (PMCD)	0	4	4
I/O Resources	Max Select I/O™	320	448	640
	Total I/O Banks	9	11	13
	Digitally Controlled Impedence	Yes	Yes	Yes
	Max Differential I/O Pairs	160	224	320
	I/O Standards	X, PCI66, GTL, GTL+, HSTL I (1	.5V,1.8V), HSTL II (1	
DSP Resources	XtremeDSP™ Slices	128	192	512
Embedded Hard IP Resources	PowerPC™ Processor Blocks	—	—	—
	10/100/1000 Ethernet MAC Blocks	—	—	—
	RocketIO™ Serial Transceivers	—	—	—
Speed Grades	Commercial (slowest to fastest)	-10, -11, -12	-10, -11, -12	-10, -11, -12
	Industrial (slowest to fastest)	-10, -11	-10, -11	-10, -11
	Configuration Memory Bits	9,147,648	13,700,288	22,745,216
	EasyPath™ Cost Reduction Solutions[1]	XCE4VSX25	XCE4VSX35	XCE4VSX55

SDR PLATFORM DEVICES (IV)

Digital to Analog Converter.

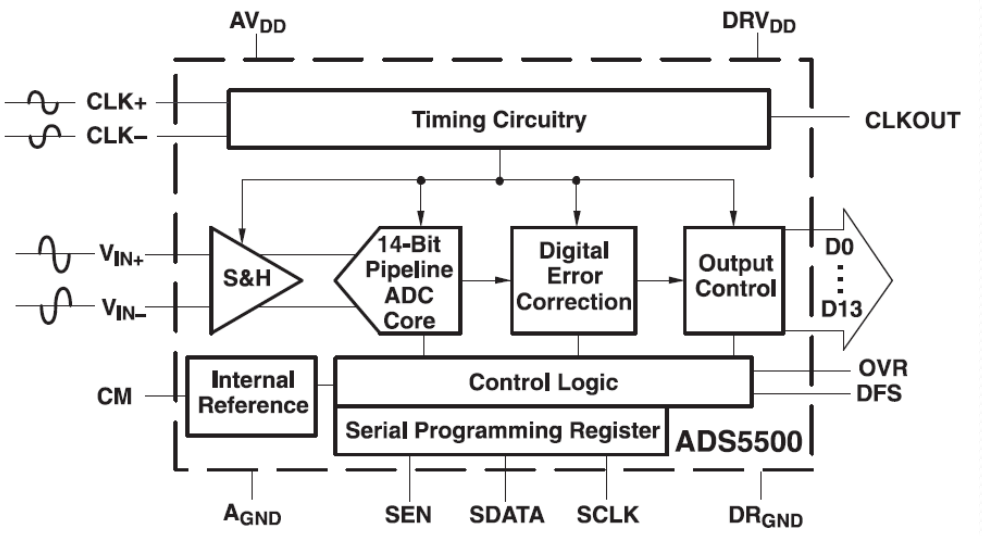
- Texas Instruments DAC5687.
- 16 bits dual-channel DAC.
- Sampling rate up to 500 MSPS.
- Interpolating from 2x to 8x.
- Mixer with 32-bits NCO.
- Quadrature Modulation Correction (QMC).
- Gain adjusting.
- *Sinc(x)*correction.
- Differential Clock signal.
- Differential Output signal.
- Serial Programming Interface (SPI)



SDR PLATFORM DEVICES (V)

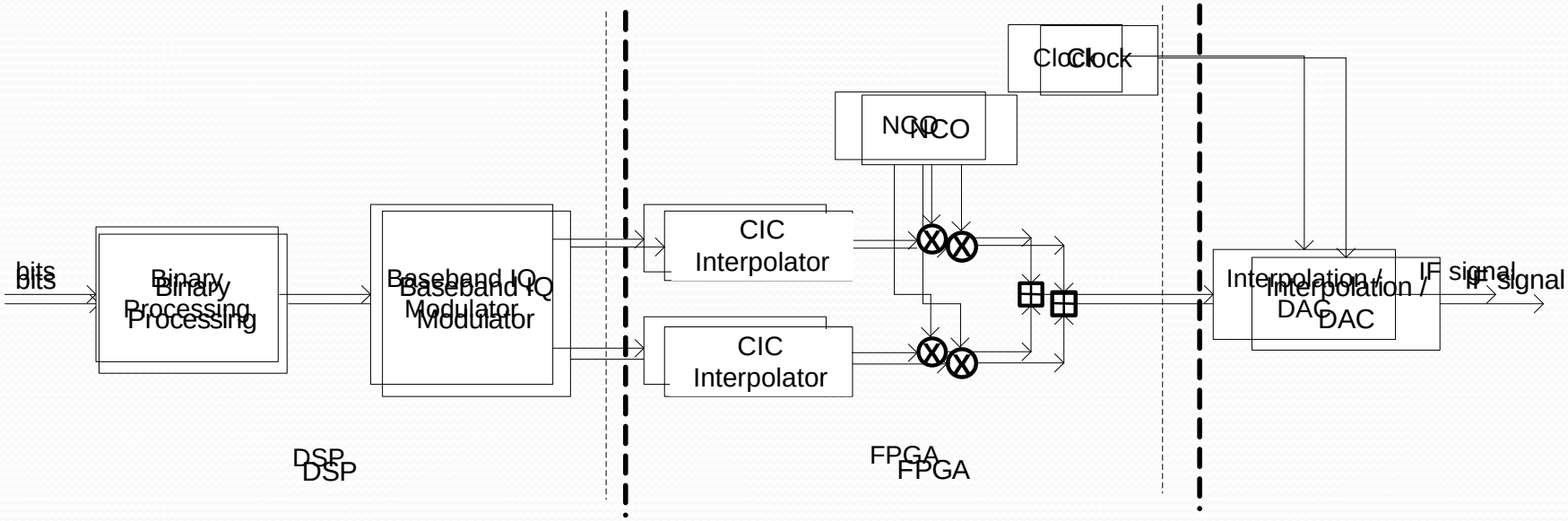
Analog to Digital Converter.

- Texas Instruments ADS5500.
- 14-bits pipeline single-channel ADC.
- Sampling Rate up to 125 MSPS.
- Two different data formats (straight binary and 2's complement).
- Two active edges (rising and falling).
- Differential Clock signal.
- Differential Input signal.
- Serial Programming Interface (SPI).



TRANSMITTER

Transmitter Diagram.



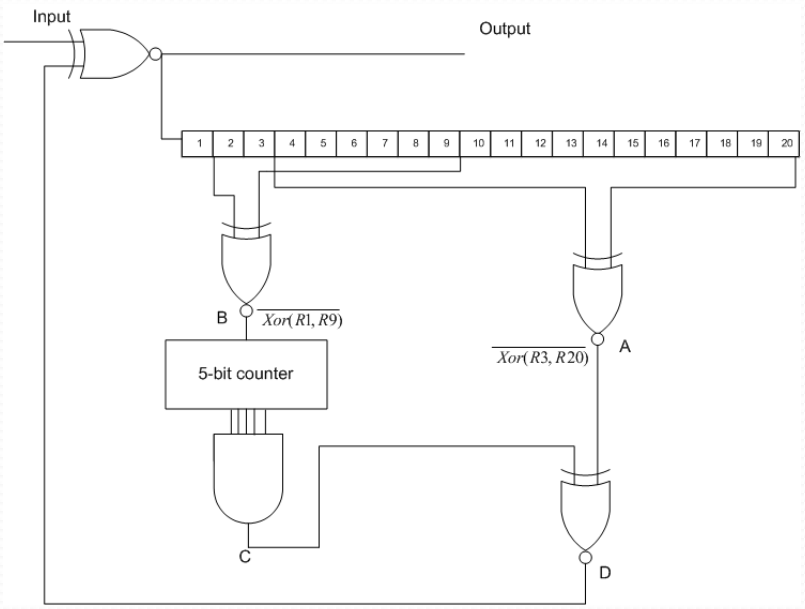
BINARY PROCESSING (I)

- Suitable processes for Binary Processing.
  - Source Coding
  - Encryption
  - Scrambling
  - Interleaving
  - Channel Coding
    - Block Coding
    - Convolutional Coding
  - Line Coding

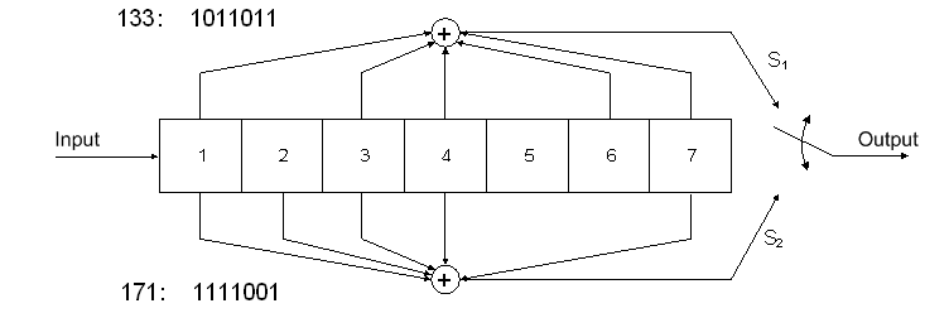
BINARY PROCESSING (II)

Binary Processing in the Transmitter.

- Performed in the DSP
  - Auto-synchronized Scrambler



- Performed in the VCP of the DSP
  - Convolutional Encoder (2,1,7)
    - 2 Output bits
    - 1 Input bit
    - 7 Number of Cells in the Shift Register or Constraint Length

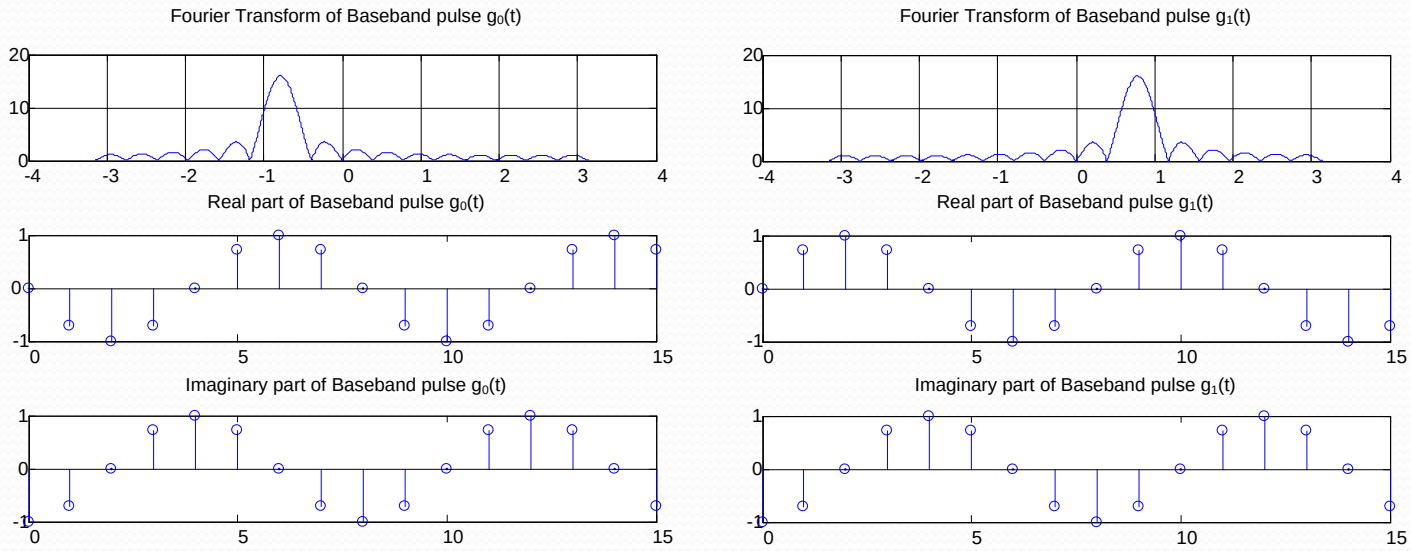


DIGITAL BASEBAND MODULATOR (I)

- 2-FSK Symbols in Time and Frequency domains.

$$g_0(t) = W(t) \cdot \exp\left(j \cdot \left((w_0 - w_c)t - \pi/2\right)\right)$$

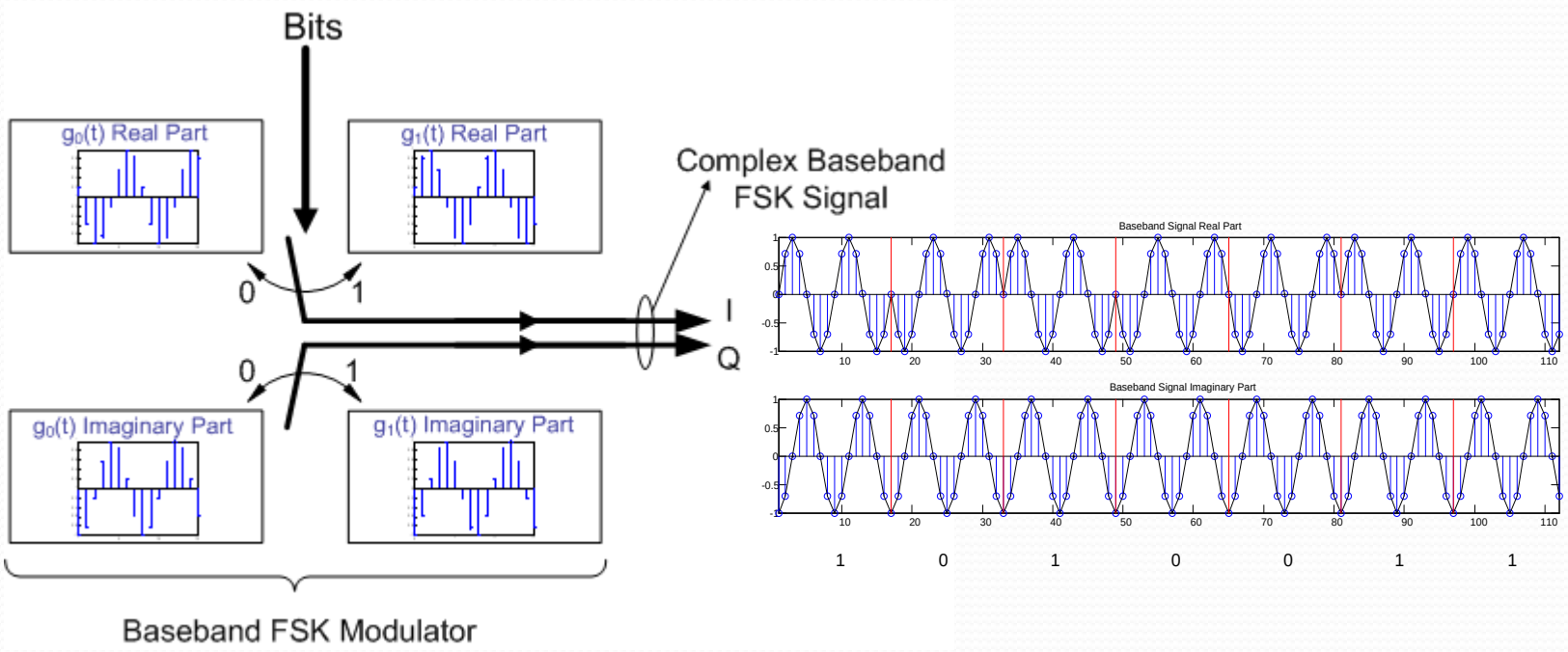
$$g_1(t) = W(t) \cdot \exp\left(j \cdot \left((w_1 - w_c)t - \pi/2\right)\right)$$



Matlab Simulation

DIGITAL BASEBAND MODULATOR (II)

- Generation of 2-FSK Symbols.



UP CONVERSION (I)

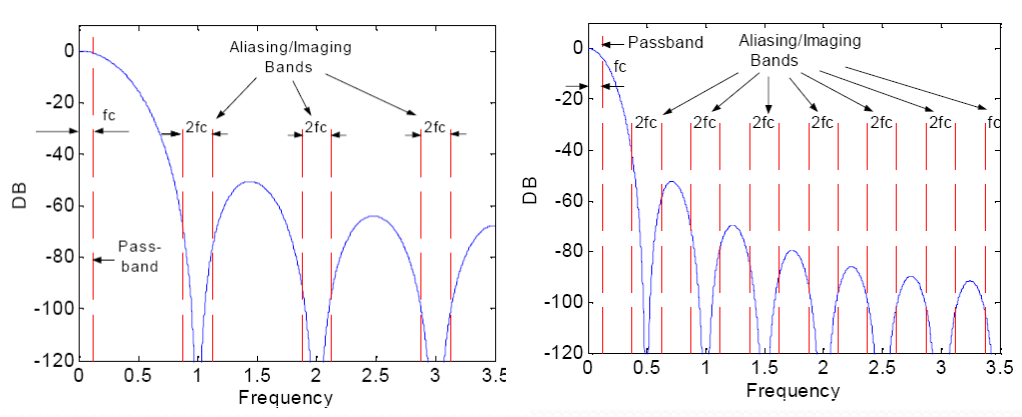
Interpolator CIC.

- Equations

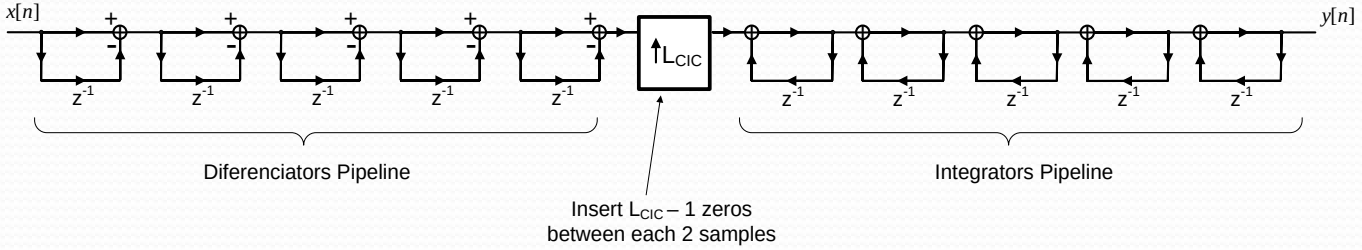
$$H(z)=\frac{\left(1-z^{-RM}\right)^N}{\left(1-z^{-1}\right)^N}=\left[\sum_{k=0}^{RM-1}z^{-k}\right]^N$$

$$H(z)=H_I(z)\cdot H_C(z)=\frac{\left(1-z^{-RM}\right)^N}{\left(1-z^{-1}\right)^N}=\frac{1}{\left(1-z^{-1}\right)^N}\cdot\left(1-z^{-RM}\right)^N$$

$$\left|H(f)\right|=\left[\frac{\sin(\pi MfT)}{\sin(\pi fT/R)}\right]^N\approx\left[RM\frac{\sin(\pi MfT)}{\pi MfT}\right]^N$$



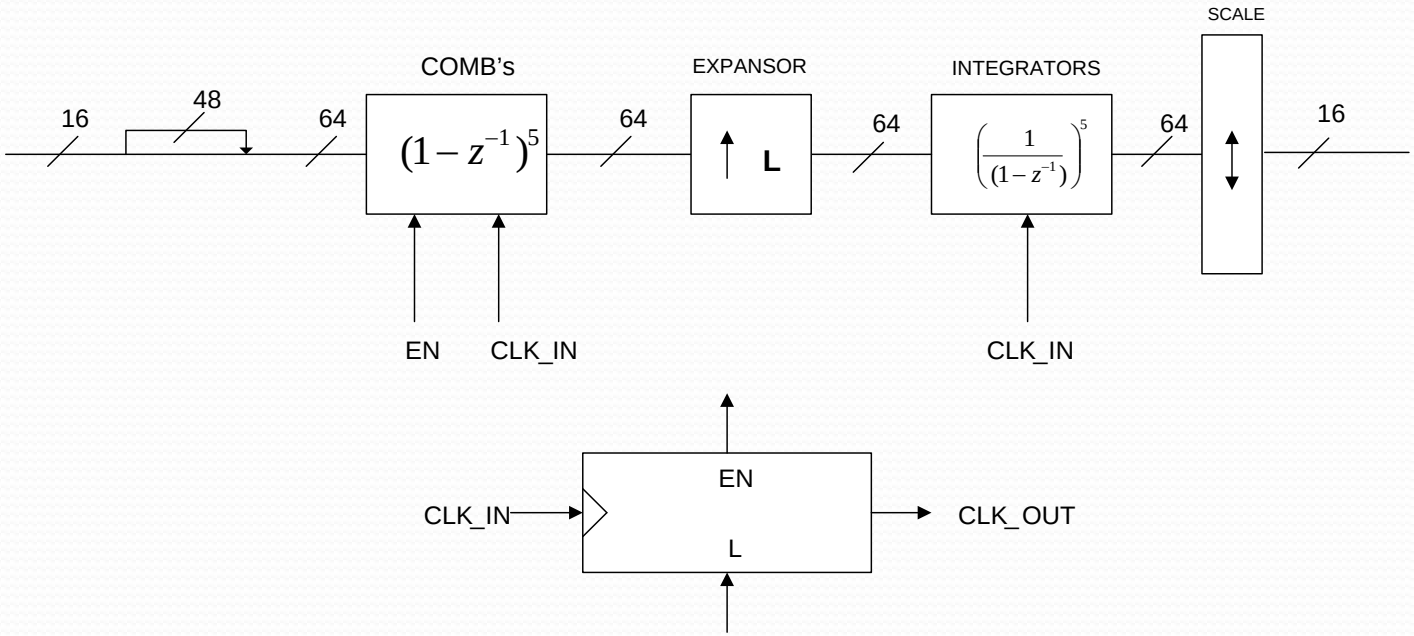
- Architecture.



UP CONVERSION (II)

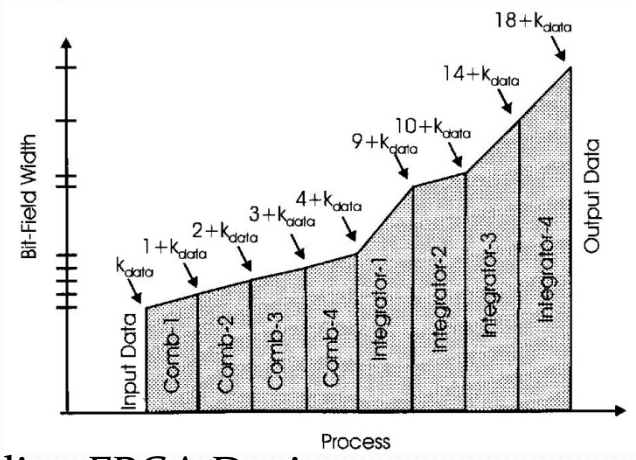
Interpolator CIC.

- Hardware Diagram.



UP CONVERSION (III)

Interpolator CIC.



- Precision & Datapath
  - Differentiators
    - Linear increasing
  - Integrators

$$B_{OUT} = \lceil B_{IN} + N \cdot \log_2(R) \rceil$$

- Hardware Resources in XC4VSX35-10 Xilinx FPGA Device

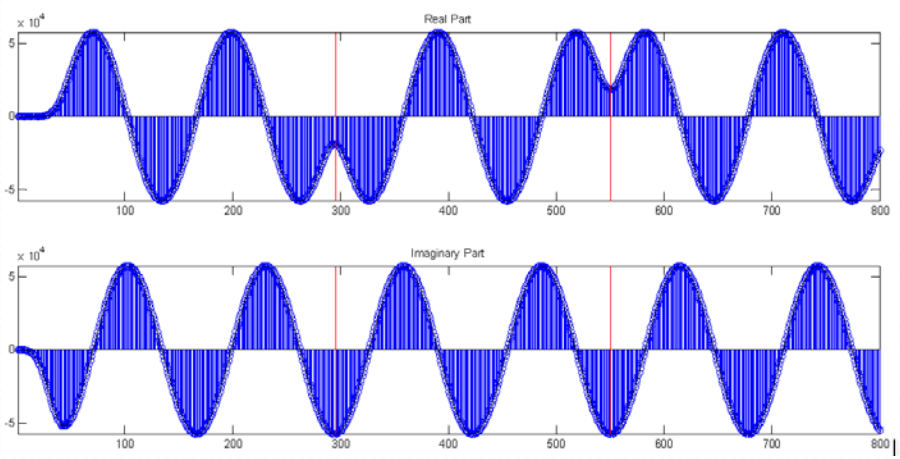
Device Utilization Summary		
Slices	2293 out of 15360	14%
Flip Flops	2070 out of 30720	6%
4 Input LUTs	3140 out of 30720	10%
IOBs	140 out of 448	31%
GCLKs	1 out of 32	3%

Timing Summary	
Minimum period	6.435 ns
Maximum frequency	155.412 MHz
Minimum input arrival time before clock	7.350 ns
Maximum output required time after clock	7.358 ns
Maximum combinational path delay	7.906 ns

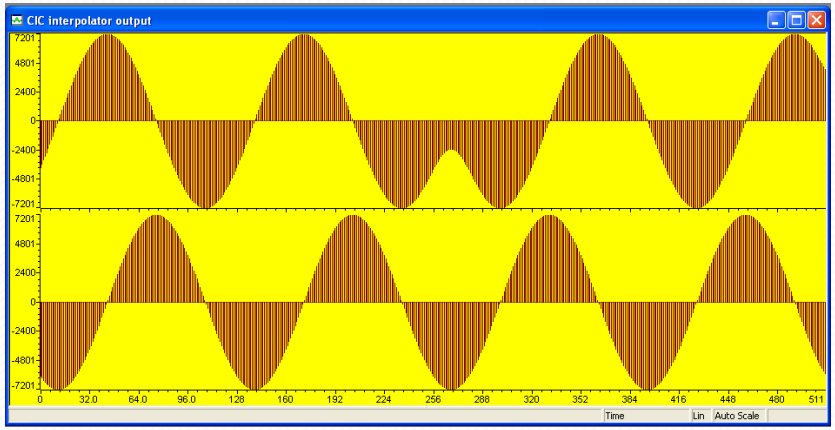
UP CONVERSION (IV)

Interpolator CIC.

- Graphical comparison between real and theoretical results.



Matlab Simulation

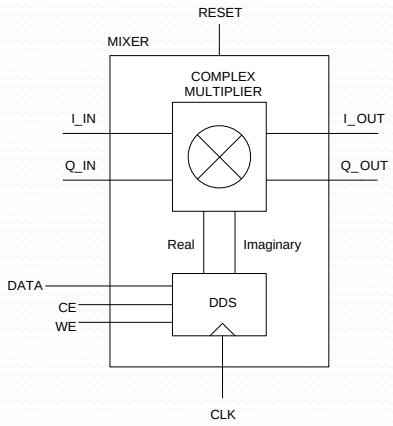


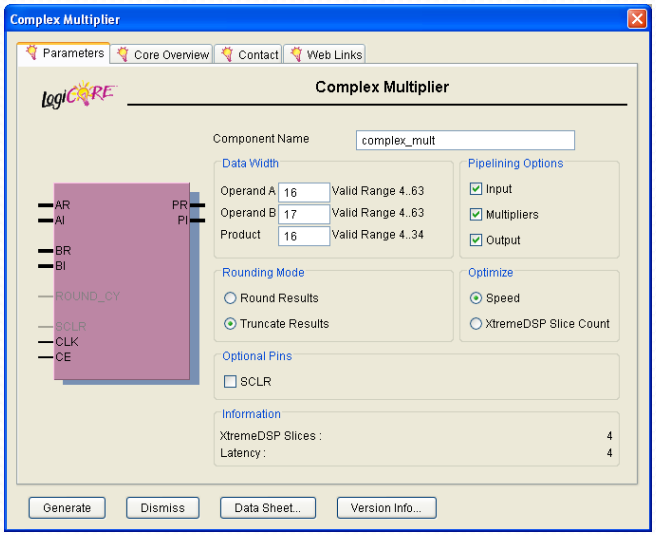
Code Composer Studio graph of a real-time execution

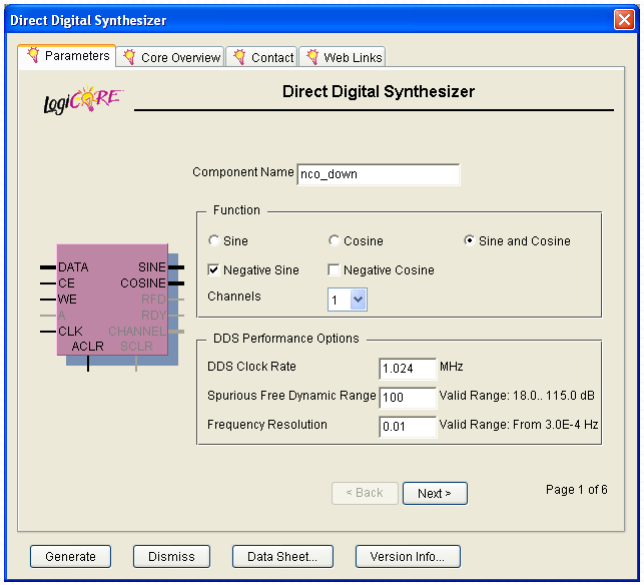
UP CONVERSION (V)

Mixer.

- Architecture.







- Hardware Resources.

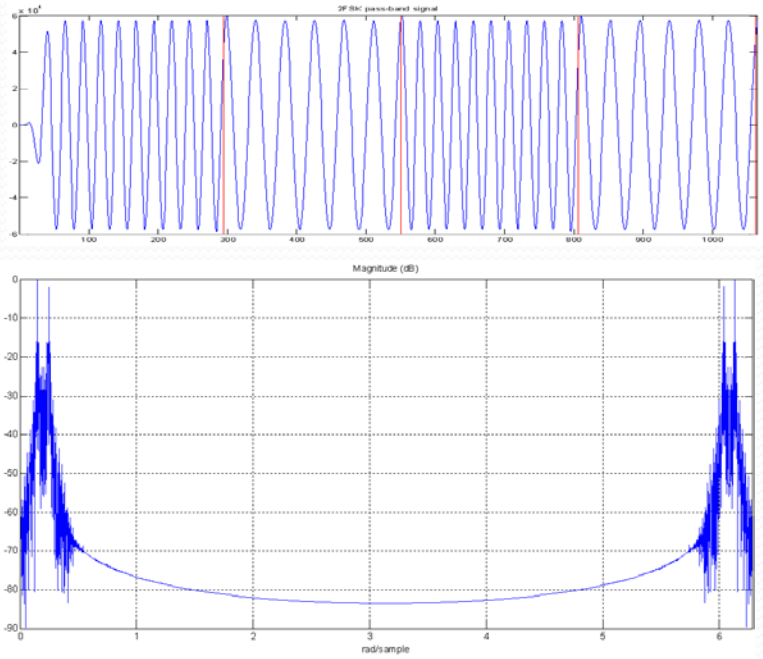
Device Utilization Summary		
Slices	167 out of 15360	1%
Flip Flops	266 out of 30720	0%
4 Input LUTs	193 out of 30720	0%
IOBs	95 out of 448	21%
FIFO16 / RAMB16	8 out of 192	4%
GCLKs	1 out of 32	3%
DSP48s	4 out of 192	2%

Timing Summary	
Minimum period	4.214 ns
Maximum frequency	237.290 MHz
Minimum input arrival time before clock	5.541 ns
Maximum output required time after clock	5.280 ns
Maximum combinational path delay	No path found

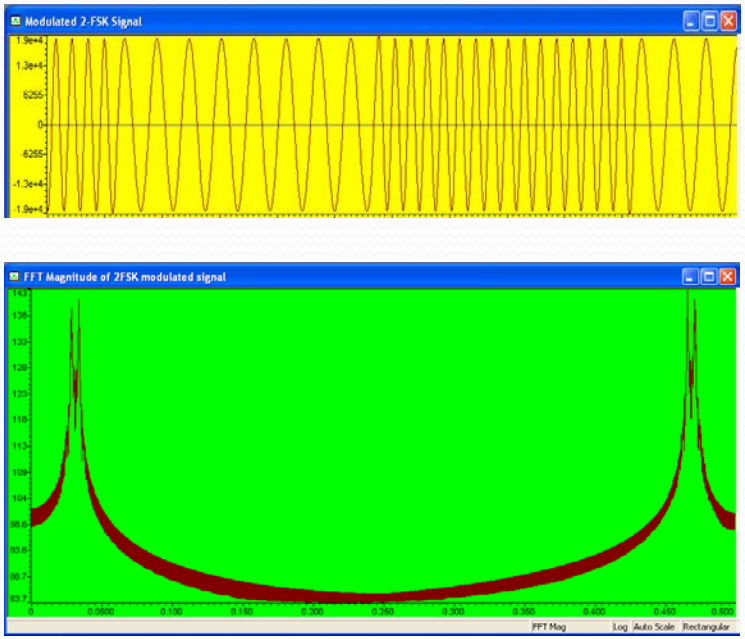
UP CONVERSION (VI)

Mixer.

- Comparison between real and theoretical results.



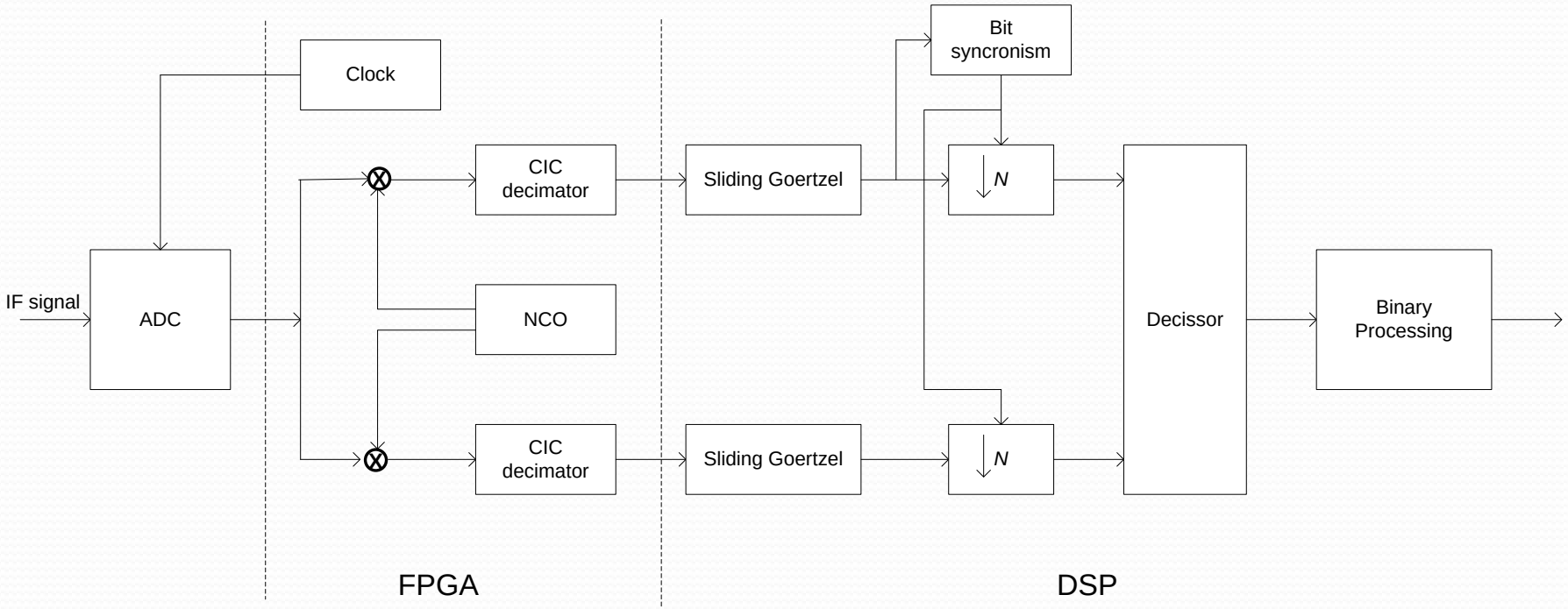
Matlab Simulation



Code Composer Studio graph of a real-time execution

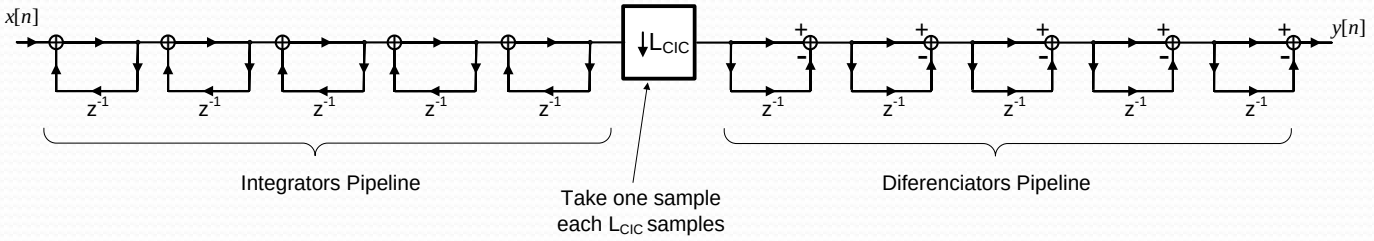
RECEIVER

Receiver Diagram.

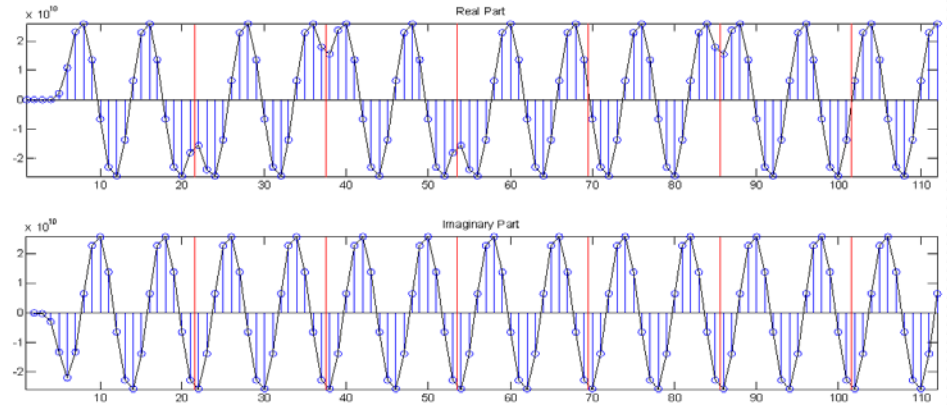


DOWN CONVERSION

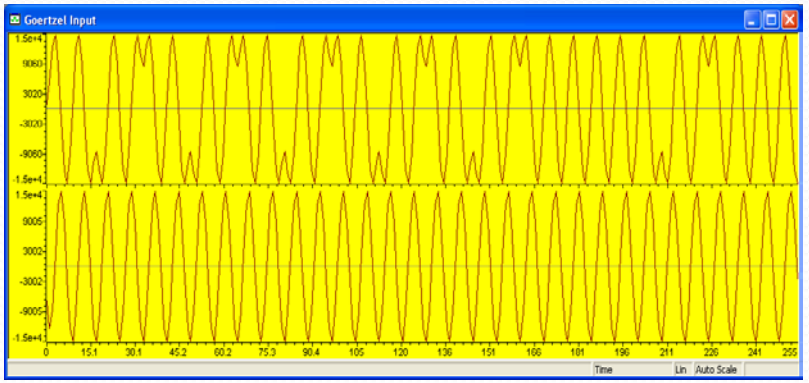
Mixer and Decimator CIC.



Graphical comparison between real and theoretical results.



Matlab Simulation

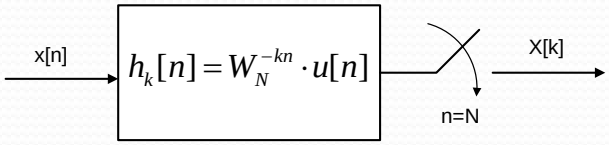


Code Composer Studio graph of a real-time execution

DIGITAL BASEBAND DEMODULATOR (I)

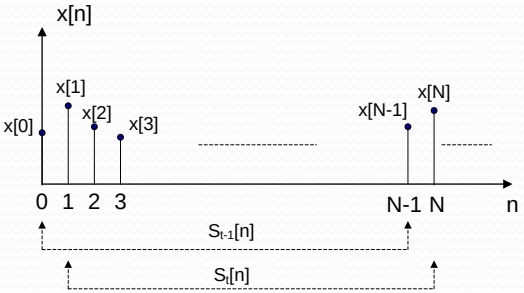
Digital Baseband Demodulator.

- Goertzel Algorithm. (One filter for each frequency)

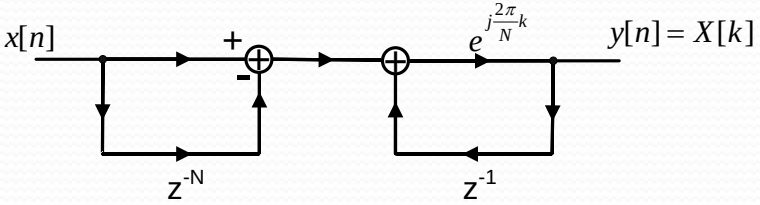


$$W_N = e^{-j\frac{2\pi}{N}}$$

- Sliding Goertzel Algorithm.



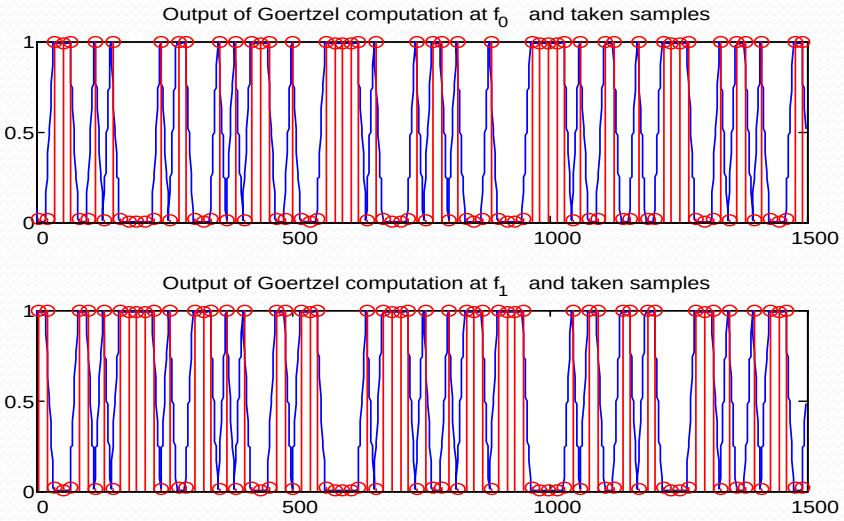
$$S_t[K] = e^{j\frac{2\pi}{N}K} \cdot \left(S_{t-1}[K] + x[N] - x[0]\right)$$



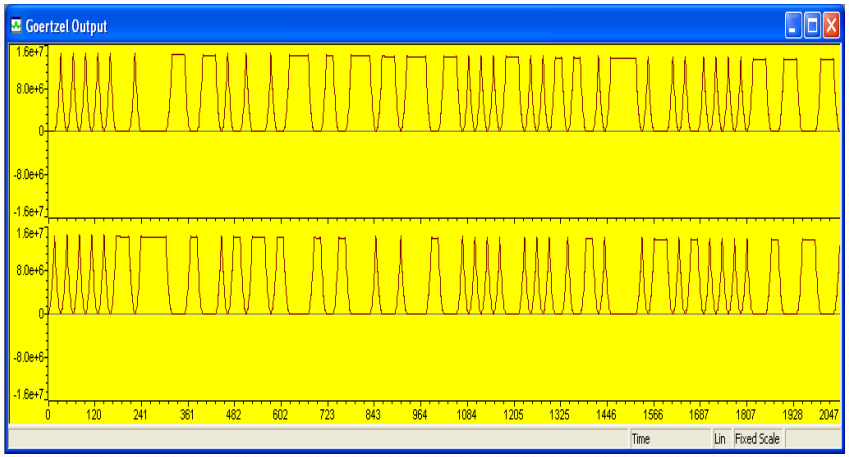
DIGITAL BASEBAND DEMODULATOR (II)

Goertzel Algorithm.

- Comparison between real and theoretical results.



Matlab Simulation

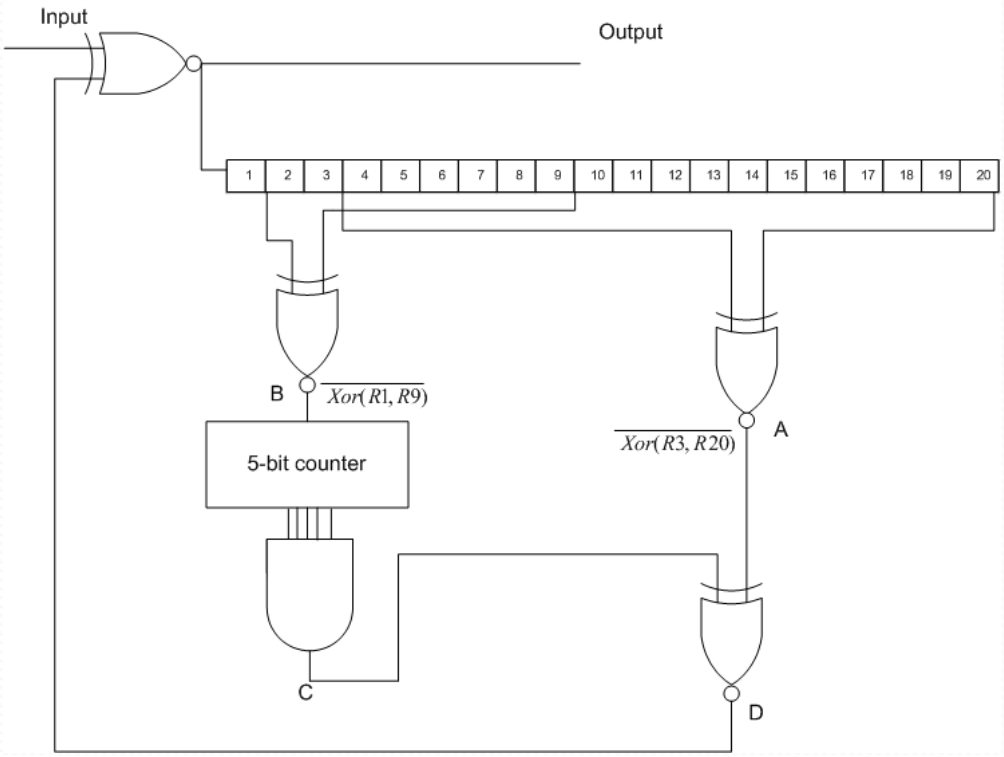


Code Composer Studio graph of a real -time execution

BINARY PROCESSING (III)

Binary Processing in the Receiver.

- Performed in the DSP
- Binary Processing at the Down Channel
  - Auto-synchronized Descrambler
  - Viterbi Convolutional Decoder, based on the Viterbi Coprocessor of the DSP



CONCLUSIONS

- Proposal of a design and implementation of a 2-FSK continuous waveform.
- Based on Software Defined Radio design.
- Software Defined Radio Concept: " Place data converters as close as possible to the antenna"
- Modular architecture
- Other possibilities
  - Tradeoff between complexity and hardware utilization
- Comparison between theoretical results and the real time results we achieved.