

An Embedded Controlled Flexible Baseband Processing Approach



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Agenda

1. General Flexible Base Station Architecture
2. Flexible Baseband Architecture
3. Control Application
4. System on a Programmable Chip
5. Flexible Baseband Processing
6. Performance Analysis

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General Flexible Base Station Architecture



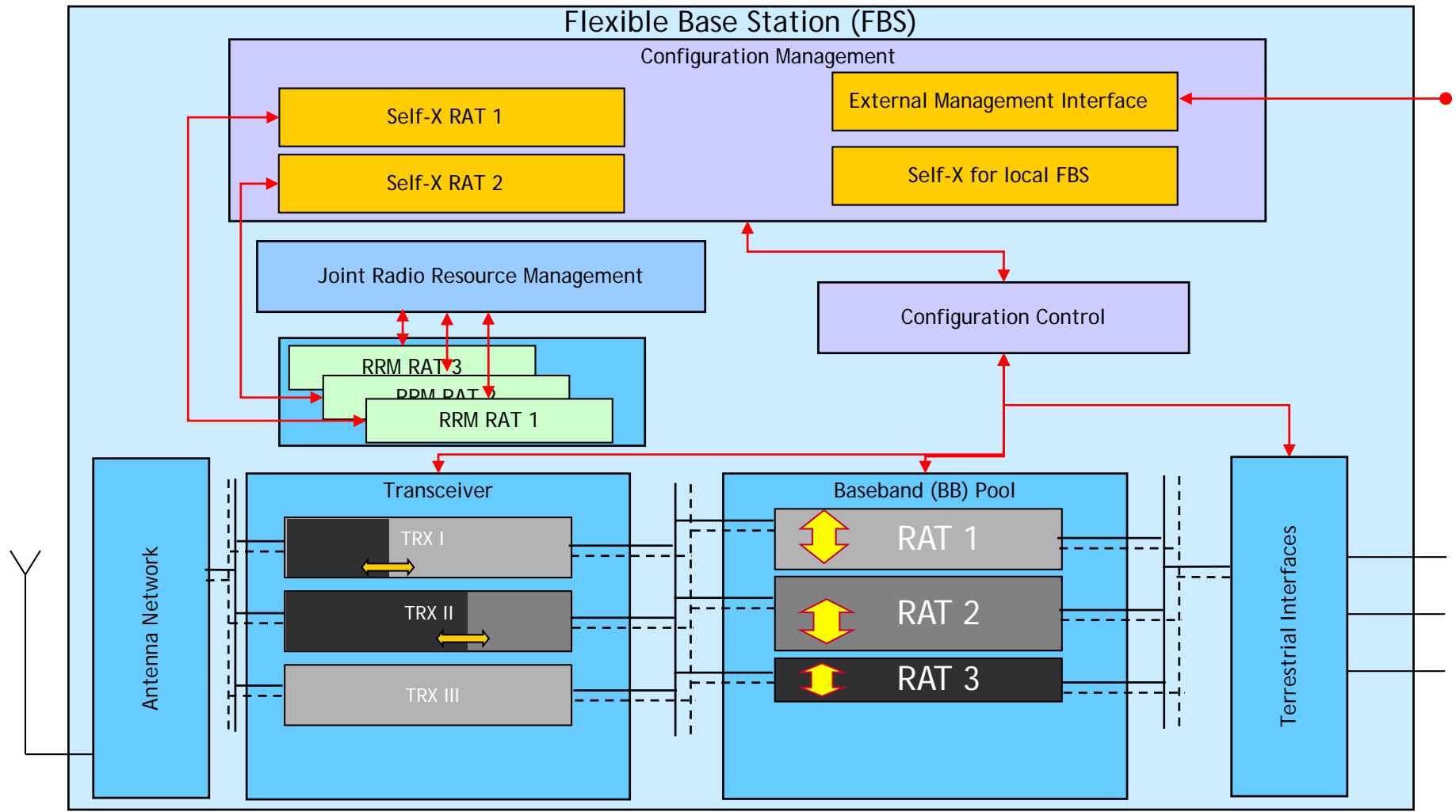
What is a Flexible Base Station (FBS)?

What are the key elements of such FBS?

Flexible Base Station Architecture

- Multi-standard Transceiver
- Flexible baseband processing
- Multiple radio-standard processing chains
 - Universal Mobile Telecommunication System (UMTS)
 - Long Term Evolution (LTE)
- Dynamic load balancing between these standards
- Simple extension of the Radio Access Technology (RAT)
- Flexible assembly of radio functional modules

Flexible Base Station Architecture



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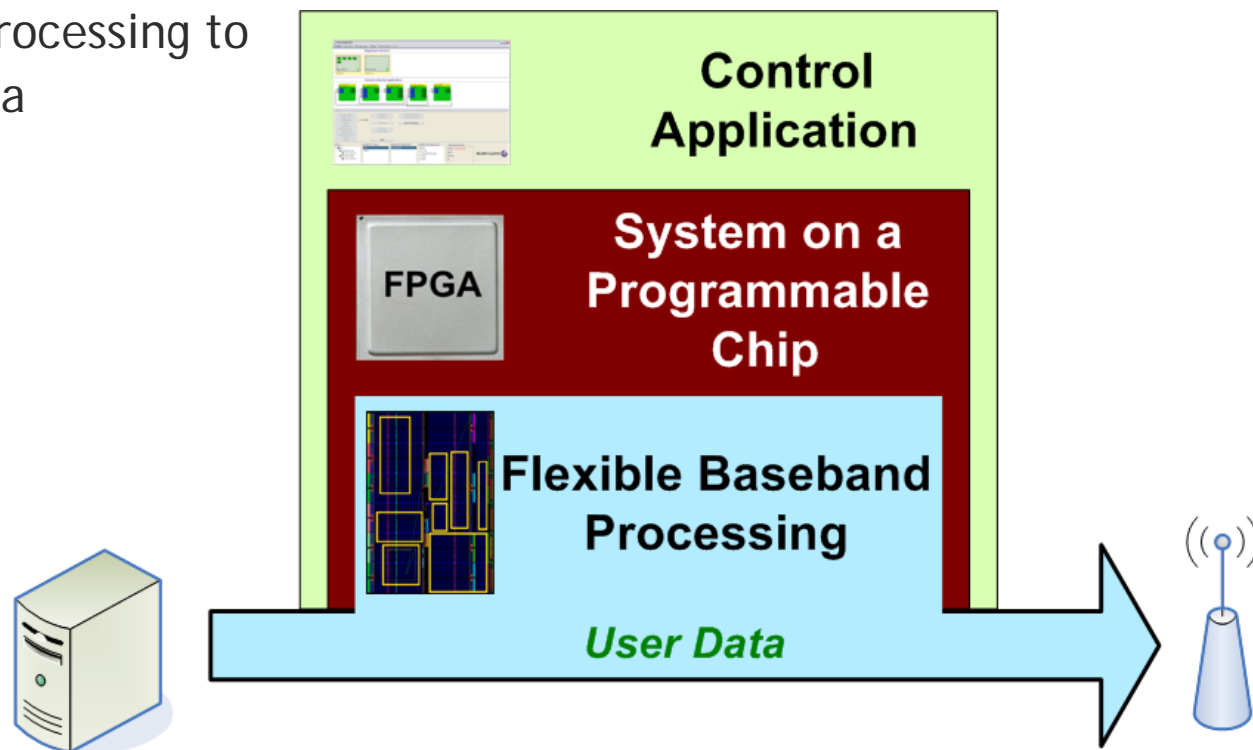
Flexible Baseband Architecture



What are the key elements of the flexible baseband?

Flexible Baseband

- Control Application to establish the communication with management modules
- Embedded system on a Field Programmable Gate Array (FPGA), so called System on a Programmable Chip (SoPC), to control the re-configuration
- Flexible baseband processing to process the user data



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Control Application



What is the Control Application?

What are the tasks of the Control Application?

Control Application

- Interface between different management modules and different flexible baseband boards
- Supports Object Management Group (OMG) commands
- Direct control and monitoring of the flexible baseband boards
- Easy and detailed setup of the baseband processing chain
 - Allocate Capacity, SendSegment, Execute, Start, Stop, Release etc.
- Gives an overview about all running RATs and all possible RATs

Control Application

The screenshot displays the 'Control Application' window with the following sections:

- Registered devices:** Shows two device groups. The first group, labeled 'ML505 (1)', contains five modules (M1, M2, M3, M4, M5) and a component '505_LX50T (1)'. The second group, labeled 'ML507 (2)', contains a component '507_FX70T (2)'. Both groups have a green status indicator.
- Current selected application:** A flow diagram showing five modules in a sequence: M6: CRC 16a, M7: TB Segmentation, M8: Turbo Encoder, M9: Rate Matching, and M10: QPSK. Each module is labeled 'Running' and contains a grid of numbers representing data paths. Arrows indicate the flow from M6 to M7, M7 to M8, M8 to M9, and M9 to M10.
- Control Buttons:** A set of buttons for managing the application, including 'Allocate Capacity', 'Initiate Load', 'SendSegment', 'Execute', 'Initialize', 'GetProvidedPorts', 'ConnectPort', 'ConnectExternalPort', 'Configure', 'Start', 'DeAllocate', 'UnLoad', 'Terminate', 'Release', 'Disconnect', 'Stop', 'Start automatic load', 'Stop automatic load', and 'Reload ConfigFiles'. There is also an 'overwrite' checkbox.
- Bottom Panel:** Contains four panels: 'Devices' (listing PC, ML505 (1) [1/1], 505_LX50T (1), ML507 (2) [0/1], and 507_FX70T (2)), 'Available RAT Types' (listing LTE and UMTS), 'Deployed RAT Applications' (listing LTE (default)), and 'Available Reconfigurations' (listing default, CRC 24a, Convolutional Encoder, 16 QAM, and 64 QAM). To the right is a 'Management Agent' section with fields for Status (not connected), Name, Address, and IP.

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System on a Programmable Chip

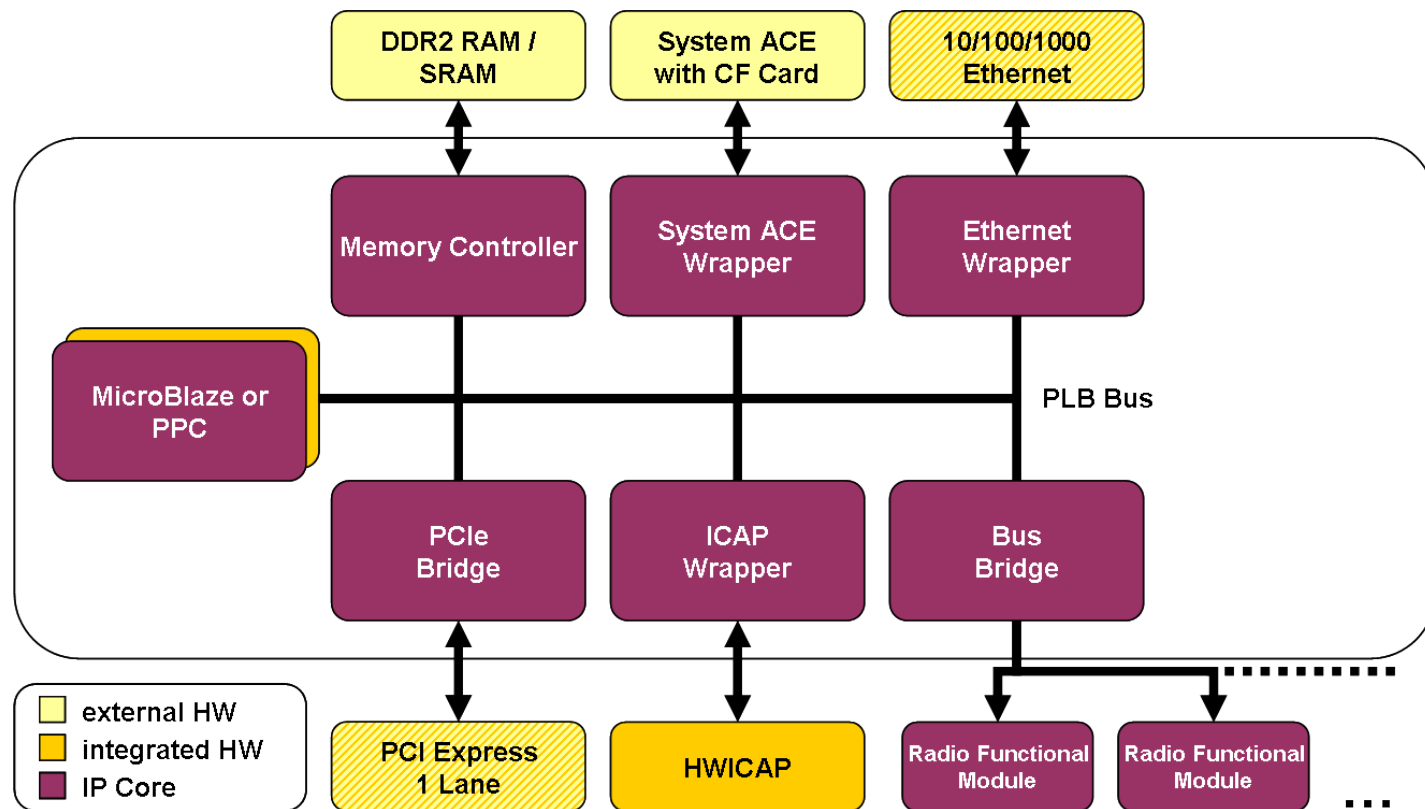


Why we need such a system?

What is the architecture of this system?

System on a Programmable Chip

- Major element for the flexibility and serviceability of the flexible baseband processing (FBP)
- Interface to the outside, e. g. to the Control Application



System on a Programmable Chip

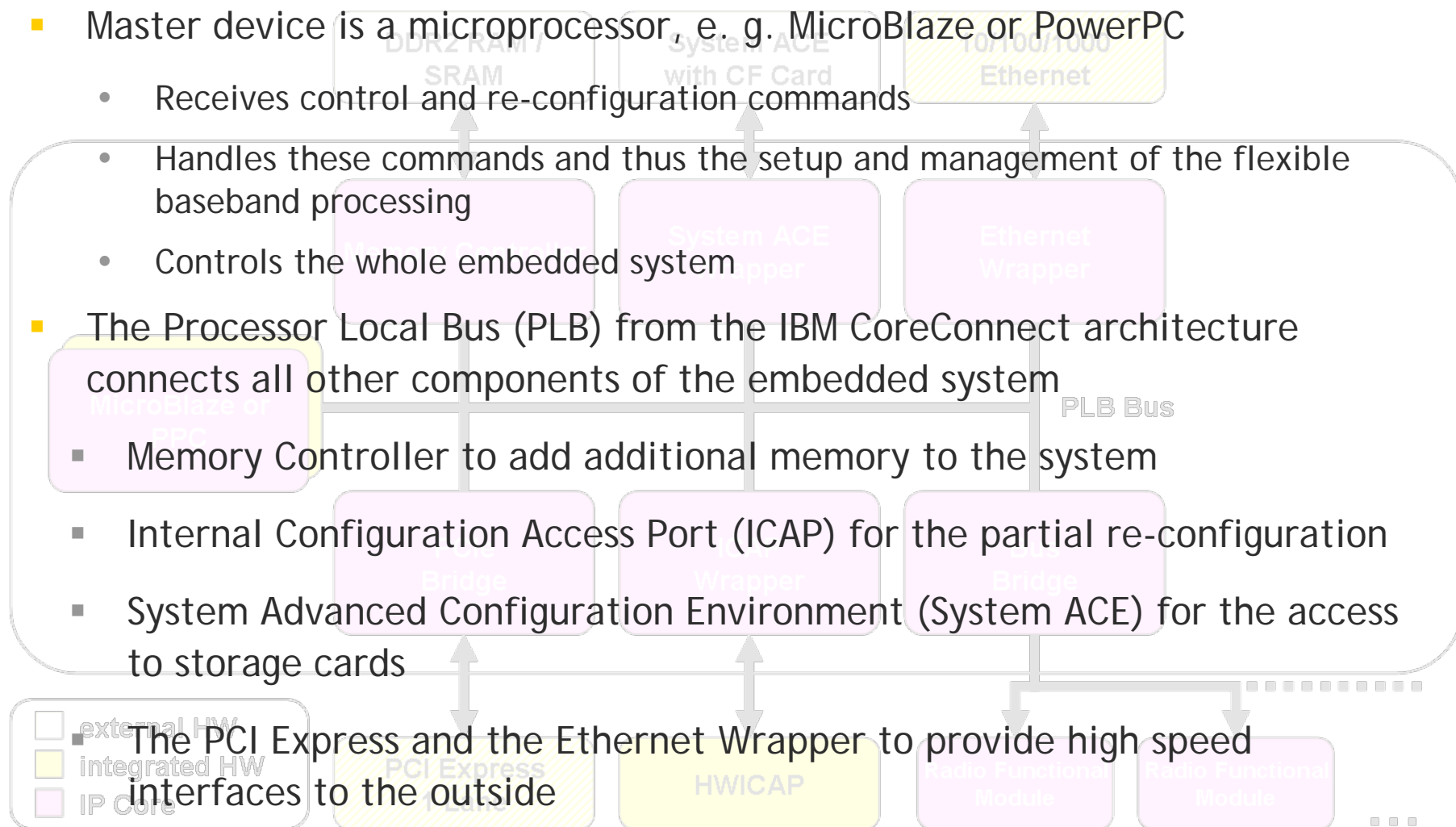
- Master device is a microprocessor, e. g. MicroBlaze or PowerPC

- Receives control and re-configuration commands
- Handles these commands and thus the setup and management of the flexible baseband processing
- Controls the whole embedded system

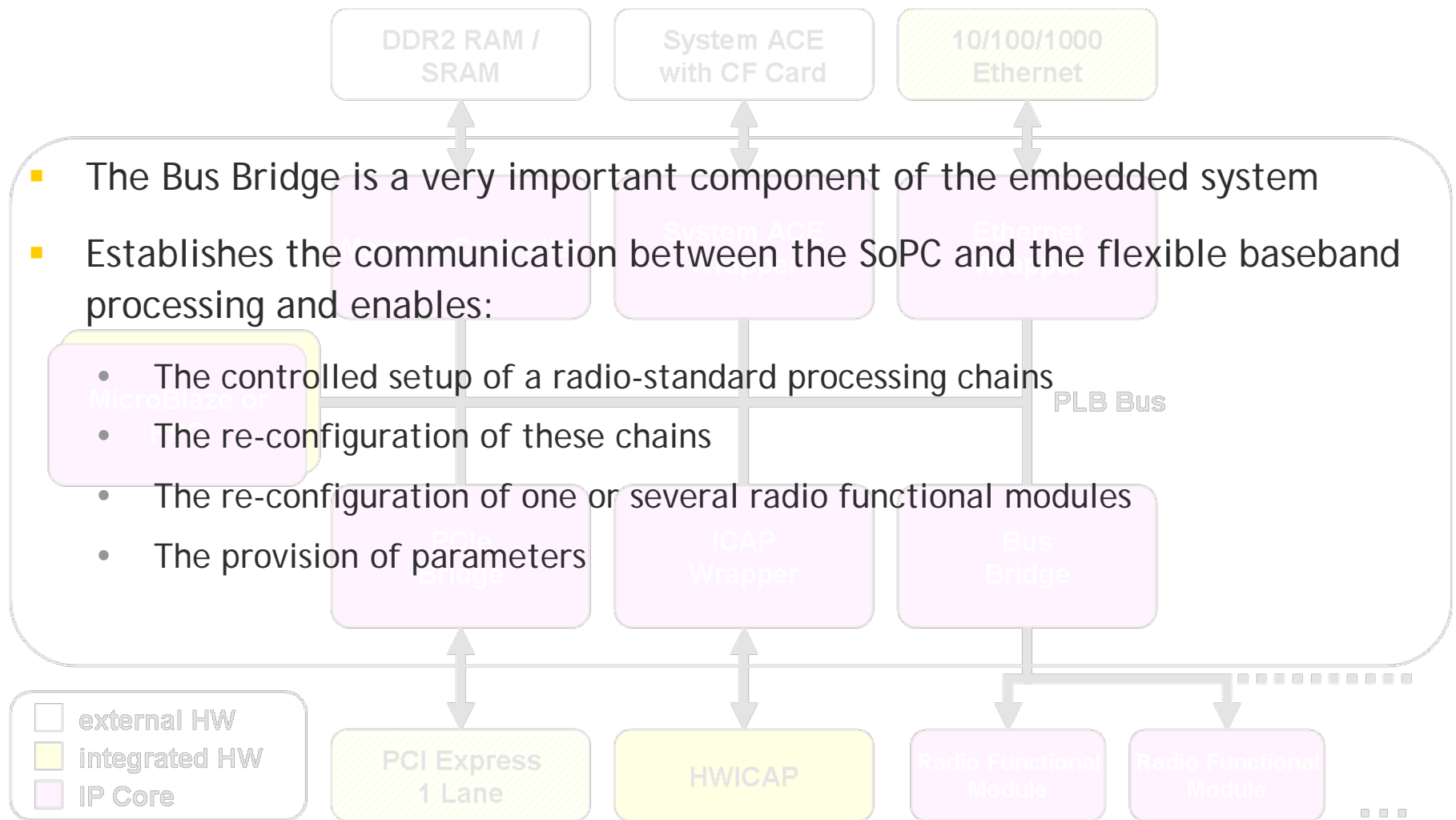
- The Processor Local Bus (PLB) from the IBM CoreConnect architecture connects all other components of the embedded system

- Memory Controller to add additional memory to the system
- Internal Configuration Access Port (ICAP) for the partial re-configuration
- System Advanced Configuration Environment (System ACE) for the access to storage cards

- The PCI Express and the Ethernet Wrapper to provide high speed interfaces to the outside



System on a Programmable Chip



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Flexible Baseband Processing

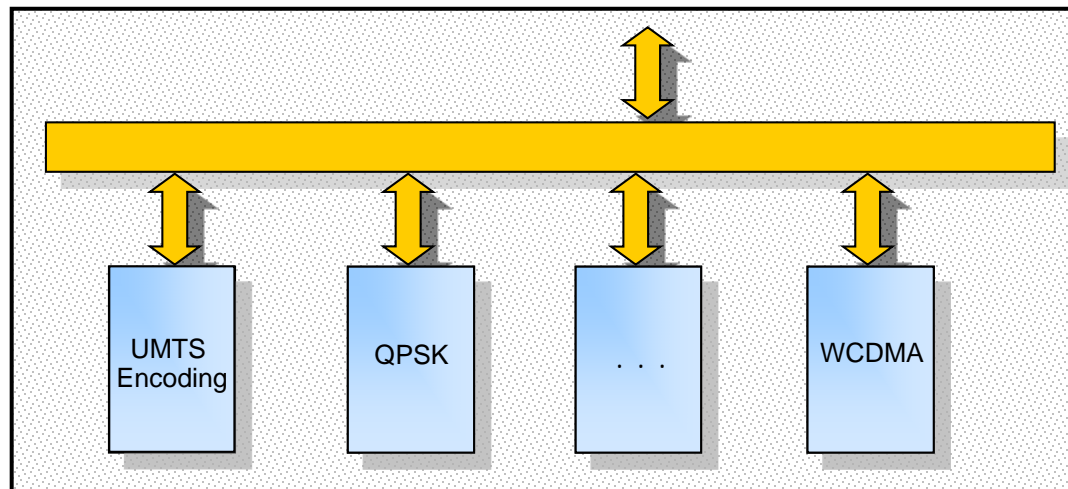


What are possible architectures?

How we can realize the flexible baseband processing?

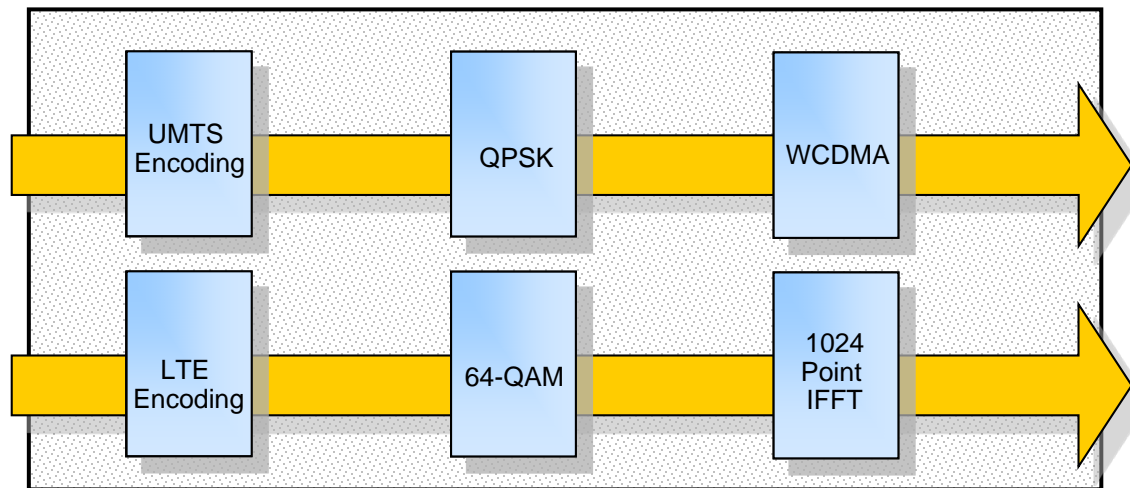
Flexible Baseband Processing

- Bus system
 - Good upgradeable and serviceable
 - Limited throughput



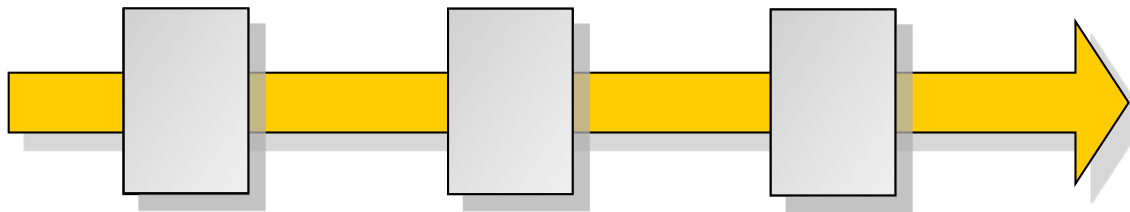
Flexible Baseband Processing

- Signal processing chain
 - Higher throughput compared to the bus system
 - Limited flexibility



Flexible Baseband Processing

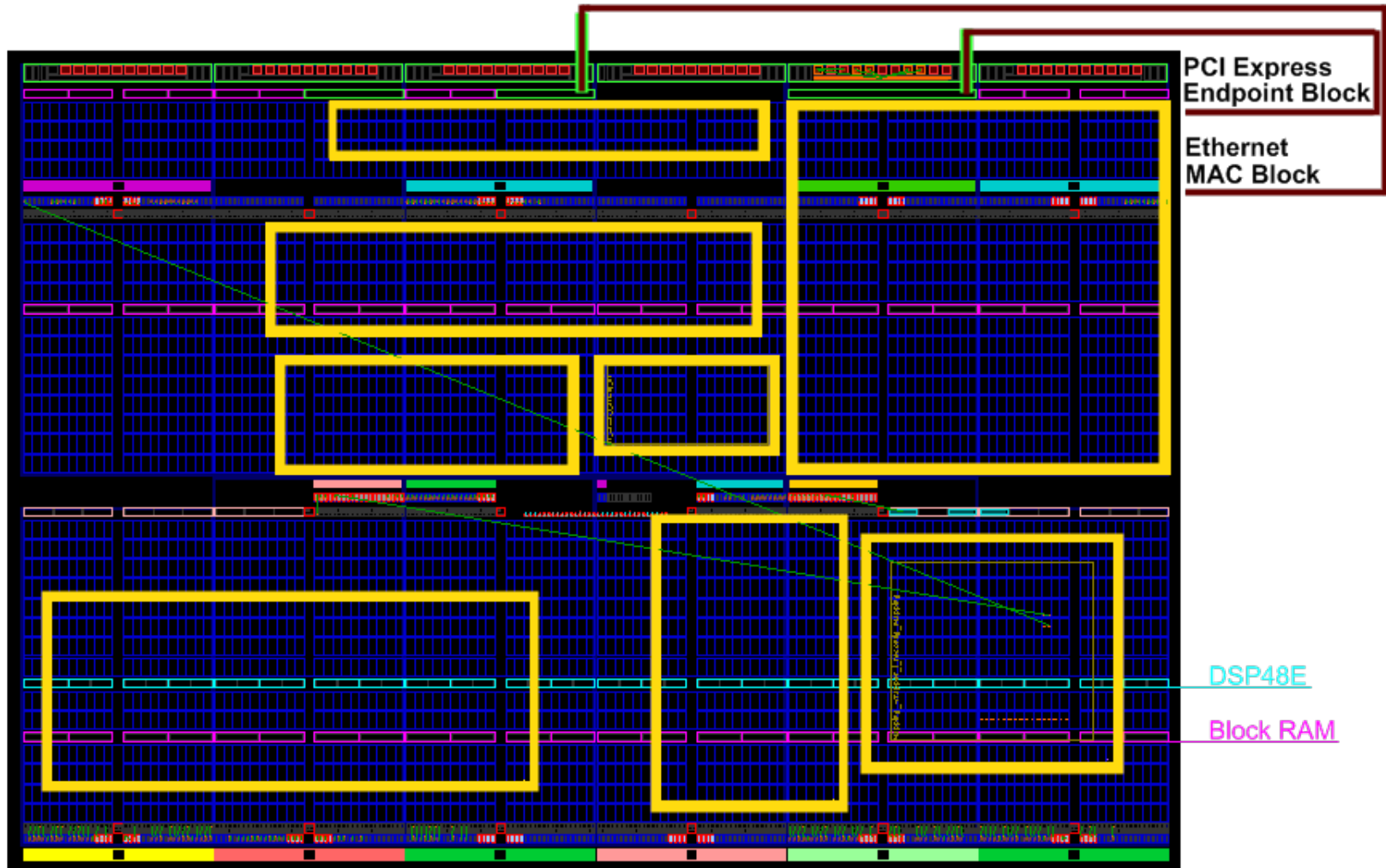
- Parametrizable radio functional modules
- Partial reconfiguration technology
 - Static baseband processing chain with placeholders (so-called partial reconfiguration regions (PRRs))



- Setup of the baseband processing via the ICAP
- Initialization via the Bus Bridge

Flexible Baseband Processing

- A good design of the static chain is necessary for a maximum of flexibility



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Performance Analysis



What is the expected (re-configuration) performance?

Performance Analysis

- Theoretical parameters

- Partial re-configuration bus is 32 bit wide
- Partial re-configuration bus runs at 100 MHz
- Gives a theoretical re-configuration rate of 3.2 Gbps

- Partial bit stream size

- Depends on the number of needed look-up tables, flip-flops, DSP48E elements and BRAMs

- The FBP design

- 8 bit wide re-configuration bus (minimum resource usage) running at 100 MHz
- Data rate of 800 Mbps
- Additional overhead to address the correct PRR

- A performance analysis can be done with the FBP design parameters and the partial bit stream size

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Thank you!

Any questions?

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