An Embedded Controlled Flexible Baseband Processing Approach

Dr. Thomas Loewel
Christian Lange
Andreas Wich
Wolfgang Koenig
Ferenc Noack

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Agenda

1. General Flexible Base Station Architecture
2. Flexible Baseband Architecture
3. Control Application
4. System on a Programmable Chip
5. Flexible Baseband Processing
6. Performance Analysis

1 General Flexible Base Station Architecture

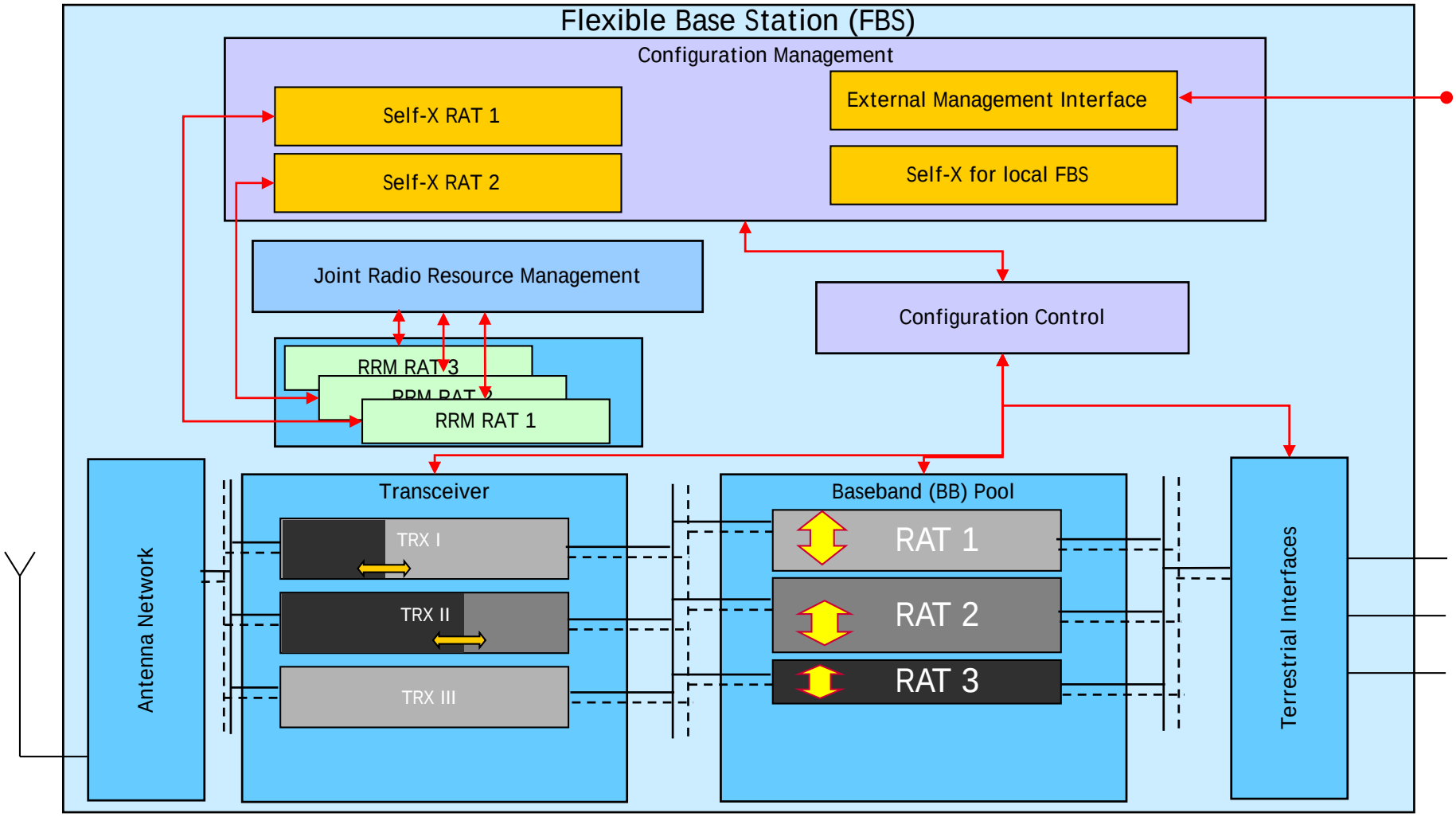
What is a Flexible Base Station (FBS)?

What are the key elements of such FBS?

Flexible Base Station Architecture

- Multi-standard Transceiver
- Flexible baseband processing
- Multiple radio-standard processing chains
  - Universal Mobile Telecommunication System (UMTS)
  - Long Term Evolution (LTE)
- Dynamic load balancing between these standards
- Simple extension of the Radio Access Technology (RAT)
- Flexible assembly of radio functional modules

Flexible Base Station Architecture

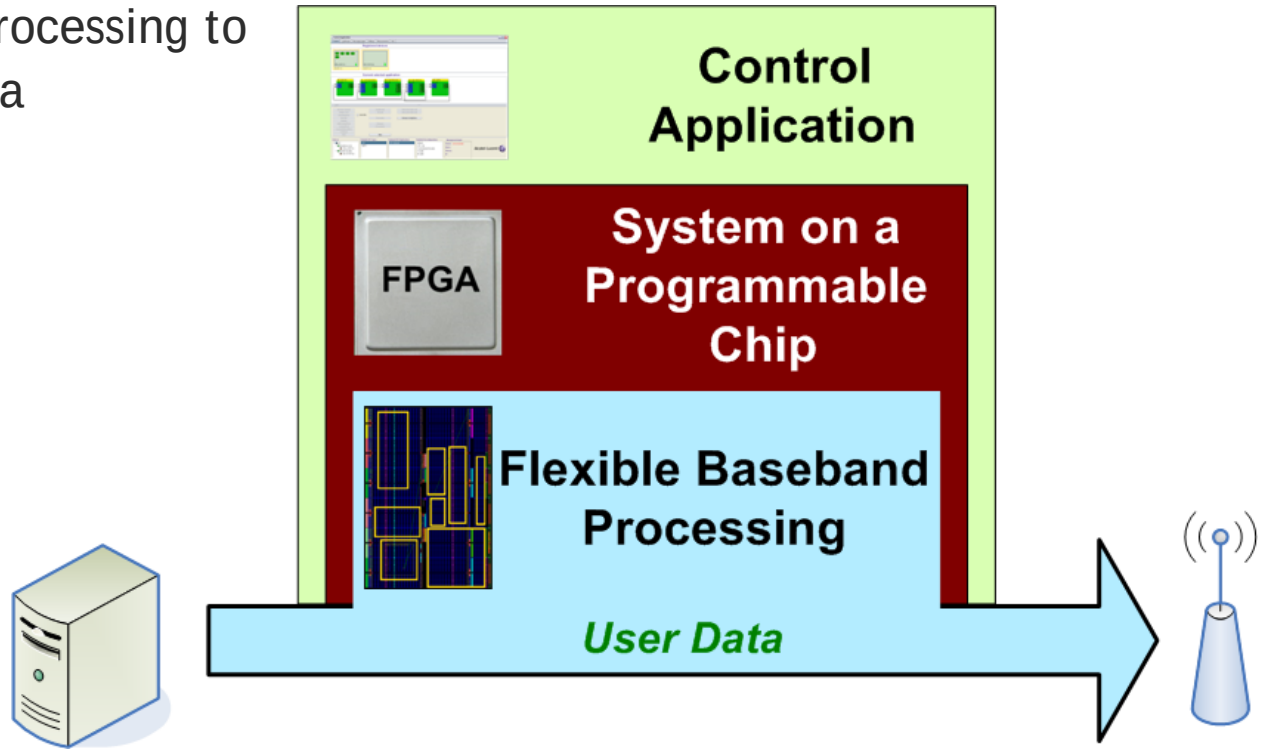


2 Flexible Baseband Architecture

What are the key elements of the flexible baseband?

Flexible Baseband

- Control Application to establish the communication with management modules
- Embedded system on a Field Programmable Gate Array (FPGA), so called System on a Programmable Chip (SoPC), to control the re-configuration
- Flexible baseband processing to process the user data



3 Control Application

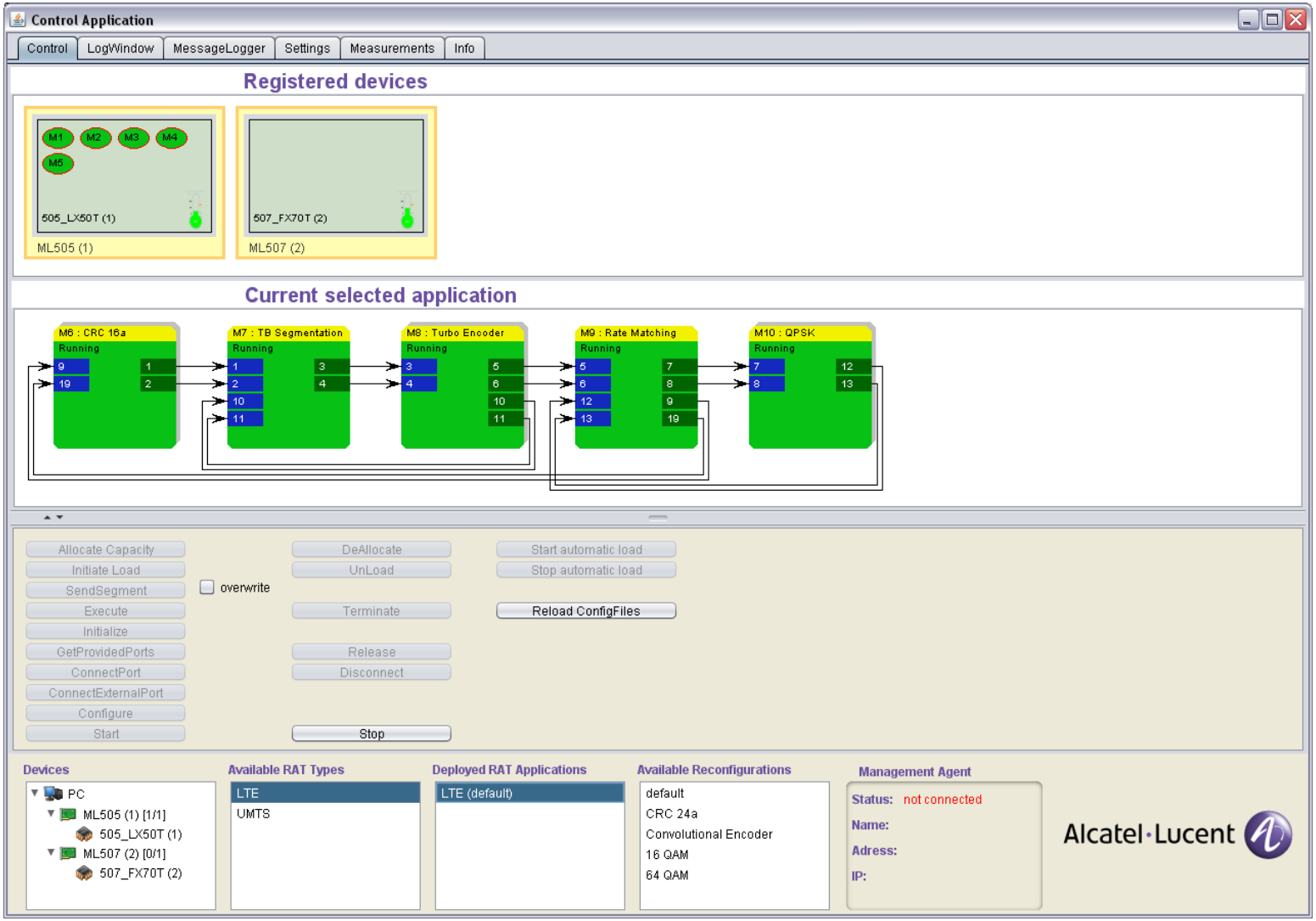
What is the Control Application?

What are the tasks of the Control Application?

Control Application

- Interface between different management modules and different flexible baseband boards
- Supports Object Management Group (OMG) commands
- Direct control and monitoring of the flexible baseband boards
- Easy and detailed setup of the baseband processing chain
  - Allocate Capacity, SendSegment, Execute, Start, Stop, Release etc.
- Gives an overview about all running RATs and all possible RATs

Control Application



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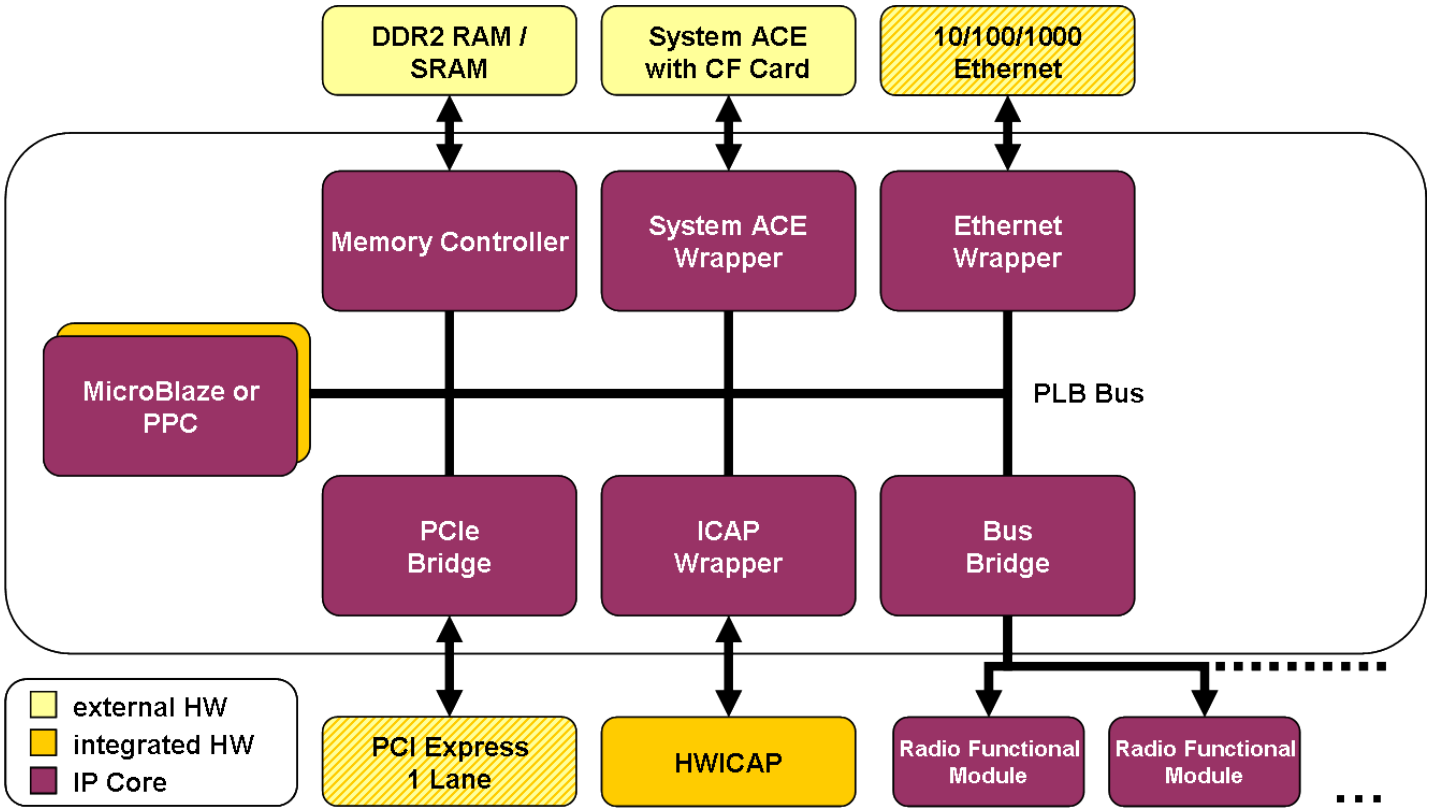
4 System on a Programmable Chip

Why we need such a system?

What is the architecture of this system?

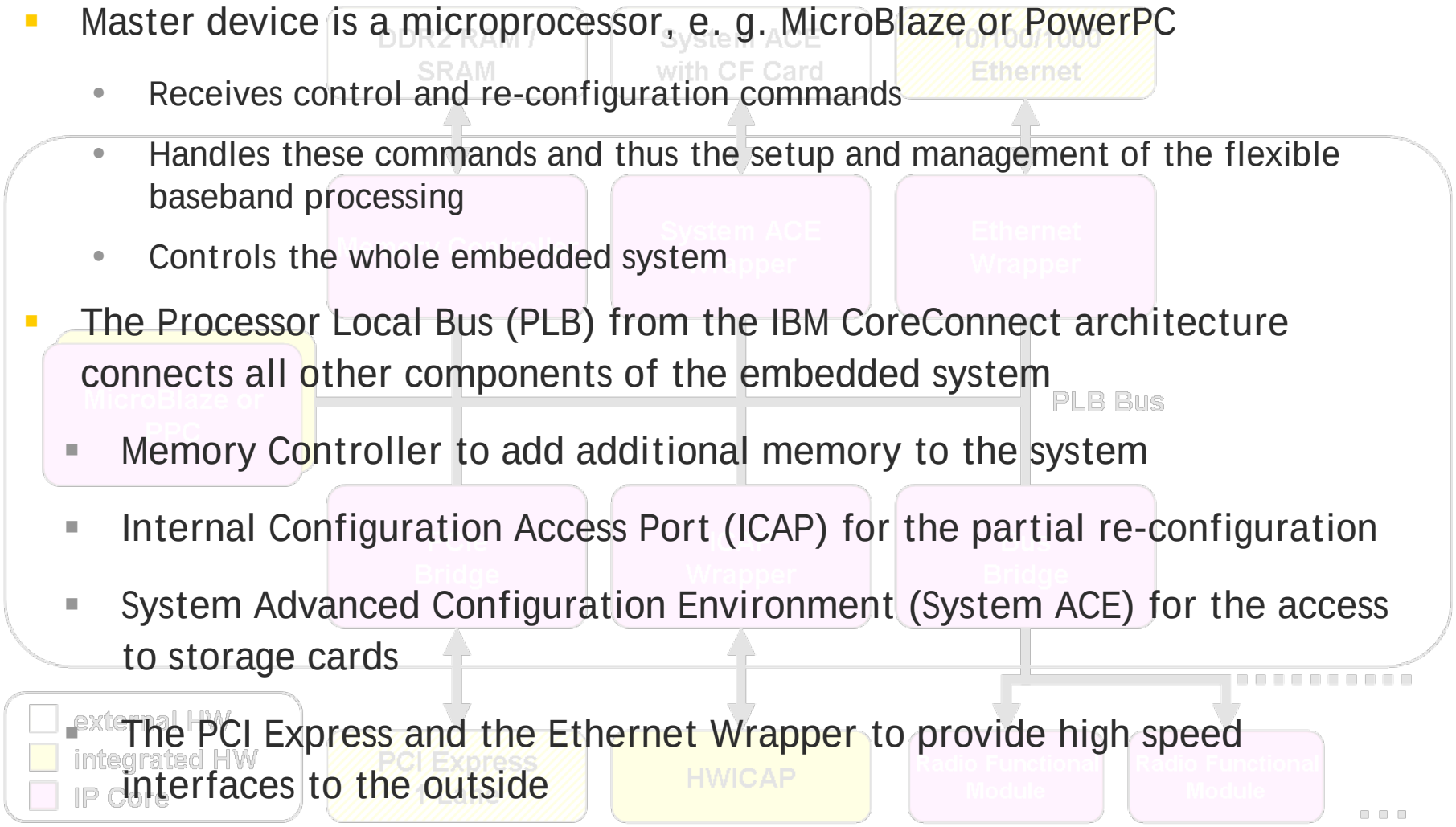
System on a Programmable Chip

- Major element for the flexibility and serviceability of the flexible baseband processing (FBP)
- Interface to the outside, e. g. to the Control Application

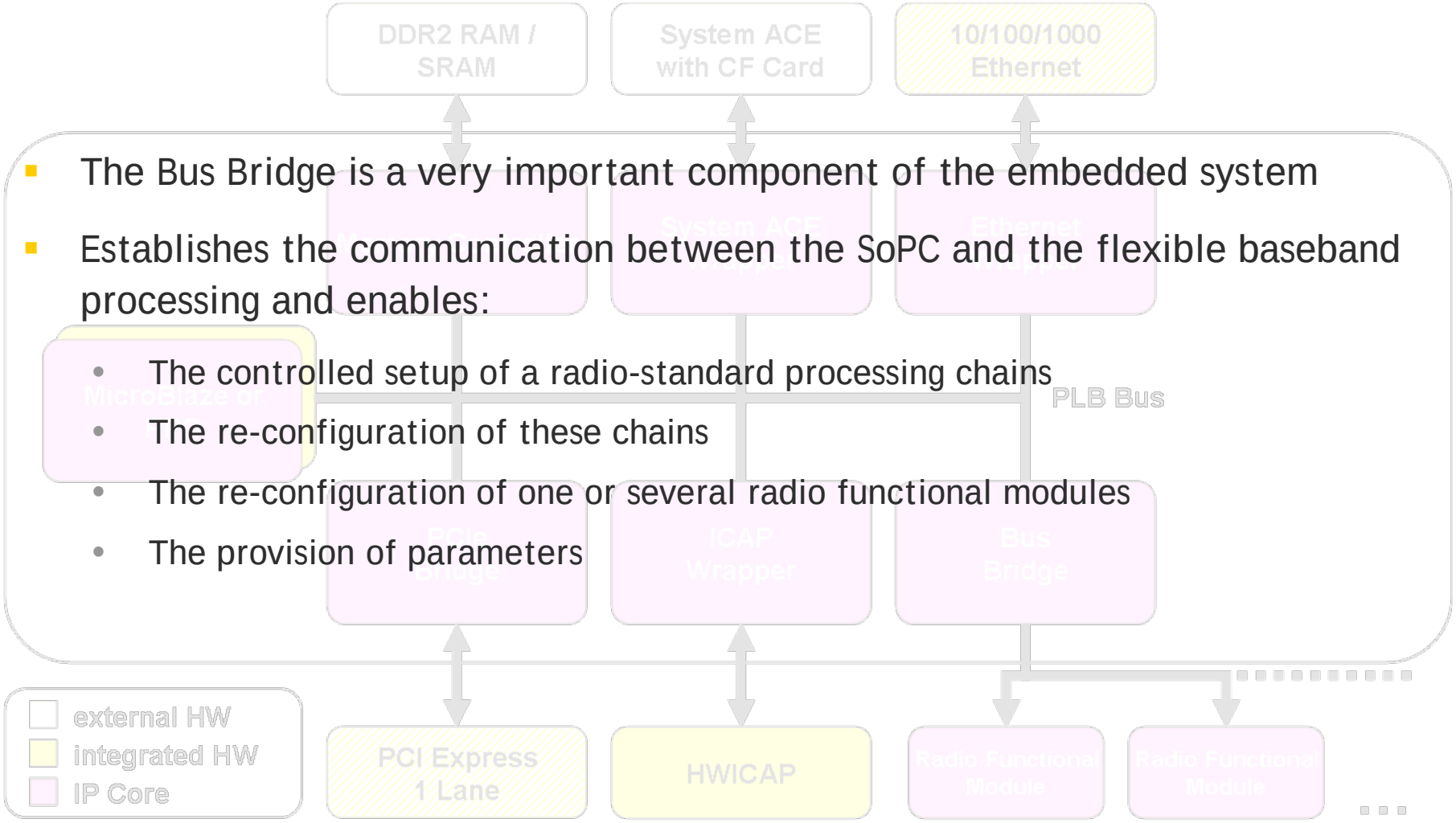


System on a Programmable Chip

- Master device is a microprocessor, e. g. MicroBlaze or PowerPC
  - Receives control and re-configuration commands
  - Handles these commands and thus the setup and management of the flexible baseband processing
  - Controls the whole embedded system
- The Processor Local Bus (PLB) from the IBM CoreConnect architecture connects all other components of the embedded system
  - Memory Controller to add additional memory to the system
  - Internal Configuration Access Port (ICAP) for the partial re-configuration
  - System Advanced Configuration Environment (System ACE) for the access to storage cards
  - The PCI Express and the Ethernet Wrapper to provide high speed interfaces to the outside



System on a Programmable Chip



- The Bus Bridge is a very important component of the embedded system
- Establishes the communication between the SoPC and the flexible baseband processing and enables:
  - The controlled setup of a radio-standard processing chains
  - The re-configuration of these chains
  - The re-configuration of one or several radio functional modules
  - The provision of parameters

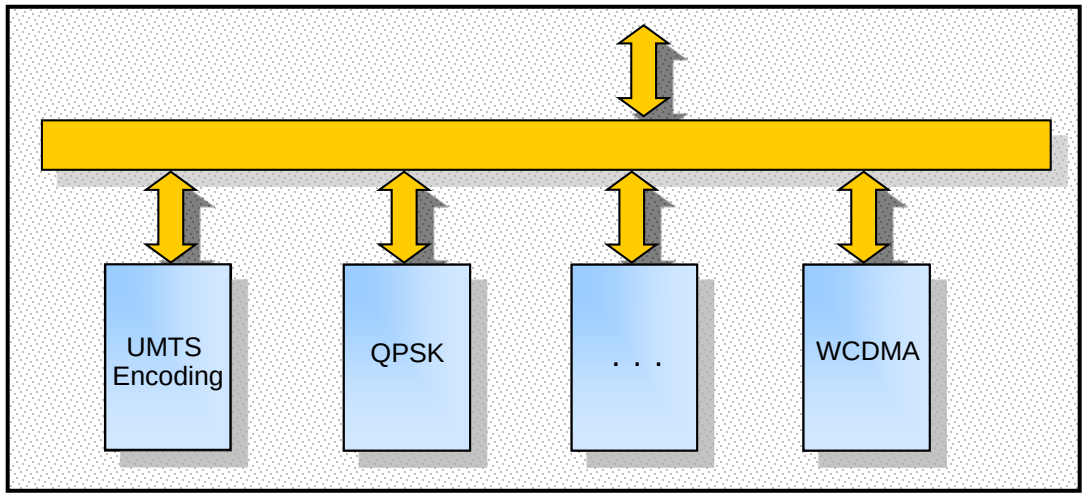
5 Flexible Baseband Processing

What are possible architectures?

How we can realize the flexible baseband processing?

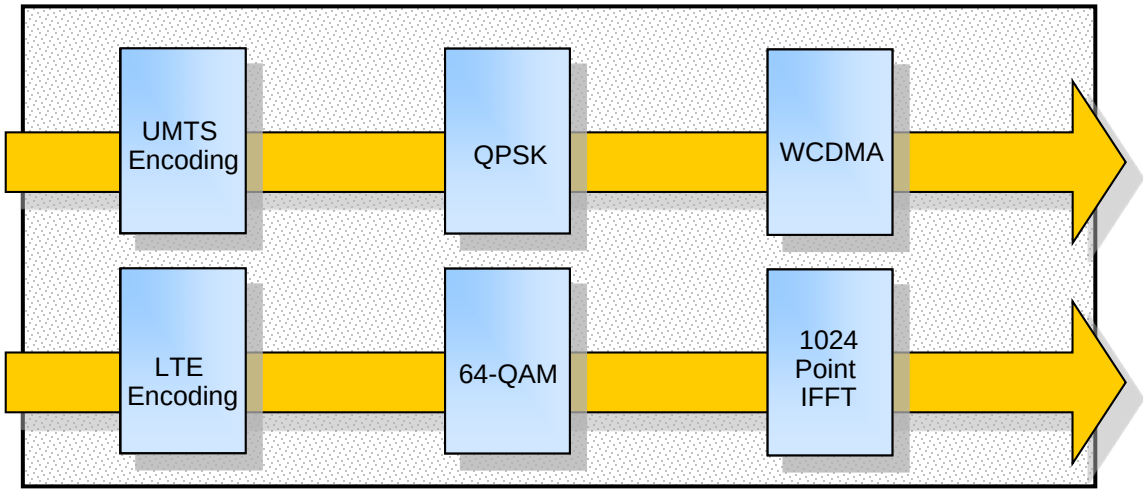
Flexible Baseband Processing

- Bus system
  - Good upgradeable and serviceable
  - Limited throughput



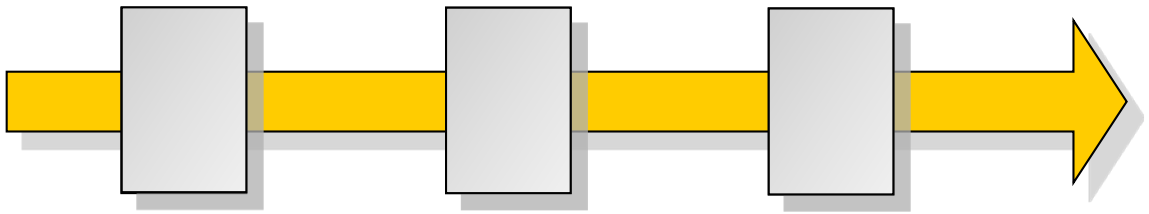
Flexible Baseband Processing

- Signal processing chain
  - Higher throughput compared to the bus system
  - Limited flexibility



Flexible Baseband Processing

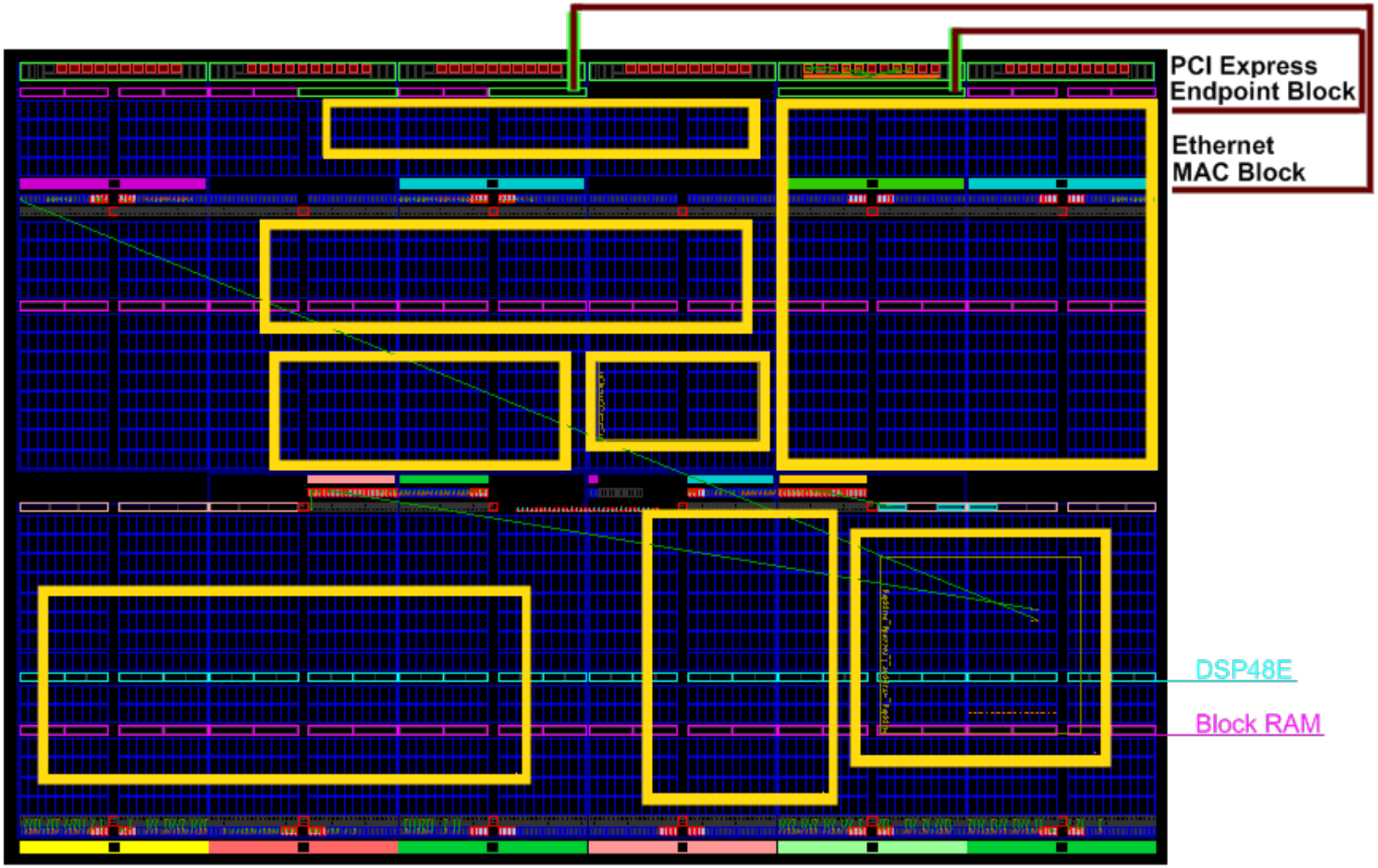
- Parametrizable radio functional modules
- Partial reconfiguration technology
  - Static baseband processing chain with placeholders (so-called partial reconfiguration regions (PRRs))



  - Setup of the baseband processing via the ICAP
  - Initialization via the Bus Bridge

Flexible Baseband Processing

- A good design of the static chain is necessary for a maximum of flexibility



6 Performance Analysis

What is the expected (re-configuration) performance?

Performance Analysis

- Theoretical parameters
  - Partial re-configuration bus is 32 bit wide
  - Partial re-configuration bus runs at 100 MHz
  - Gives a theoretical re-configuration rate of 3.2 Gbps
- Partial bit stream size
  - Depends on the number of needed look-up tables, flip-flops, DSP48E elements and BRAMs
- The FBP design
  - 8 bit wide re-configuration bus (minimum resource usage) running at 100 MHz
  - Data rate of 800 Mbps
  - Additional overhead to address the correct PRR
- A performance analysis can be done with the FBP design parameters and the partial bit stream size

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Thank you!

Any questions?

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