Implementation of a 350 Mbps FPGA-Based Modem

Michael Rupar

John Glancy

Benjamin Egg

SDR '09
Paper #1569210259
2 December 2009

Extended Reachback Communications

This effort is to develop an affordable, small, low power modem/data link for communications from a UAV to a stationary receiver capable of moving up 350 Mbps off the platform over a distance no less than 70 nautical miles.

350 Mbps

High Data Rate Requirements for Detection & Identification

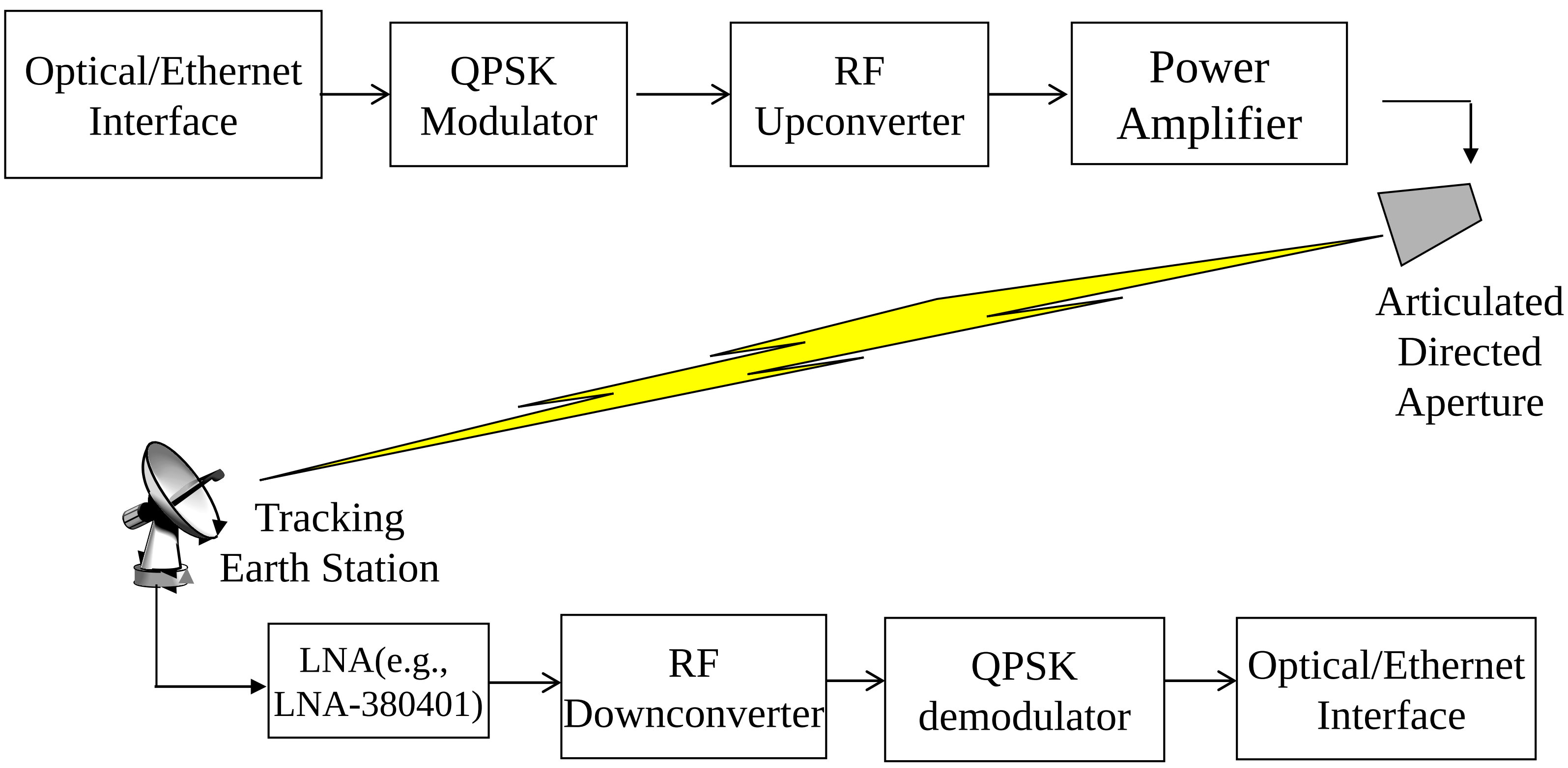
- Search Radars
- Mid-wave IR Sensors
- Electro Optic cameras

- Devices exist for installation on UAVs and manned aircraft
  - Real-time lossless compression algorithms to significantly reduce/compress the required data transfer rate back to the “exploitation site” are a serious challenge on UAVs
  - ATR (automatic target recognition) algorithms and real time code aren't mature for returning only detection reports. This dictates that raw sensor data must be returned to the intelligence analyst.

- Therefore, it is necessary to provide high data rate links off the UAV platform to effectively convey surveillance information!

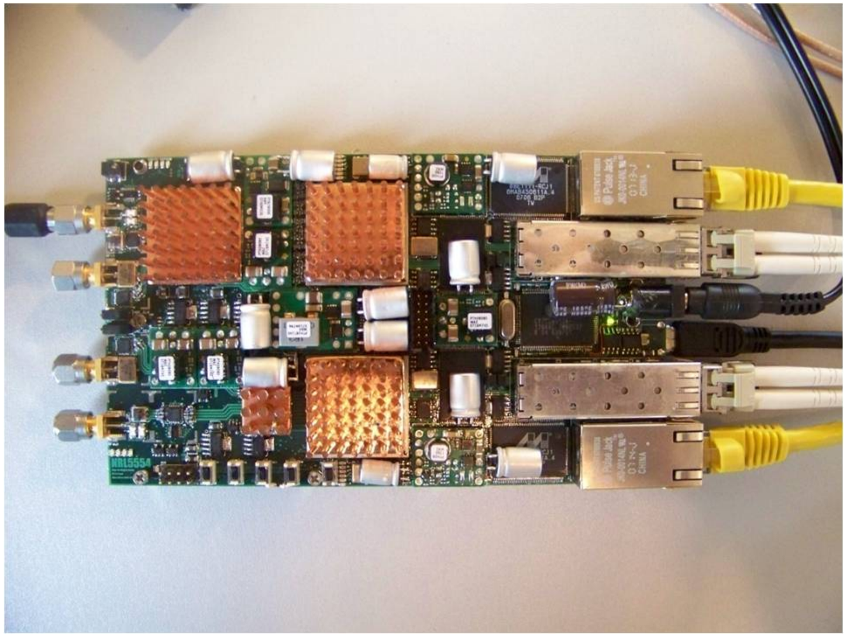
System Diagram

- Return link at lower frequencies, utilizing UHF and Omnidirectional antennas
- Modem developed for simplex operation – no closed loop



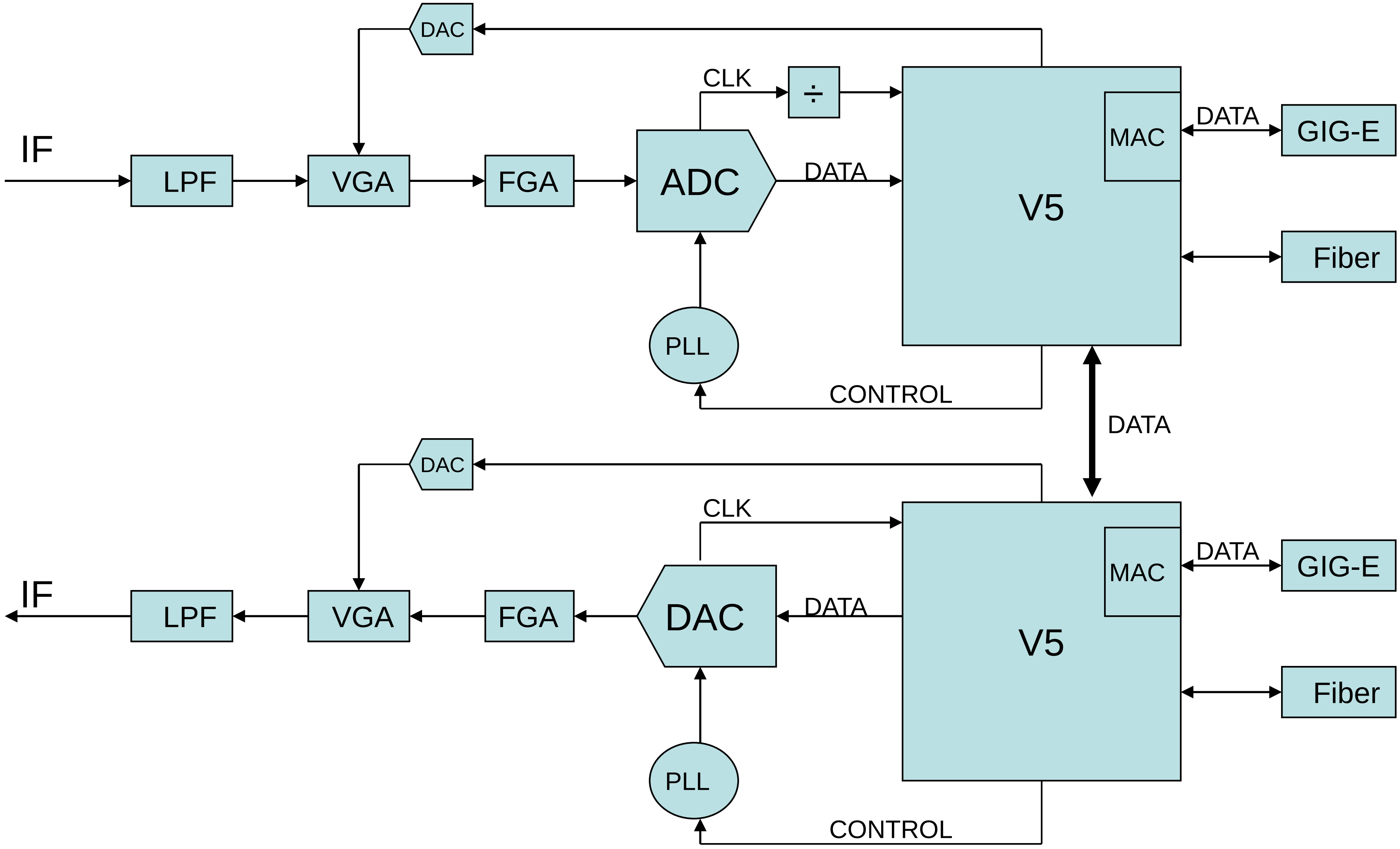
Target Development Board

- BDR-1, Basic Digital Radio Platform
  - 2 Xilinx Virtex-5 FPGAs (SX50T)
    - 550 MHz Max Speed
    - 288 DSP48E Blocks
    - 132 BRAMS (4,752 Kbits)
  - 2.3 Gsps 12-bit DAC
  - 1.5 Gsps 8-bit ADC
  - Low jitter reference clocks

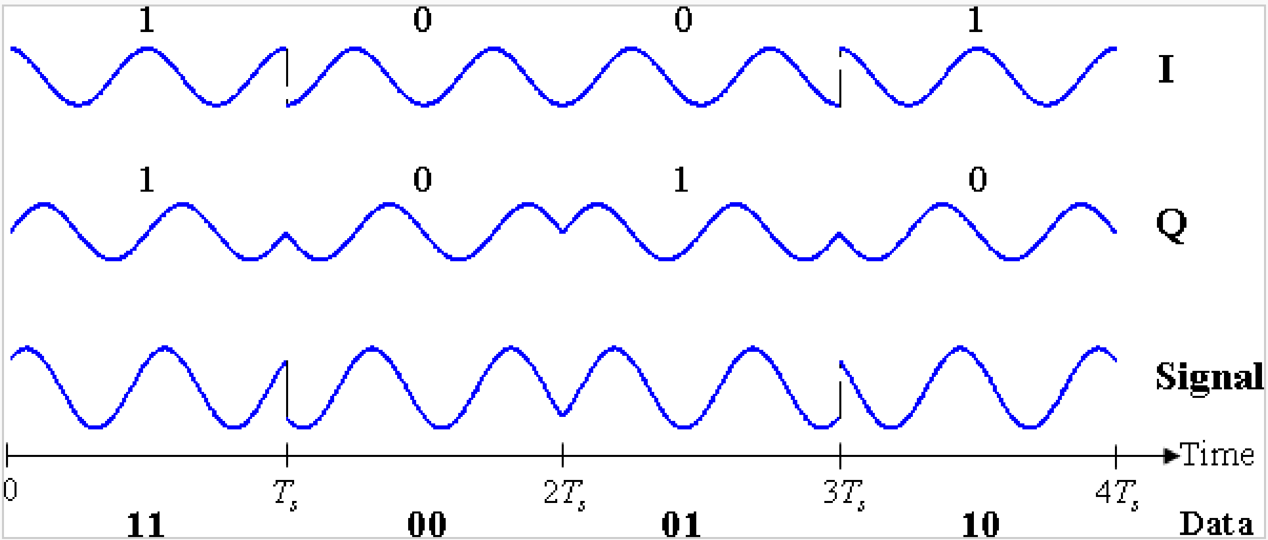


- 18W power draw
- Simplex or full-duplex
- Technical consultants
  - Dr. Fred Harris and Associates, San Diego State University

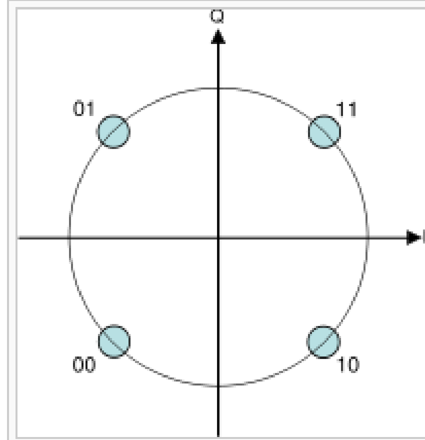
Block Diagram
BDR-1 Platform



Quadrature Phase-Shift Keying (QPSK) Modulation



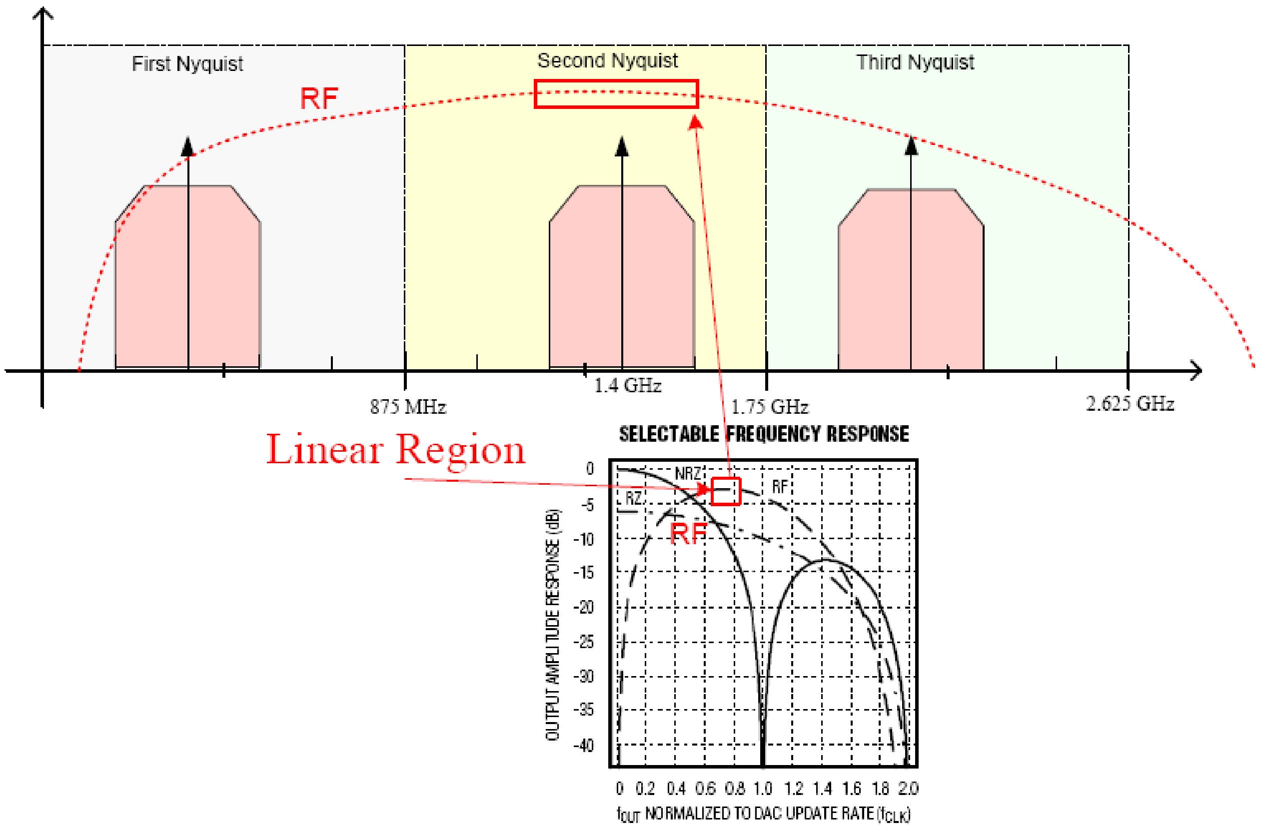
Timing diagram for QPSK. The binary data stream is shown beneath the time axis. The two signal components with their bit assignments are shown the top and the total, combined signal at the bottom. Note the abrupt changes in phase at some of the bit-period boundaries.



Constellation diagram for QPSK with Gray coding. Each adjacent symbol only differs by one bit.

* Diagrams taken from Wikipedia

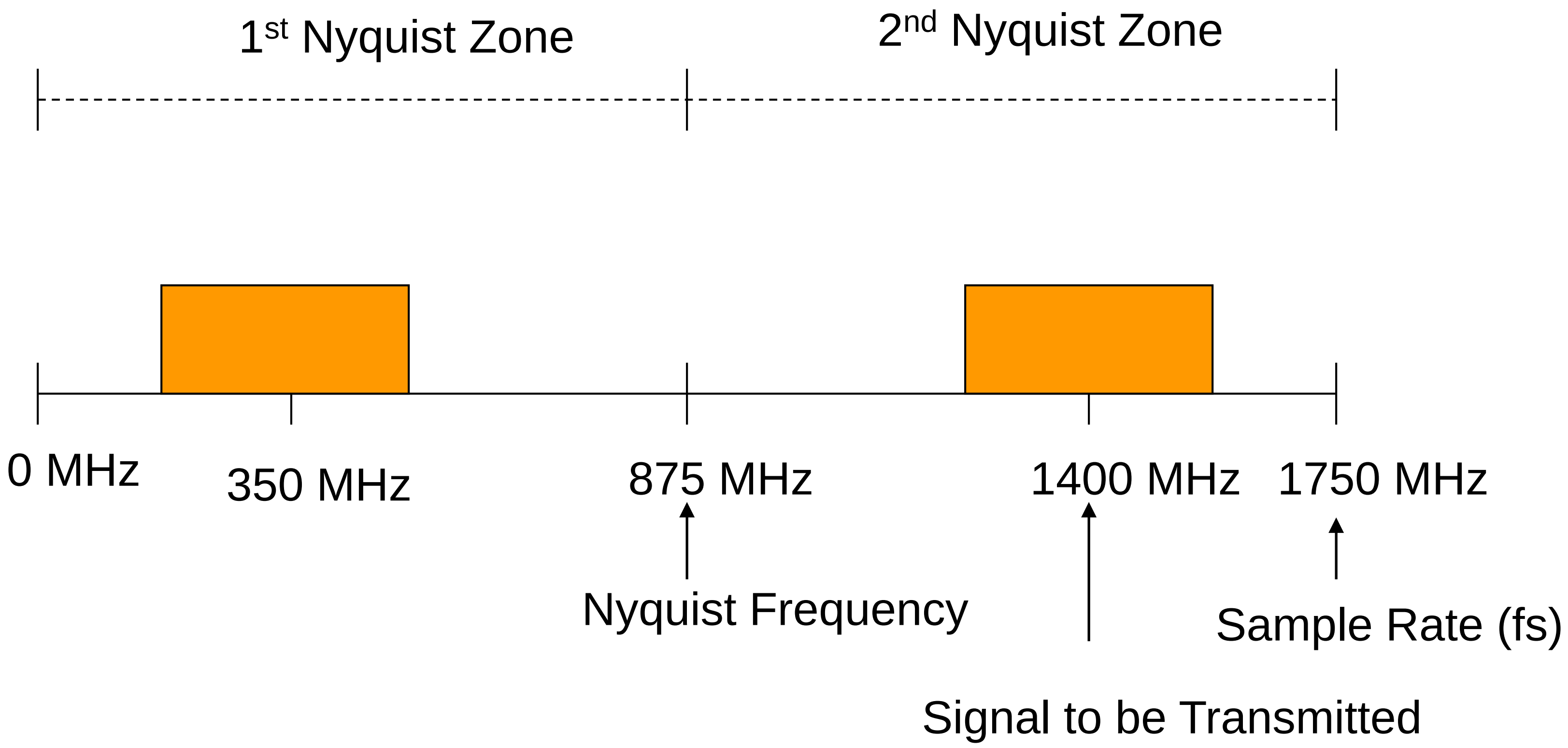
DAC Frequency Response



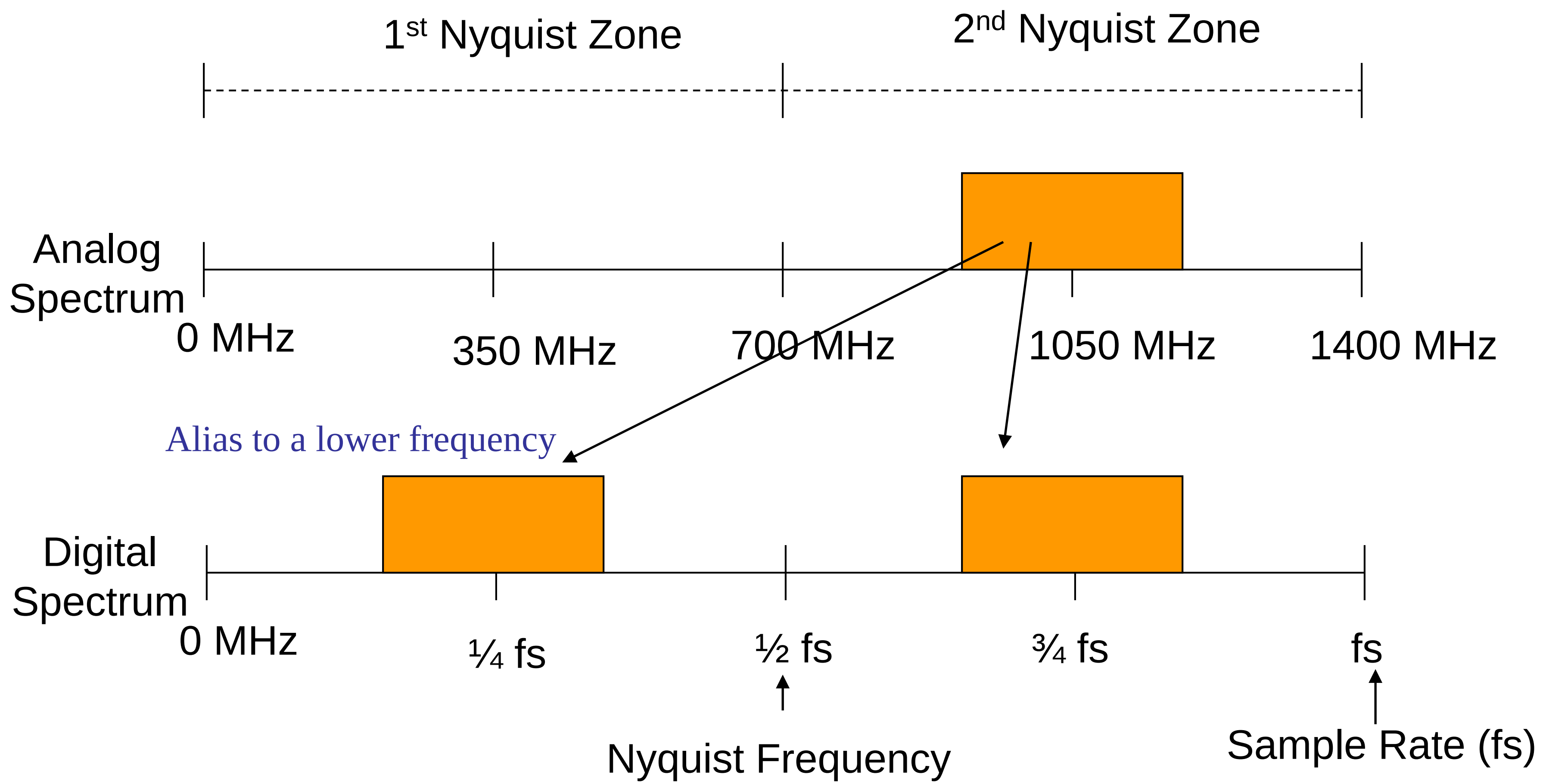
Maxim 2.3 GSPS DAC with RF output Mode: MAX19692

Tx signal centered at the most linear region of the DAC

Tx Frequency Plan



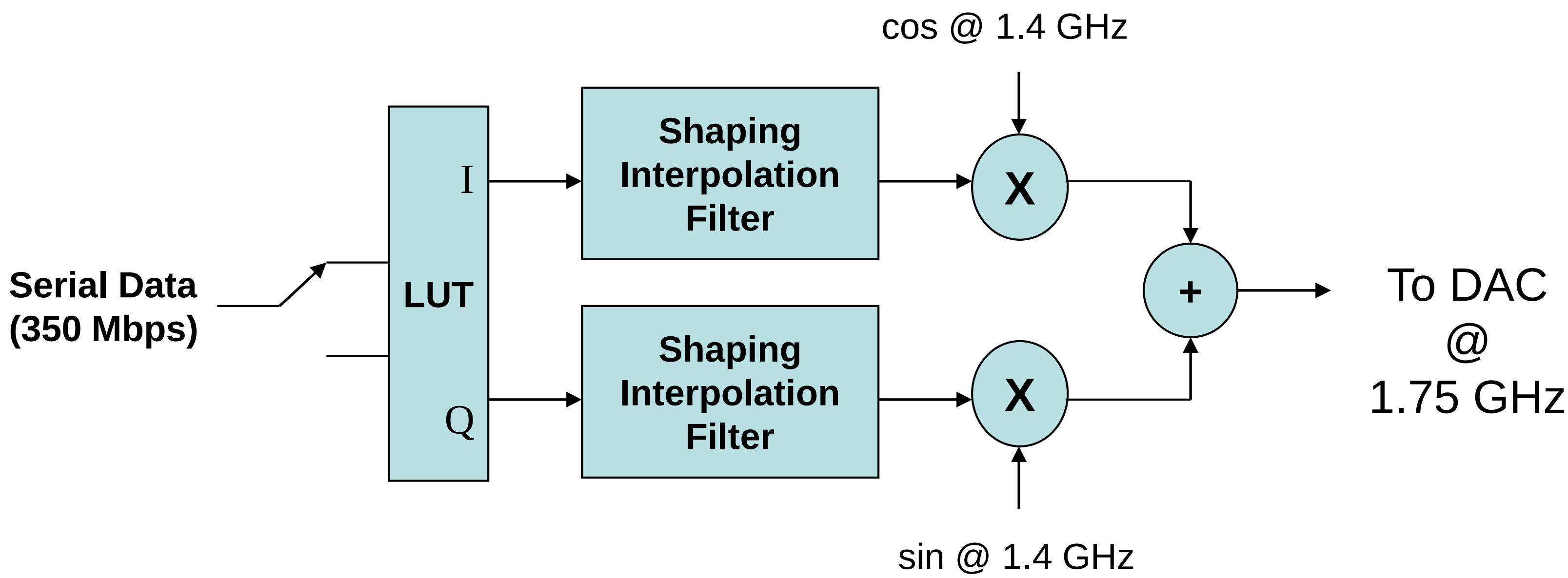
Rx Frequency Plan



On receive, the signal is at 1.05 GHz and is undersampled at 1.4 GHz

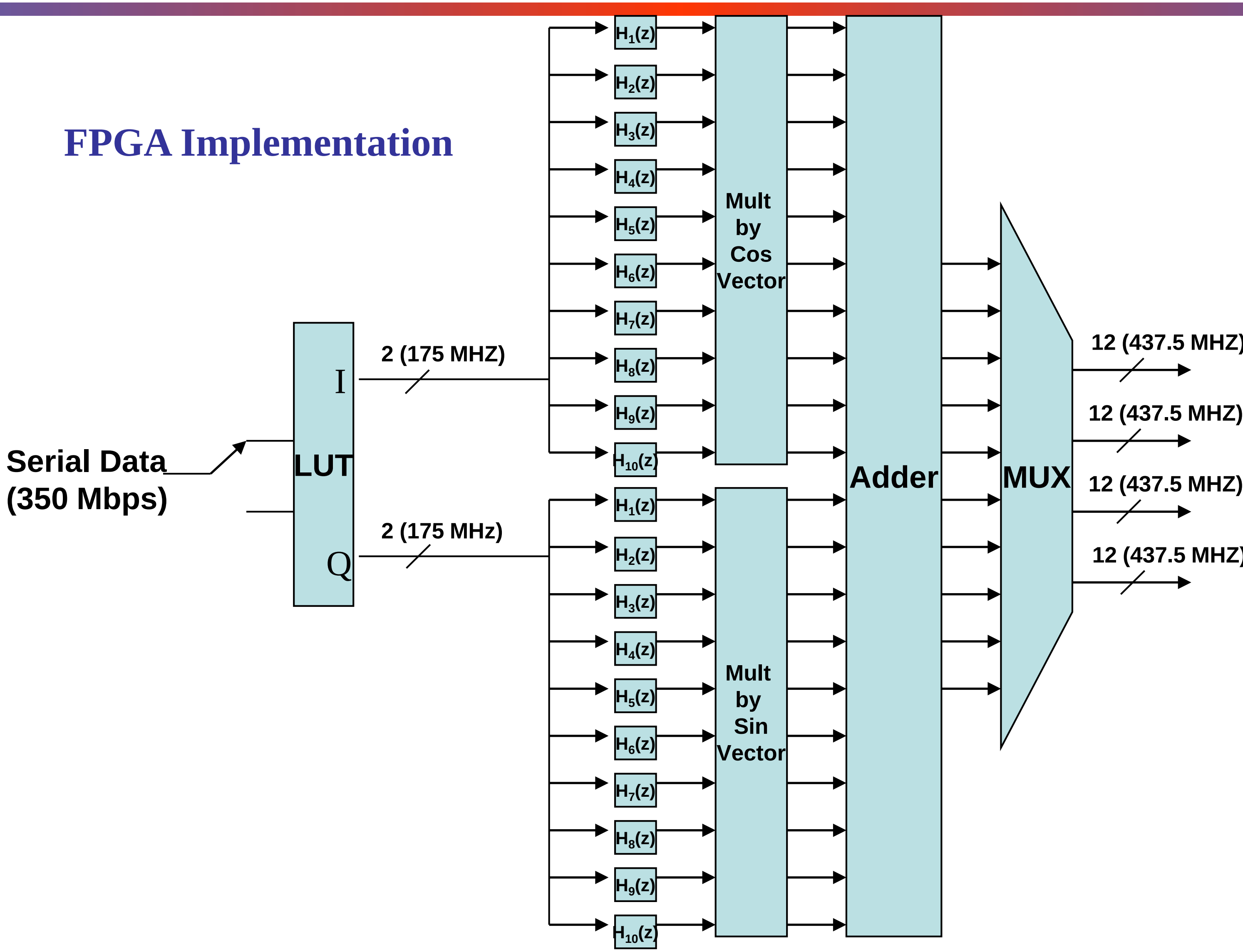
➢ ***downconversion without the IF analog chain***

QPSK Modulator

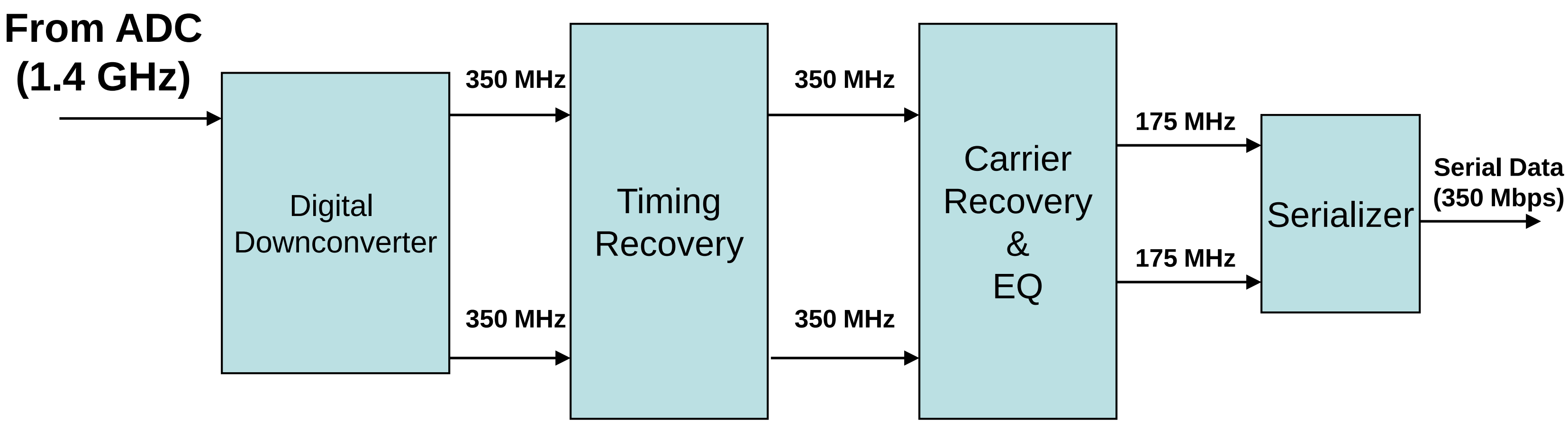


Detail on QPSK Modulator

FPGA Implementation

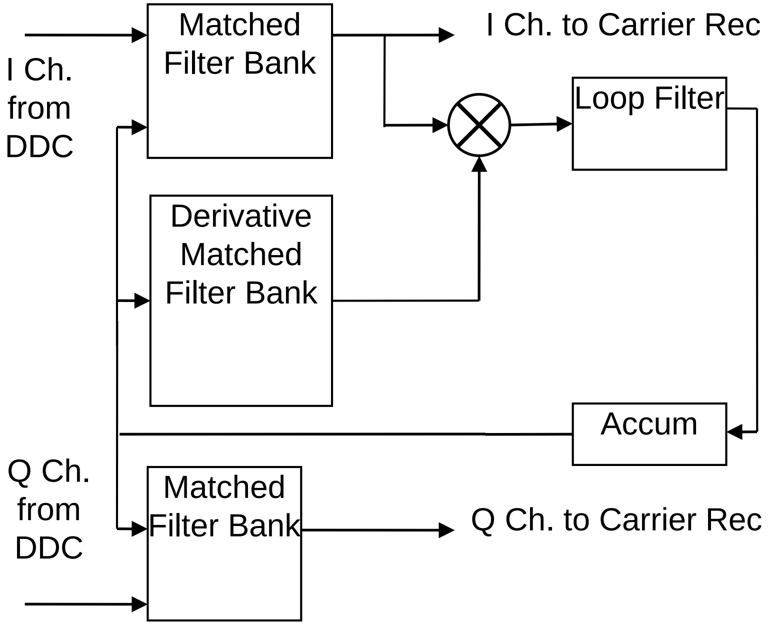


QPSK Demodulator



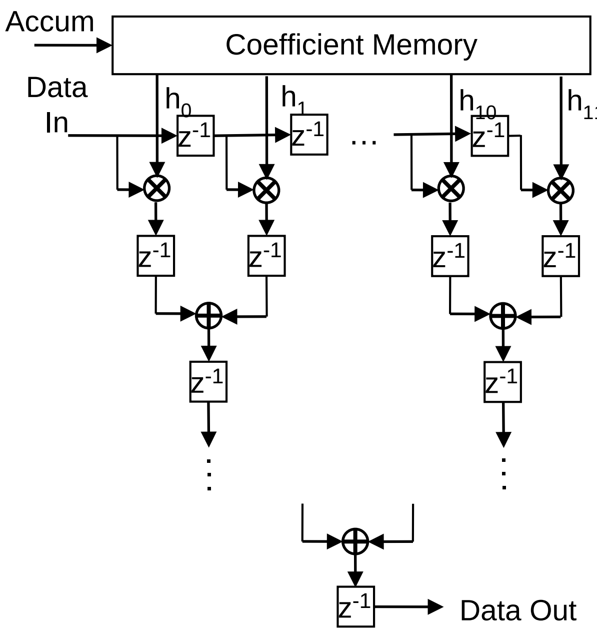
Timing Recovery

- Maximum Likelihood
  - Allows for faster locking than other algorithms.
- DDC Outputs are interpolated with polyphase matched filters. Only the correct leg is selected as an output.
- Timing error is the product of the Matched Filter output (amplitude) and the Derivative Matched Filter output
- Operates at 2 samples per symbol.
- "Valid" signal at output of timing recovery circuit indicates whether the 1st or 2nd sample is the valid data sample.



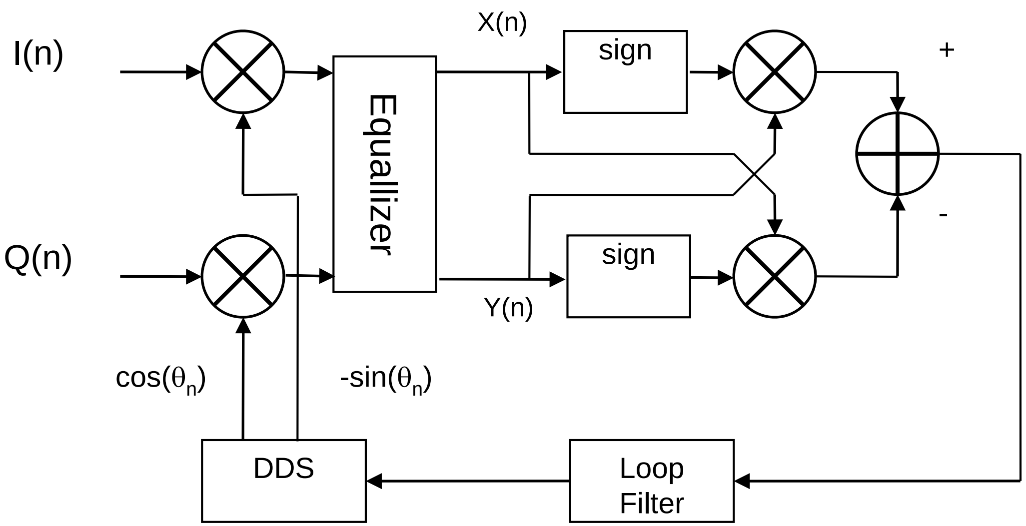
Matched Filter Bank FPGA Implementation

- Implemented as a reloadable coefficient filter with an adder tree.
- Using reloadable coefficients reduces the number of multipliers used.
- Using an adder tree allows for a shorter loop delay when new coefficients are loaded.



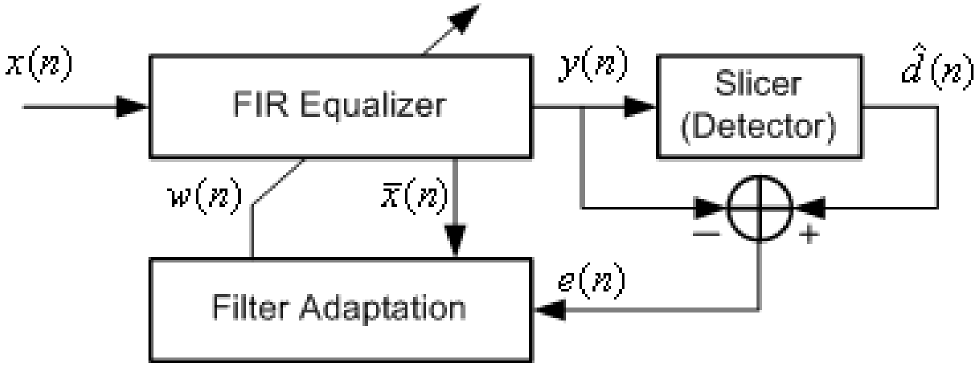
Carrier Recovery

- Angle between the received signal and the estimated signal is determined.
- The error is fed through a loop filter into a DDS which generates a complex sinusoid.
- The complex sinusoid is multiplied by the incoming signal to correct for any frequency rotation.



Linear Adaptive Equalizer

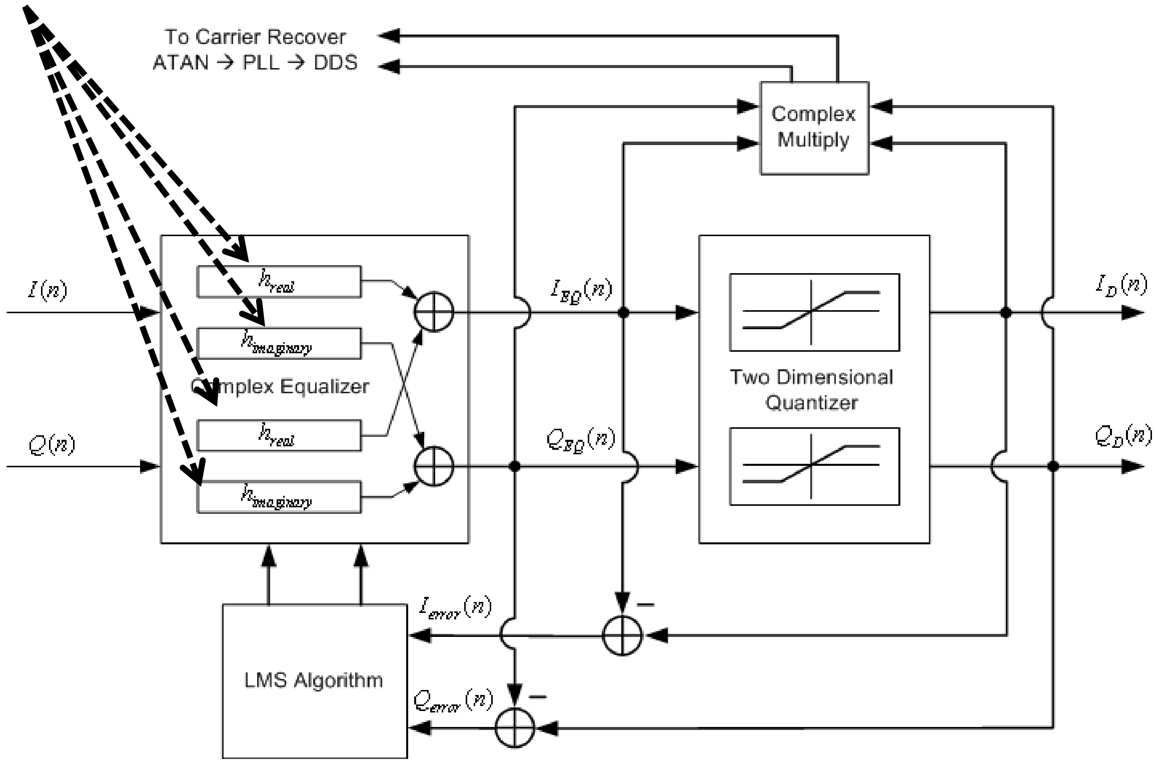
- The Equalizer is located directly after the polyphase match-filters and associated timing recovery loop. Acts as a fundamental component of the carrier recovery loop
- The equalizer attempts to correct channel distortions that it can "see" by adaptively modifying its complex filter coefficients *w(n)* until the error *e(n)* is minimized.



- The Error is calculated by subtracting the hard bit decision d(n) from the soft data value y(n) received into the "SLICER".

The Equalizer filter = 4 Filters

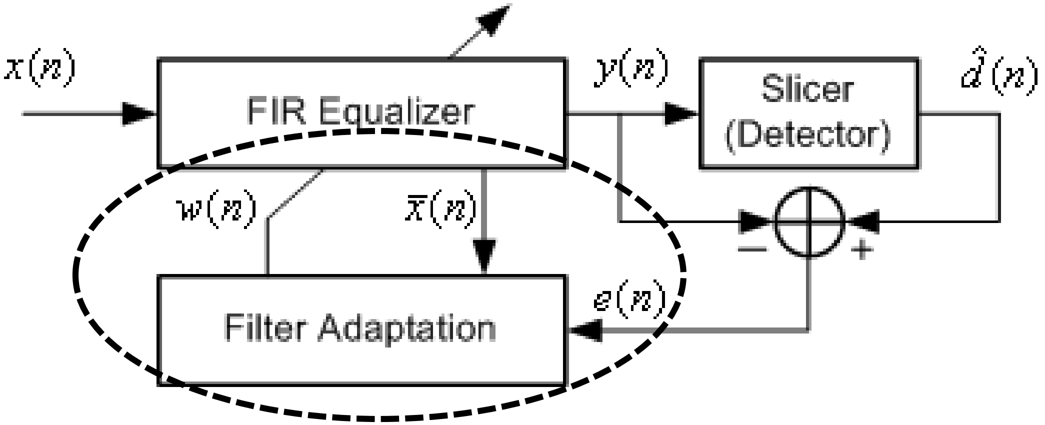
- The data into the equalizer is complex. Lets define the data as I(n)+j*Q(n).
- The equalizer filter is complex. Let's define the filter as: h_{real}+ j* h_{imag}(n).
- Thus we need **4 filters**:



Adapting to the channel

- The equalizer modifies it's complex filter coefficients using the LMS update algorithm:
  - The next set of filter coefficients w(n+1) is created by taking the previous coefficient set w(n) and adding a correction vector.
  - The correction vector is generated by multiplying the data vector X(n) with the complex conjugate of the error SCALAR e(n), and an additional damping factor μ.

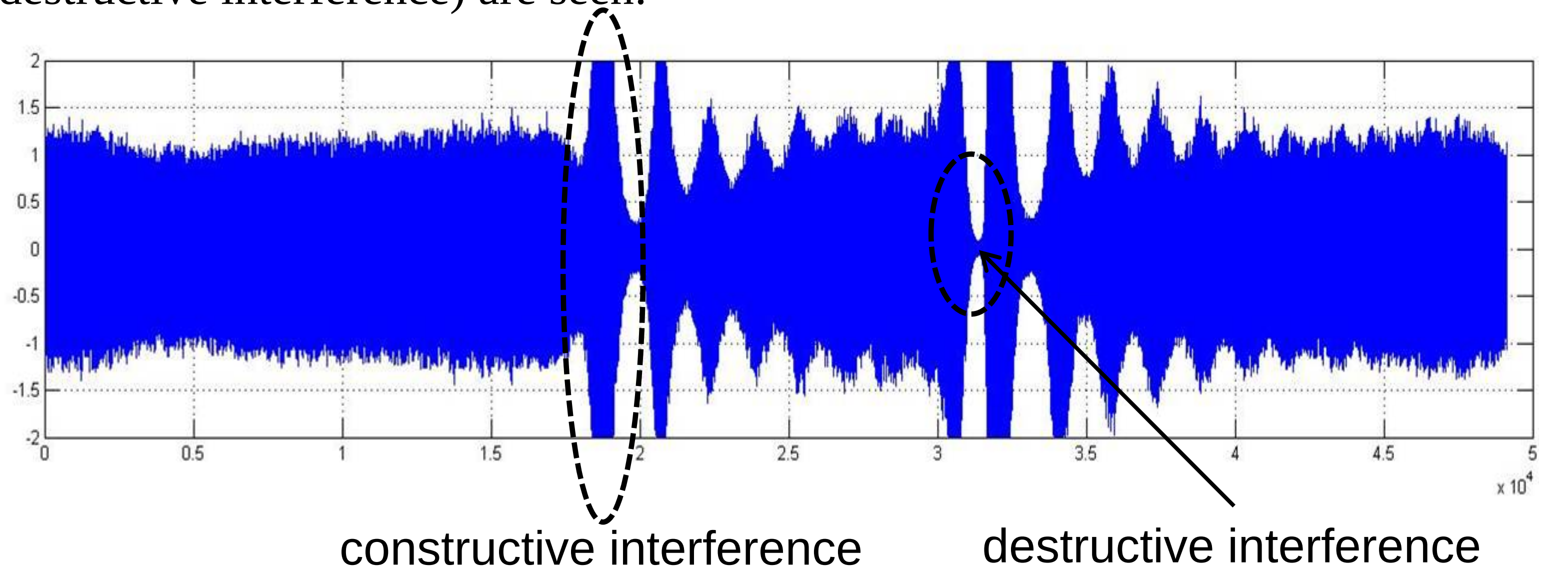
$$W(n+1) = W(n) + \mu \cdot e(n)^* \cdot X(n)$$



One Tough Channel: Test Data

Raw Output samples from ADC

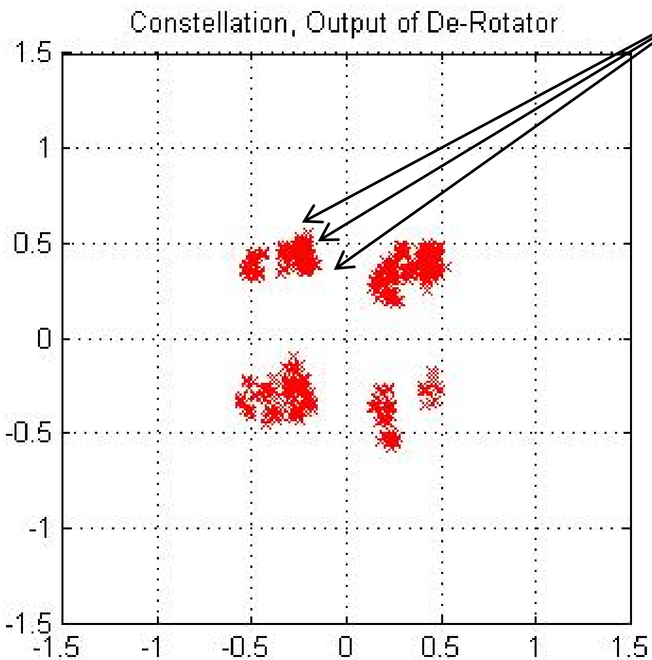
- Air-field testing for Line-of-sight data link provides massive multipath distortions: Constructive and destructive interference, see the selected sample below, taken over ~50K samples. Complete saturation (constructive interference) to 40 dB nulls (destructive interference) are seen:

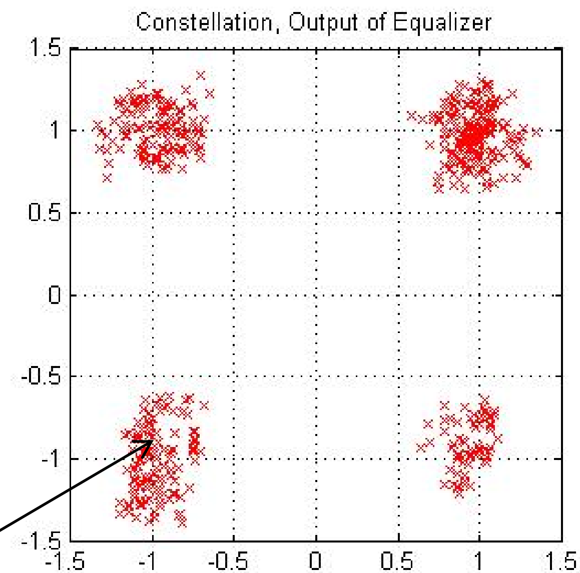


Field Test Data:
LOS @ 350 Mbps

- Even when the extreme fades are absent, multipath components are still severe. The image on the left illustrates the presence of multiple paths, and the constellation on the right is the equalized constellation.

Each ‘point’ is a possible indicator of an additional “multi-path’





The equalized constellation maximizes the Euclidian distance between valid points.

Field Testing, Sept 09

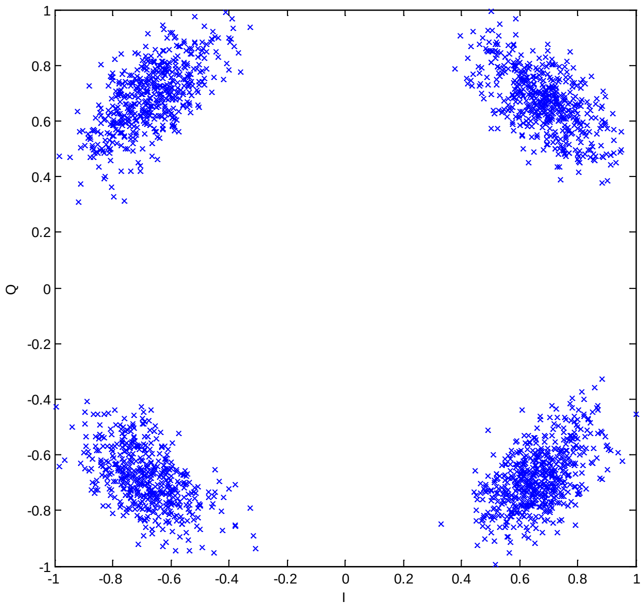
- Airborne node – Cessna 206
  - Risley Prism (Ball Aerospace)
  - C-MIGITS GPS/INS Tactical System
  - RF hardware
  - COTS modem (EBEM)
  - NRL modem
- Ground Node – 50 cm pedestal
  - NRL integration of DRS pedestal with RF electronics
  - TALIN INS with DAGR
  - Telemetry link - UHF

Testing Procedures

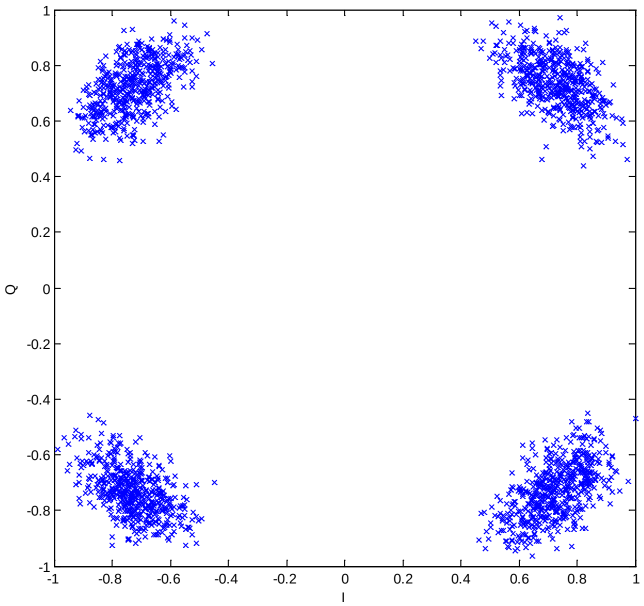
- All static testing (no flying)
  - Modem completed at very end of test window
  - Complications with aircraft antenna system
- Runway checkout
  - Verification of operation, use over RF path
- Short Range testing
  - 3 miles, NRL to National Harbor
  - Clear LOS with water crossing, multiple buildings
    - multipath

Runway Test (300 ft.) Received Constellations

Carrier Recovery Output (no EQ)

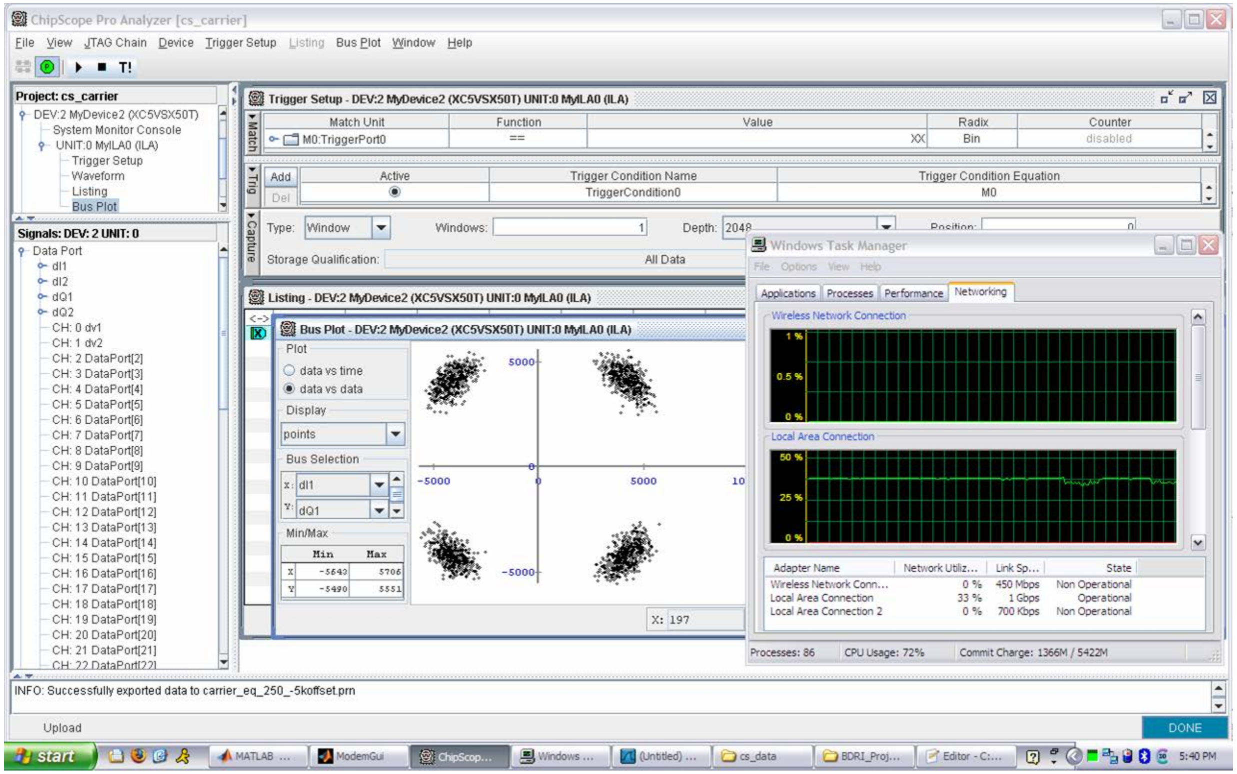


Carrier Recovery Output (with EQ)

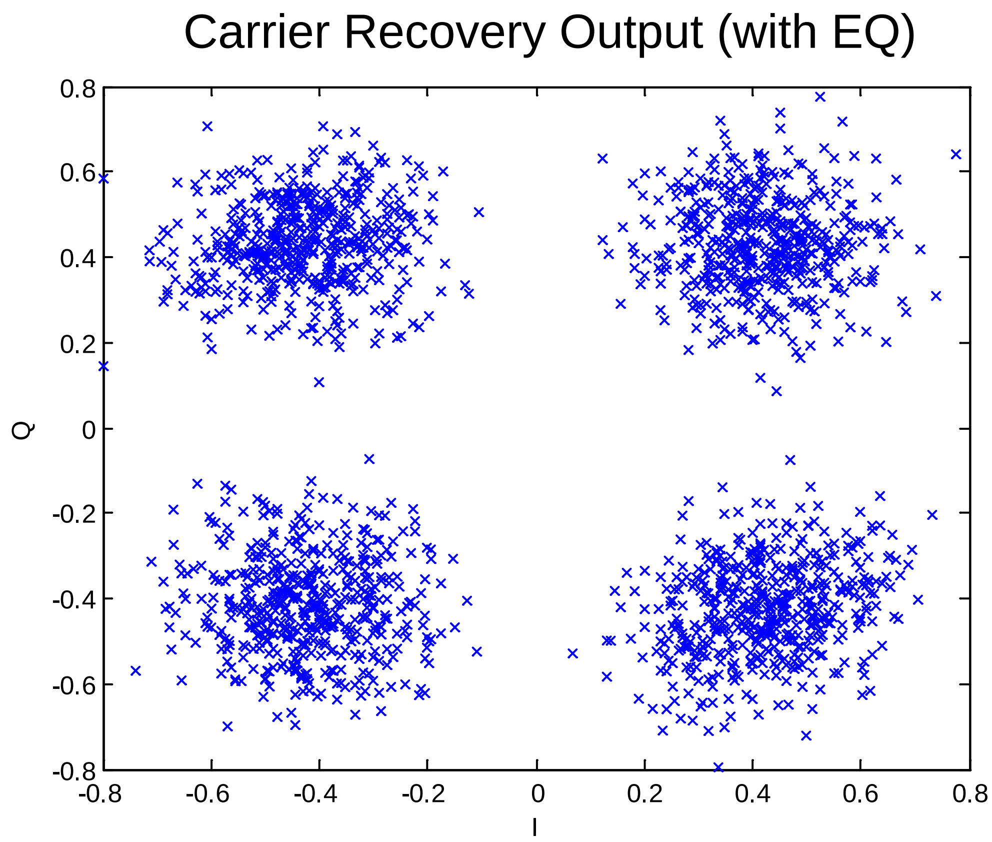


Runway Test Received Packets

- 100,000 Packets Collected
- Packet Size = 1024 kBytes
- BER = 5.7e-3
- Percentage of Packets without errors = 80%



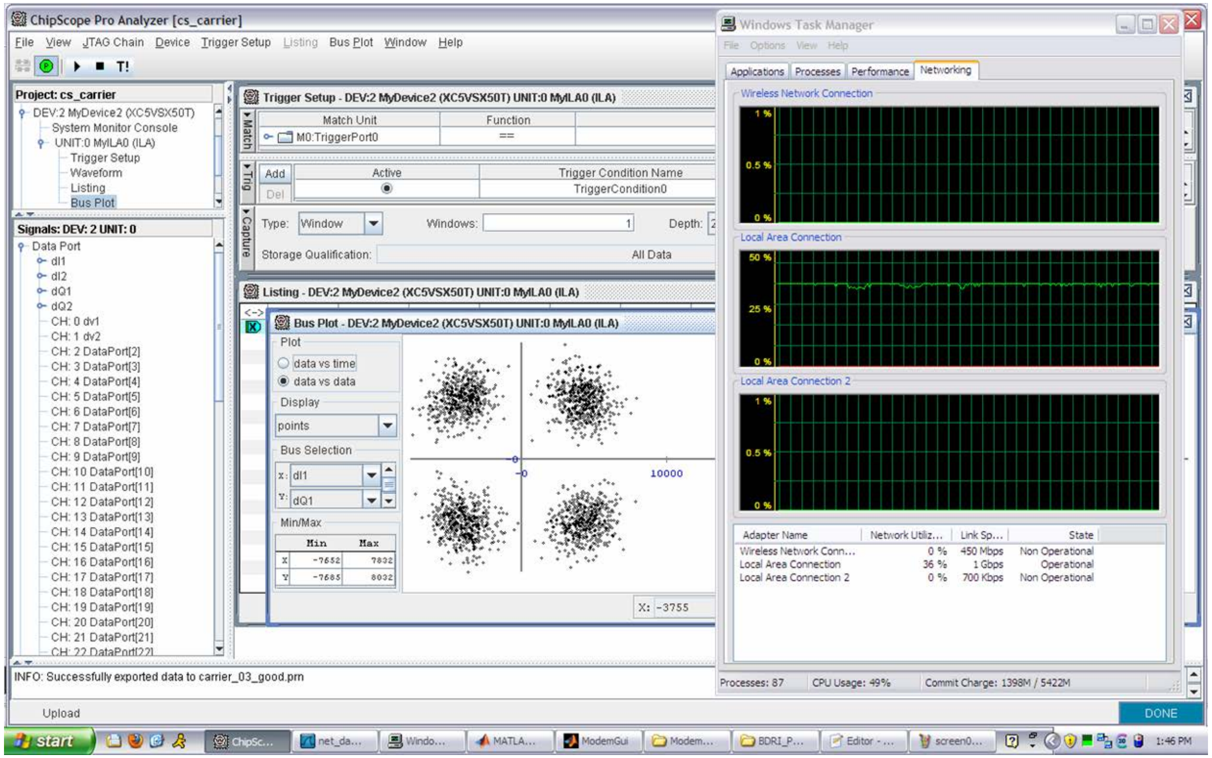
National Harbor Test (3 mi.) Received Constellation



Note: System would not lock without the equalizer enabled

National Harbor Test Received Packets

- 100,000 Packets Collected
- Packet Size = 1024 kBytes
- BER = 5.0e-3
- Percentage of Packets without errors = 50%



Future plans

- Continuing effort with ONR to develop & test very high speed modems with small form factor
  - Ongoing effort with ECC/Viasat
- Continued testing
- Limited availability to other government agencies
  - Development, testing

Back-up

Timing Recovery Rollover Conditions

- Accumulator rollovers can result in valid samples being duplicated or skipped.
- A second matched filter is used with static coefficients corresponding to the 0^{th} leg of the reloadable matched filter bank.
- Normal Operation: Samples from the reloadable coefficient matched filter are used.
- Accumulator Overflow: No samples during the symbol period are considered valid.
- Accumulator Underflow: Two valid samples are output during the symbol period (the first sample from the static filter and the second sample from the reloadable filter)