# On The Hardware Design of Front-End Processing in the SDR Systems

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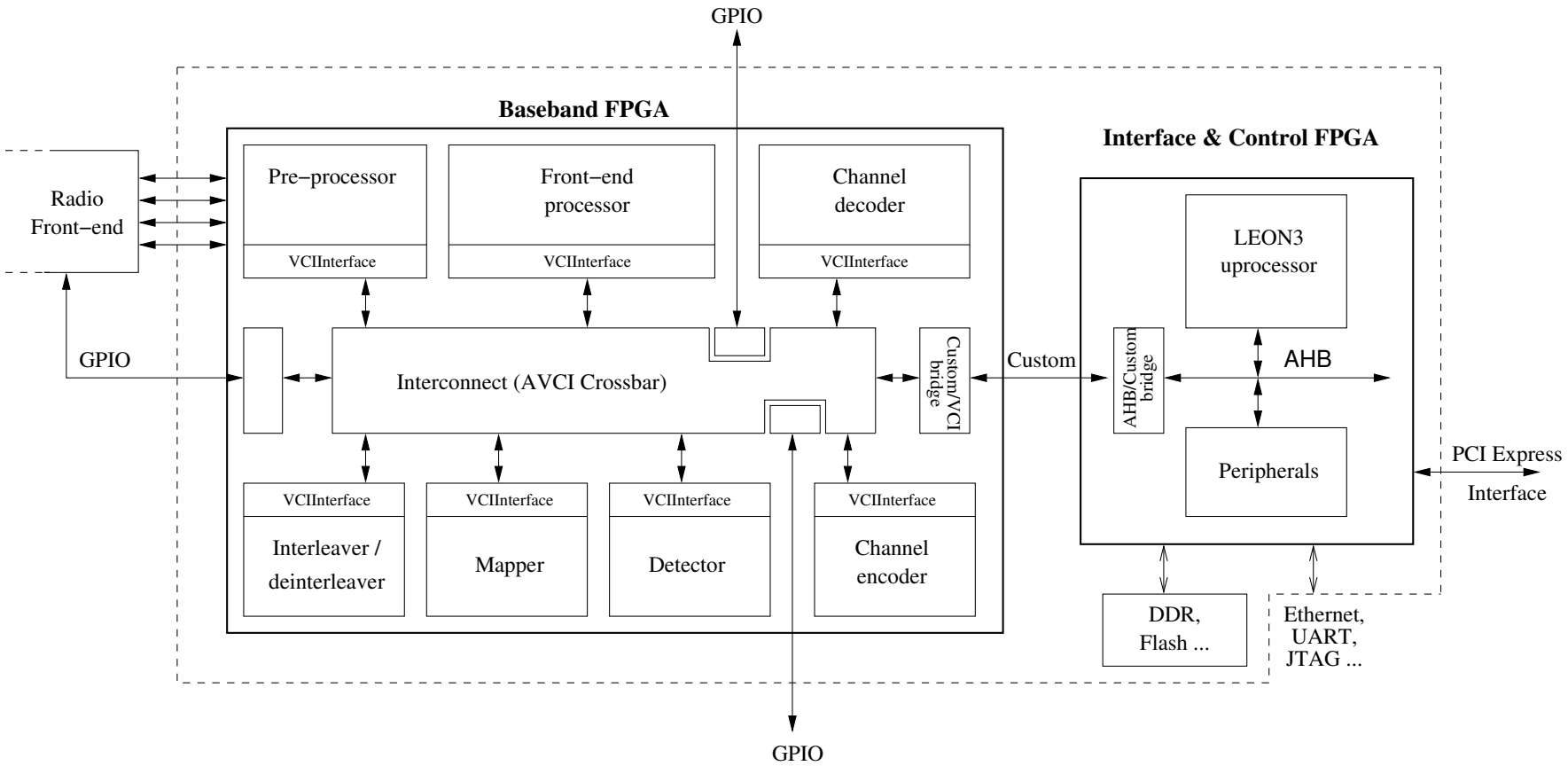
# Agenda

# Introduction

- Emergence of Multiple Wireless Communications Standards
- Motivations
  - Flexible (Reconfigurable) Platform
- Current Project
  - Flexible Efficient MODEM: Design and Implementation

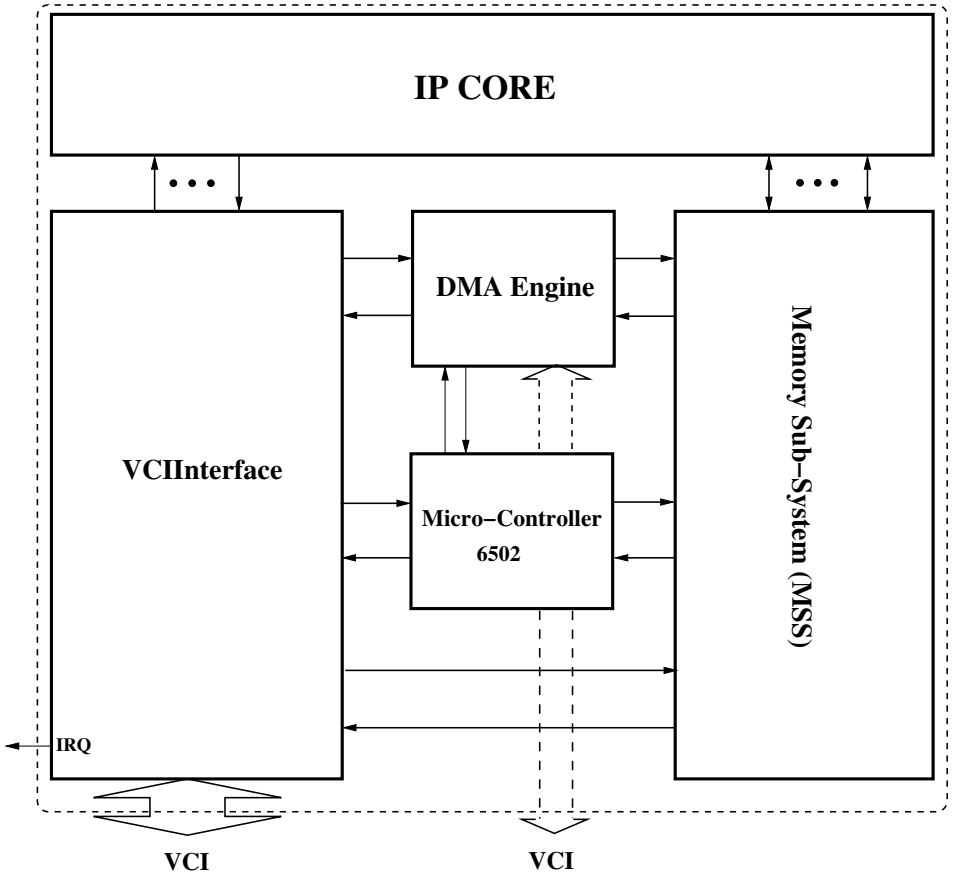
# System Architecture



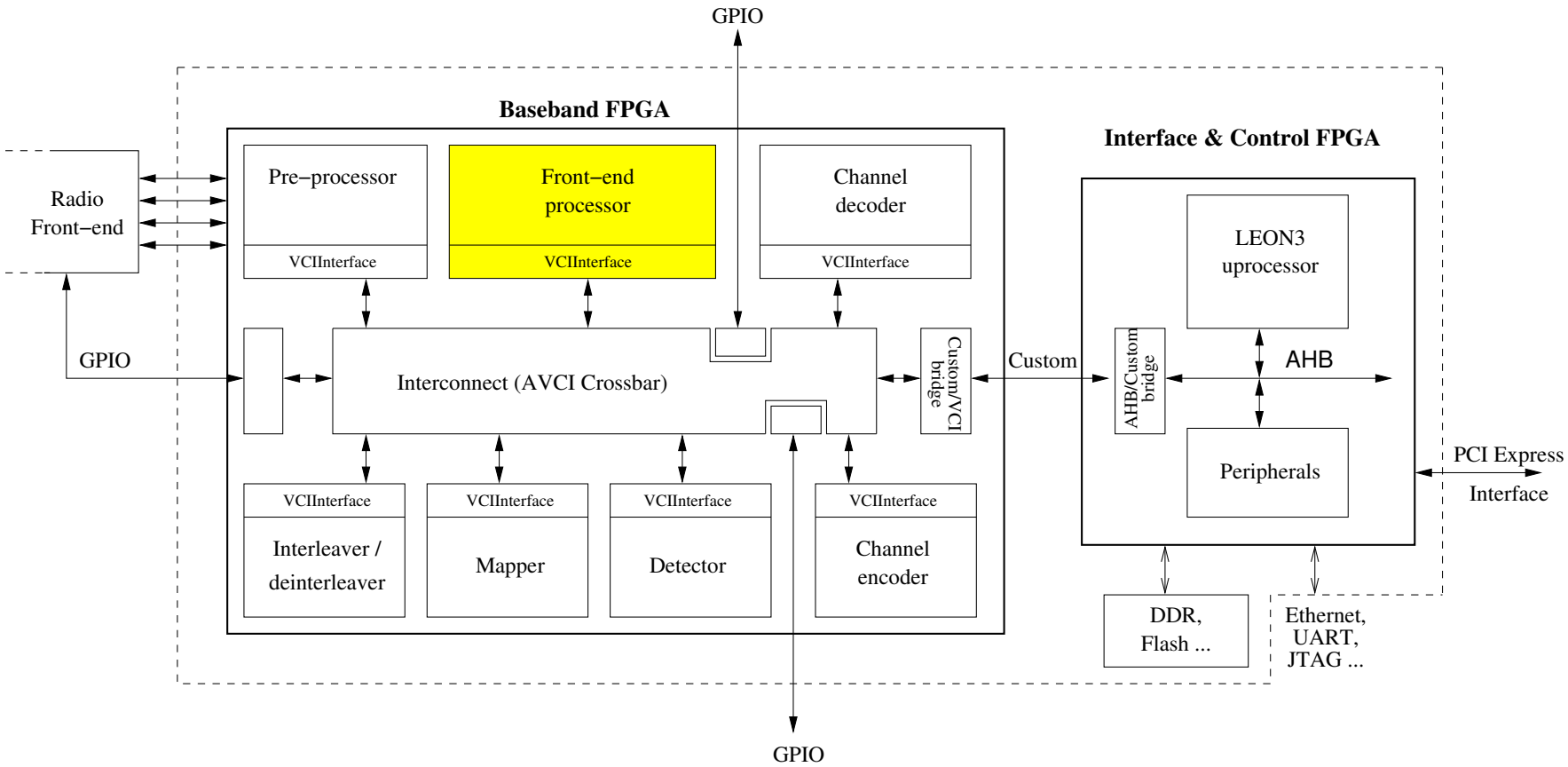
# System Architecture Details

- Interconnect
  - Generic Advaced VCI Compliant Crossbar Round robin arbitrator
  - Custom Bridge using AVCI and AHB
  - I/O blocks with SPI communication protocol
- Generic IP Shell
  - Generic design with 5 Sub-components
  - VCI Interface, DMA Engine
  - Micro-controller 6502
  - Memory Sub-system
  - Hardware Re-utilization
- Software / OS architecture
  - Software Thread for each Air-Interface
  - Three procedures: Tx, Rx, Syn
  - Parametrization of IP micro-controllers
  - LEON3 - eCos

# Generic IP architecture



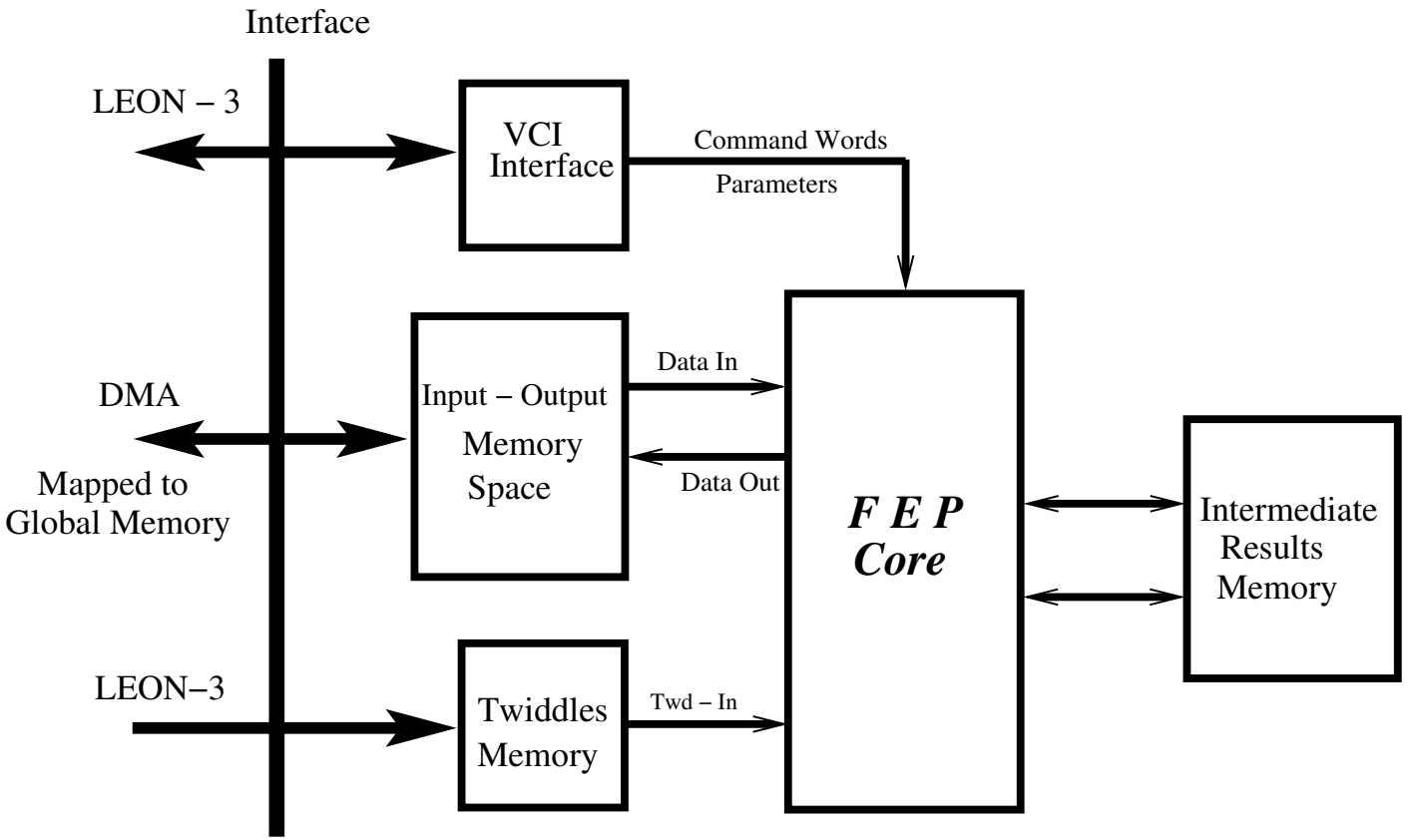
# Front End Processor



# Generic Front End Processor (FEP)

- Reconfigurable Air-Interface , Same HW / SW Architecture
- Generic Front-end for
  - MIMO / OFDMA
  - WCDMA
  - GSM
  - SCCP
- Capable of
  - Synchronization
  - Channel Estimation
  - Carrier Phase Offset (CPO) Compensation
  - Data Detection
  - Linear Matrix / Vector Processing

# Front End Processor Block Diagram



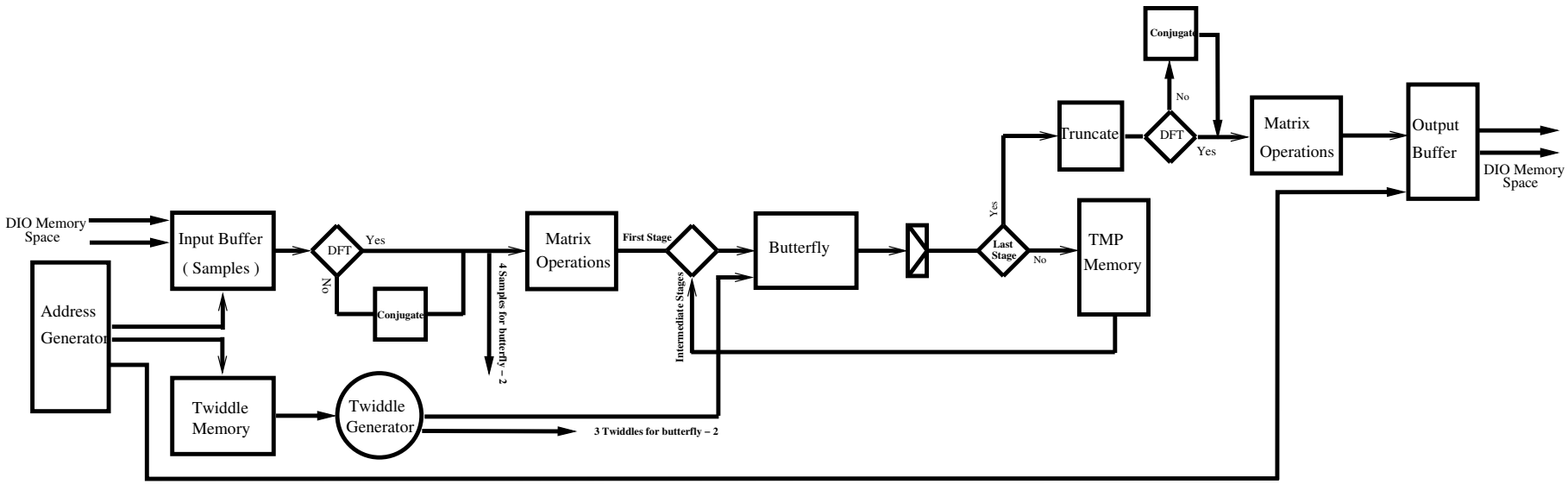
# Resource Requirements

- Throughput [ 1-sample / cycle, 2-samples / cycle ]
- Input - Output Complex Samples : 2's complement Q1.15 format
- Complex Additions
- Complex Multiplications
- Parallel Operations based on design specifications

# FEP - Processing Blocks

- Time / Frequency Conversion (DFT / IDFT)
- Operations Over Sub-band Level
  - Dot Product
  - Energy Calculations
  - Max, argMax Calculations
- Component-wise Operations Over Vectors (Addition, Product, and Division)

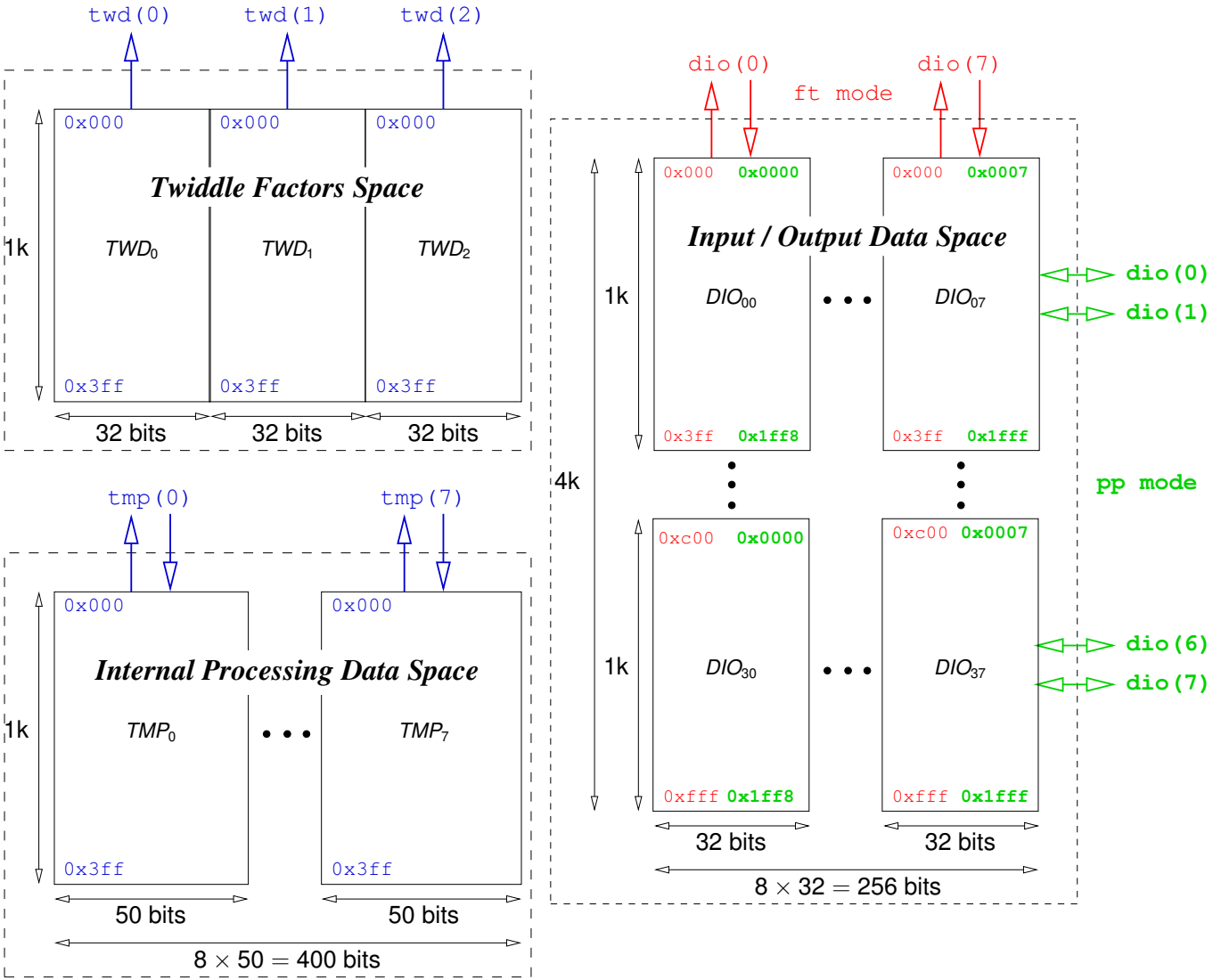
# The DFT / IDFT Processing Unit - Flow



# FEP - Memory Organization

- Shared Memory
- Priority Based Access
- Input Output Data Space (DIO)
- Twiddle factors memory space (TWD)
- Internal data processing memory space (TMP)
- Memory Access Modes
  - Fourier Transform mode - FT
  - Pre-Post Processing Mode - PP

# FEP Memory Layout : IP Core View



# Block Implementation

- 30 DSP48E slices - 16%
- DFT 135 MHz
- Vector Operations 150 MHz with 12 DSP slices
- Limitations
  - 4x4 Caches at the Input and Output
  - Mutually Exclusive Functionality

# DFT / IDFT Results

| DFT Size | # of Cycles | DFT Size | # of Cycles |
|---|---|---|---|
| 8 | 20 | 16 | 18 |
| 32 | 46 | 64 | 60 |
| 128 | 107 | 256 | 174 |
| 512 | 372 | 1024 | 695 |
| 2048 | 1597 | 4096 | 3136 |

Table: DFT : Number of cycles used for different Input Vector Sizes

# Conclusions

- Flexible Baseband Processing Architecture
- Macro Processing Blocks Approach
- Hierarchical Control Design
- Reasonable Resource Utilization
- Benchmarking and Comparative Analysis

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Thanks for Your Attention