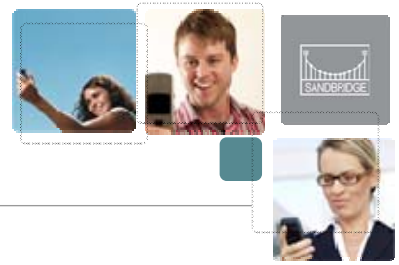
SANDBRIDGE TECHNOLOGIES

PERFORMANCE OF SELECT BASEBAND PROCESSING LTE UE BLOCKS ON A FLEXIBLE SOFTWARE BASED BASEBAND PROCESSOR

Babak Beheshti (Sandbridge Technologies, Tarrytown, NY; B.beheshti@ieee.org); Saurabh Lahoti (Sandbridge Technologies, Tarrytown, NY); Sitij Agrawal (Sandbridge Technologies, Tarrytown, NY); Daniel Iancu (Sandbridge Technologies, Tarrytown, NY); John Glossner (Sandbridge Technologies, Lowell, MA)



Introduction

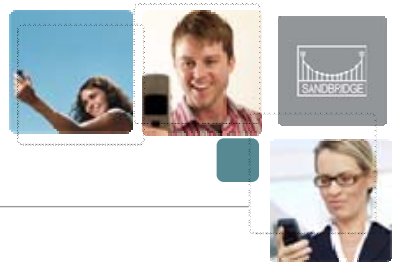
- In this paper novel approaches to implementation of several processing blocks required in the LTE standards are analyzed and benchmarked. In particular, implementation of the algorithms is assumed to be based on a flexible software based baseband processor. The blocks discussed in this paper are the FFT, the DFT and the Viterbi Decoder.

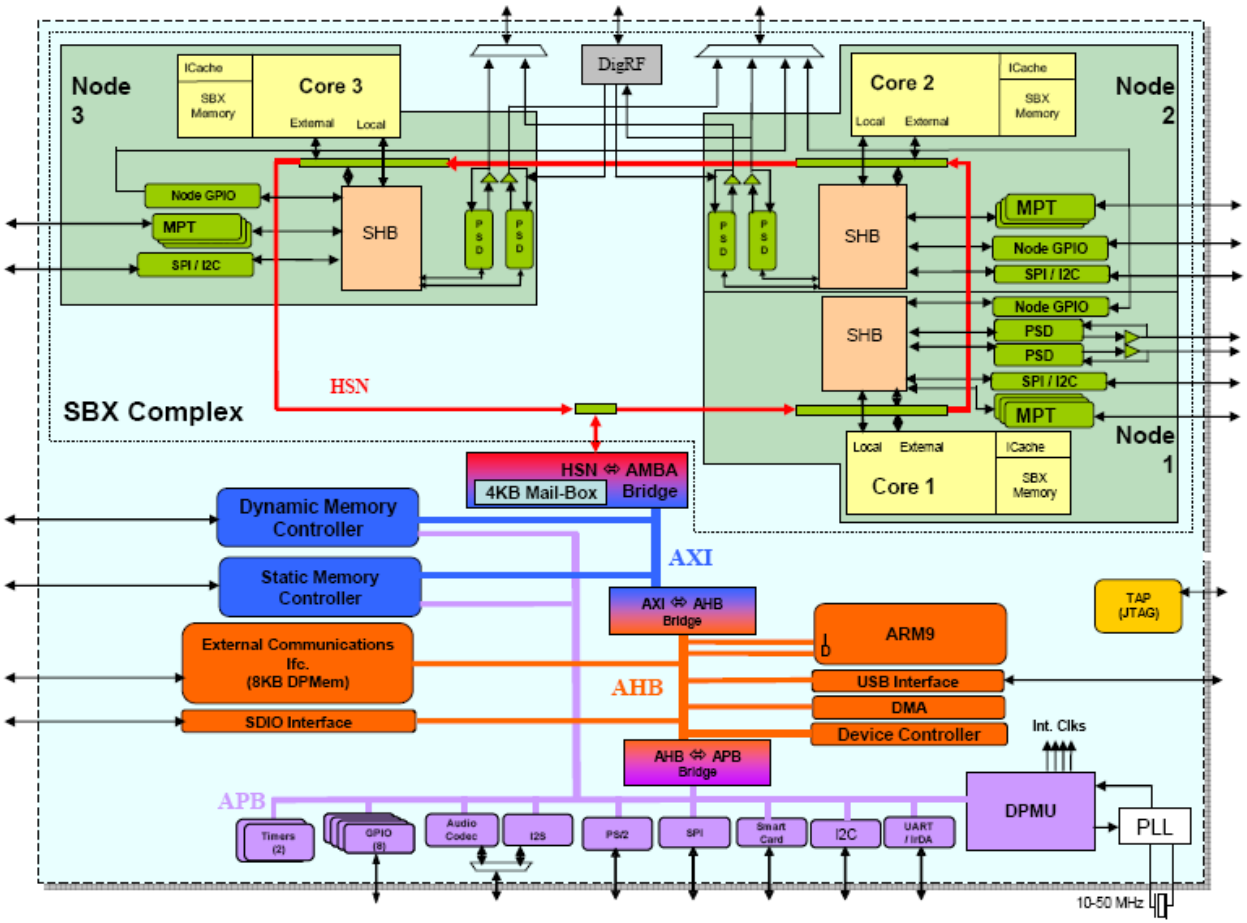
The Target Baseband Processor

The SB3500 is the second generation of SandBlaster-based low power, high performance System on a Chip (SoC) products developed to serve the Software Defined Radio (SDR) modem applications space.

It is a multi-core device, containing 3 'SBX' DSP cores and an ARM926 processor, all interconnected by a high speed network (HSN).

SB3500




Node 3
ICache
SBX Memory
Core 3
External
Local
DigRF
Core 2
ICache
SBX Memory
Local
External
Node 2
Node GPIO
MPT
SPI / I2C
SHB
PSD
PSD
SHB
MPT
Node GPIO
SPI / I2C
SHB
Node GPIO
PSD
PSD
SPI / I2C
MPT
HSN
SBX Complex
Local
External
ICache
SBX Memory
Core 1
Node 1
HSN ⇔ AMBA Bridge
4KB Mail-Box
Dynamic Memory Controller
Static Memory Controller
AXI
AXI ⇔ AHB Bridge
ARM9
TAP (JTAG)
External Communications Ifc. (8KB DPMem)
SDIO Interface
AHB
USB Interface
DMA
Device Controller
Int. Clks
AHB ⇔ APB Bridge
APB
Timers (2)
GPIO (8)
Audio Codec
I2S
PS/2
SPI
Smart Card
I2C
UART / IrDA
DPMU
PLL
10-50 MHz

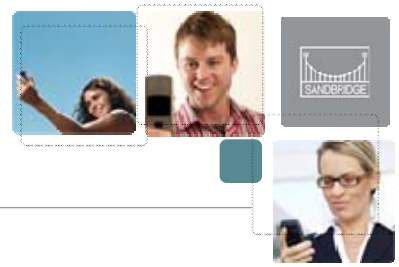
DISCRETE FOURIER TRANSFORM

This code is a mixture of functions which perform variable-size DFT's on 16 bit I/Q data.

This is performed by utilizing the generalized Cooley-Tooky factorization method in which a DFT input block (which is not a power of two in size) can be decomposed into radix-2 FFT's and then reassembled to obtain the correct output.

The radix-2 FFT's in this case are performed using the existing 4,8,16,32,64, and 256 RPU FFT blocks.

DISCRETE FOURIER TRANSFORM

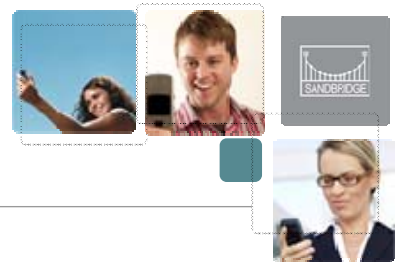


The reassembly is performed by utilizing RPU complex multiply instructions to multiply the radix-2 FFT outputs by specialized DFT twiddle factors. To reduce code size and complexity, only branch-3 and and branch-5 factorizations were utilized.

For example, to perform a 360-sized DFT, the complex-valued input block would be factorized as follows:

360 DFT = 5 * 72 DFT's = 5 * (3 * 24 DFT's) = 5 * [3 * (3 * 8 FFT's)]

DFT INTERLEAVING

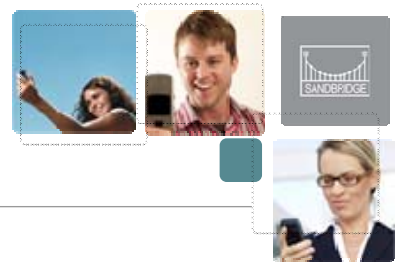


For each DFT size, interleaving is done once on the input data. The interleaving performs both decimation (by 3 or by 5 depending on the factorization) as well as the necessary bit reversal (always done for any FFT) all in one.

For each DFT there is a specific interleaving required depending on how the DFT is factored.

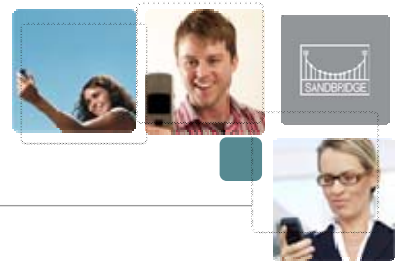
The SB3500 scatter DMA is used to speed up interleaving.

DFT INTERLEAVING



In accordance with the LTE standard, the following DFT sizes were implemented and tested on the SB3500 hardware: 12, 24, 36, 48, 60, 72, 96, 108, 120, 144, 180, 192, 216, 240, 288, 300, 324, 360, 384, 432, 480, 540, 576, 600, 648, 720, 768, 864, 900, 960, 972, 1080, 1152, 1200, 1296

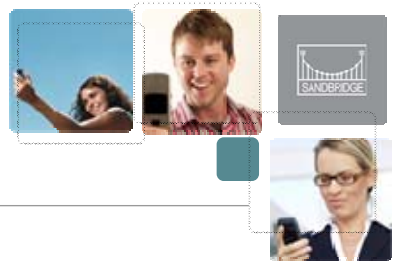
PERFORMANCE RESULTS



In each case, the amount of time to perform the actual DFT is less than the LTE real-time constraint for the sb3500 (~10700 thread cycles) when sampling at 30.72 Mhz.

Furthermore, note that the DMA can be performed concurrently with other operations and so its latency can be completely hidden and absorbed.

FAST FOURIER TRANSFORM



The formula for cycles in an N point FFT is:

(N/8)*logN + (N/3), N <= 16

(N/6)*(logN + 1), N > 16

For the examples coded up that yields:

64 point : 75 cycles

256 point : 384 cycles

512 point: 853 cycles

1024 point: 1878 cycles

2048 point: 4096 cycles

4096 point: 8875 cycles

VITERBI DECODER

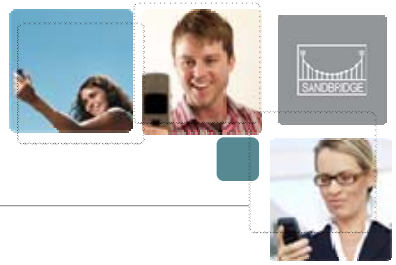
These routines implement different versions of a 1/3 rate, variable-length, SIHO Viterbi decoder designed for a k=7, tail-biting code.

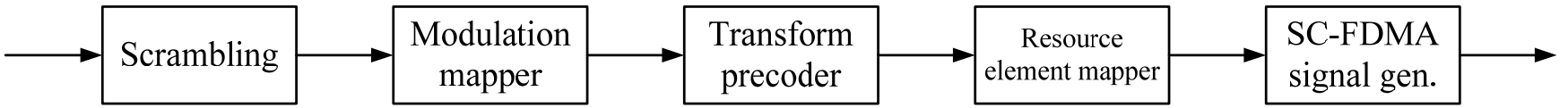
Note that, in this case, none of the symbolic bits are systematic (this is based upon a 100% parity code).

The optimized, pipelined, decoder is designed to be the central piece in the LTE blind decoding process for the PDCCH.

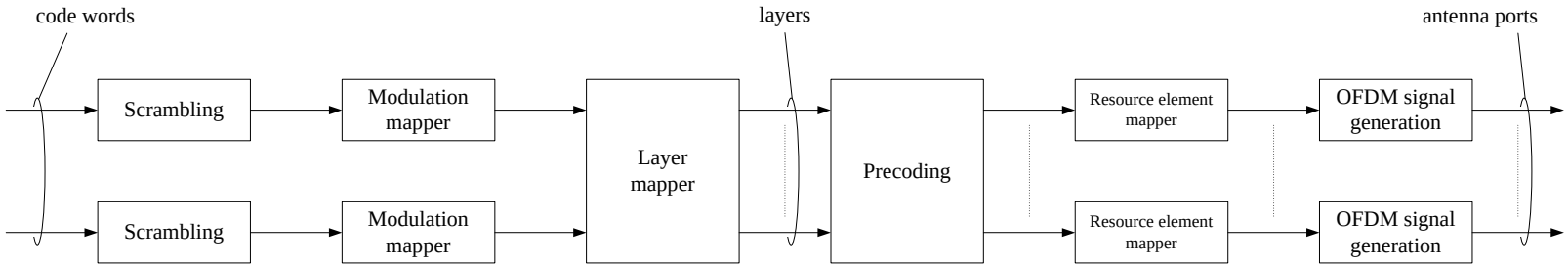
The decoder is designed to perform decoding for all DCI sizes specified in the standard and achieves a performance of 6 cycles per decoder output bit.

UL

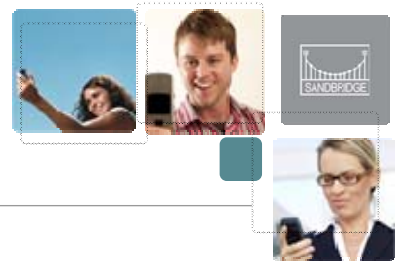


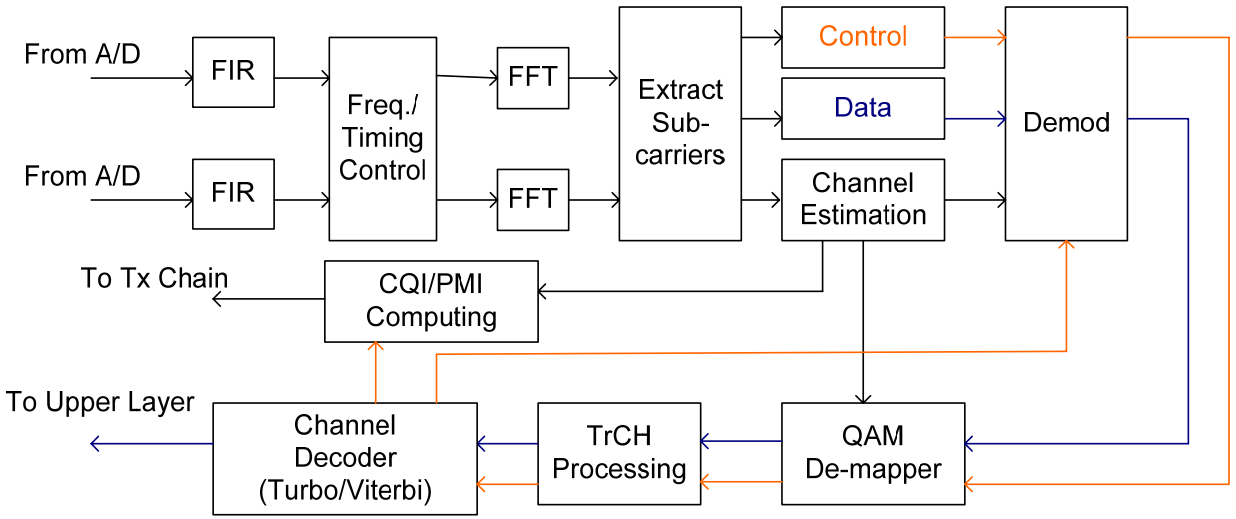

Scrambling
Modulation mapper
Transform precoder
Resource element mapper
SC-FDMA signal gen.

DL PHYSICAL LAYER PROCESSING

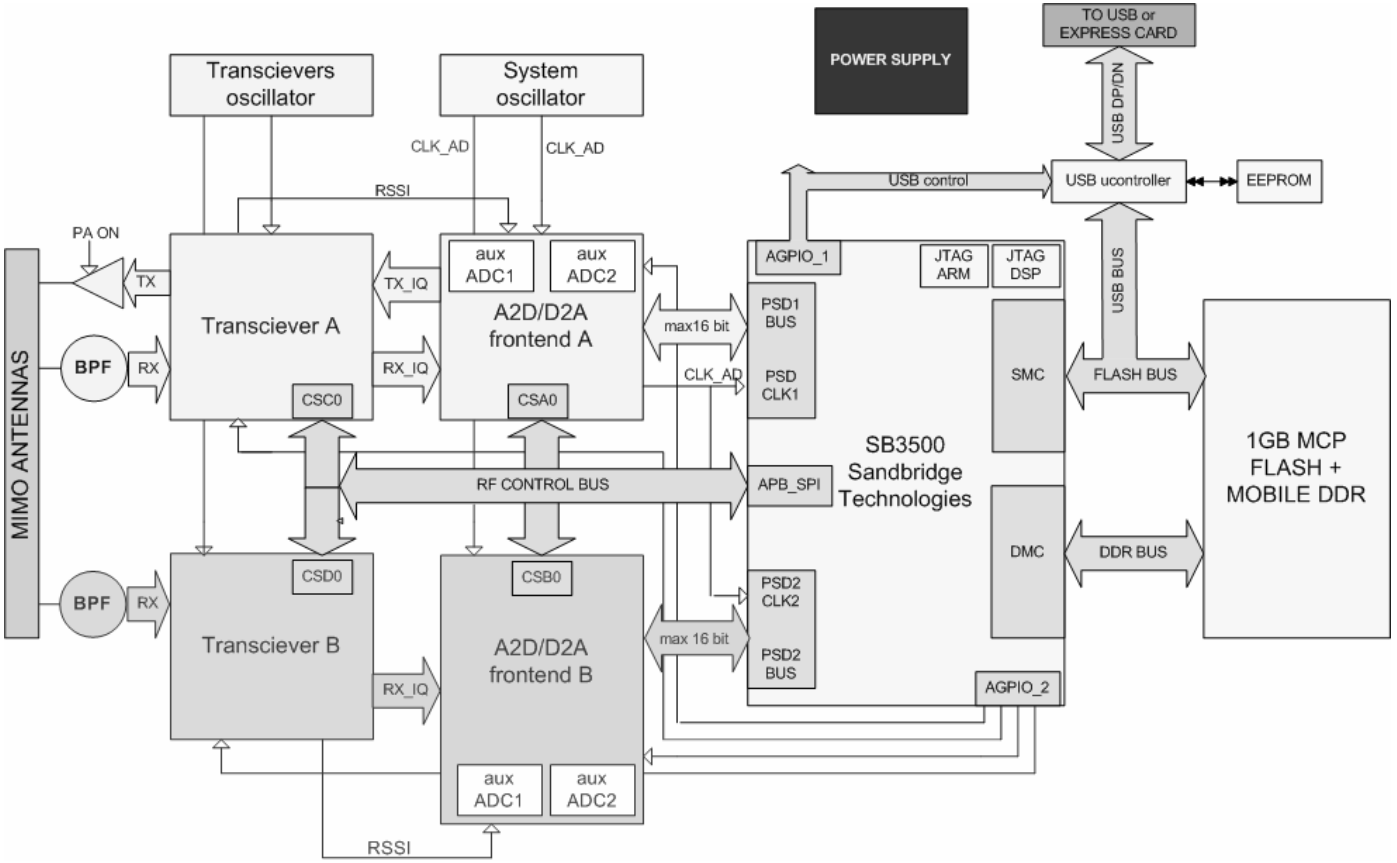


DL RECEIVER BLOCKS

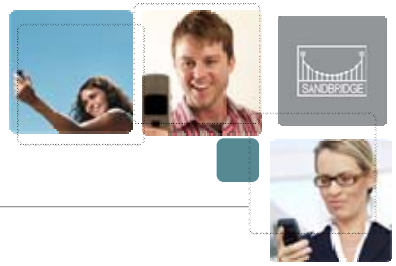


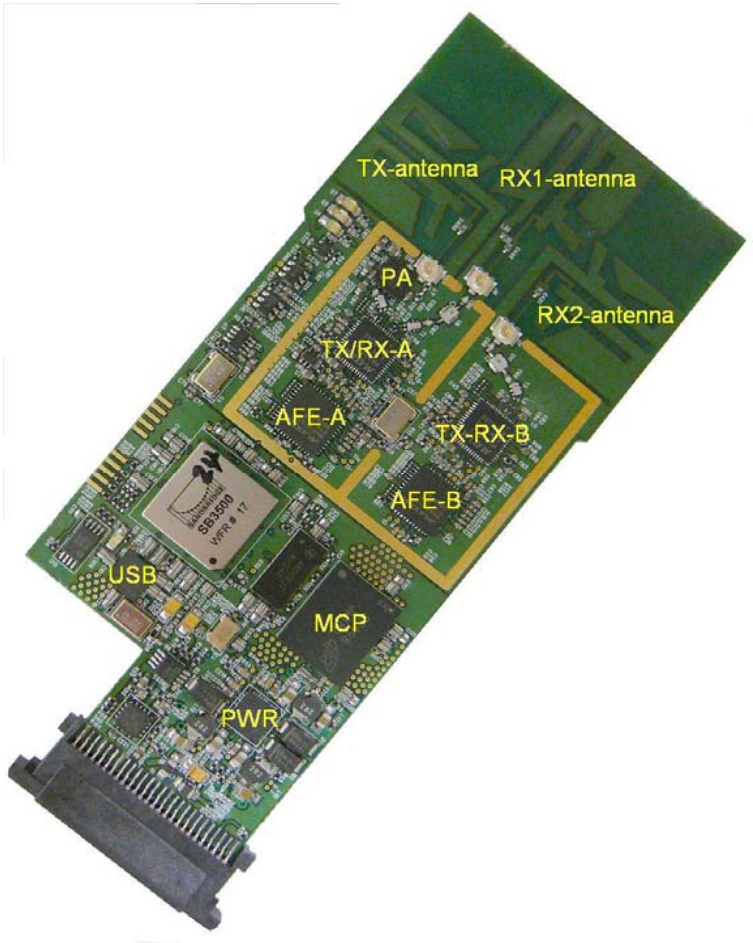


SDR PLATFORM



SDR PCI-E CARD





TX RESULTS

Agilent 89600 Vector Signal Analyzer - Press the Mode key to switch applications

File Edit Control Source Input TestSetup MeasSetup Display Trace Markers Utilities Help

A: Ch1 OFDM Meas Range: 10 V
1.5
Const
300 m /div
-1.5
-1.356 1.3558

C: Ch1 OFDM Err Vect Spectrum
20 %
LinMag
2 % /div
0 %
Start: -300 carrier Stop: 299 carrier
RBW: 15 kHz TimeLen: 42 Sym

E: Ch1 OFDM Err Vect Time 10 V
20 %
LinMag
2 % /div
0 %
Start: 0 sym Stop: 41 sym

B: Ch1 Spectrum Range: 30 dBm
-15 dBm
LogMag
15 dB /div
-165 dBm
Center: 2.5 GHz Span: 25 MHz
RBW: 1.27313 kHz TimeLen: 3 mSec

D: Ch1 Error Summary Range: 10 V

EVM	= 3.2636	%rms at
EVM Pk	= 15.605	% at
Data EVM	= 3.2814	%rms
- 3GPP-defined QPSK EVM	= —	
- 3GPP-defined 16QAM EVM	= 3.2817	%rms
- 3GPP-defined 64QAM EVM	= —	
RS EVM	= 3.1542	%rms
RS Tx. Power (Avg)	= —	
OFDM Sym. Tx. Power	= —	
Freq Err	= -17.451	kHz
SyncCorr	= 99.774	% usi
Common Tracking Error	= 109.03	m%rms
SymClk Err	= 0.30581	ppm
Time Offset	= 3.7607	msec
IQ Offset	= -42.053	dB
IQ Gain Imbalance	= -0.025	dB
IQ Quad. Error	= -1.9233	deg

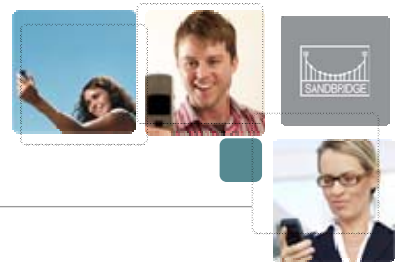
F: Ch1 Frame Summary Range: 10 V

Channel	EVM(%rms)	Power(dB
User01		
- PUSCH_QPSK	—	—
- PUSCH_16QAM	3.2814	-0.0081
- PUSCH_64QAM	—	—
- PUSCH_DMRS	3.1542	0
Non-alloc	2.3579	—

Trace B Power: -6.298 dBm

Doing demodulation... LTE INT REF AUTOCAL: OK A F E (abs)

QUESTIONS



THANK YOU FOR YOU ATTENTION