New FPGAs Revolutionize Digital Down Converters

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Software Defined Radio Forum
Technical Conference and Exhibition
Topics

- New FPGA Technology
- FPGAs Invade Software Radio
- Traditional Digital Downconverter Architectures
- Channel Bank Digital Downconverters
- Summary & Resources
What are FPGAs? Why are they so popular?

- Field Programmable Gate Arrays
  - Monolithic silicon devices with memory, CPU and logic resources
  - User programmable interconnections support custom configurations

- How Can FPGAs Outperform DSPs?
  - DSP chips have 4-8 multipliers - FPGAs can have over 1000
  - DSP chips execute sequential instructions to implement algorithms
  - FPGAs execute multiplications using hardware multipliers in parallel
  - FPGA hardware architecture can be optimized for each algorithm

- How Can FPGAs Replace ASICs?
  - ASICs have dedicated hardware for specialized processing
  - FPGAs can be reconfigured to perform the same processing
  - ASICs require long design cycle and expensive tooling
  - Flexible FPGA hardware faster to design with no tooling charges
FPGAs - New Device Technology

- 550+ MHz DSP Slices and Memory Structures
- Over 1000 dedicated on-chip hardware multipliers
- On-board GHz Serial Transceivers
- Partial Reconfigurability Maintains Operation During Changes
- Switched Fabric Interface Engines
- Gigabit Ethernet media access controllers
- Over 330,000 Logic Cells
- On-chip PowerPC RISC micro-controller cores
- Memory densities approaching 20 million bits
- Reduced power with core voltages at 1 volt
- Silicon geometries to 65 nanometers
- High-density BGA and flip-chip packaging
- Over 1200 user I/O pins
- Configurable logic and I/O channel interface standards
New Xilinx Virtex 5: Four Sub-Families

- **LX Devices**
  - Announced May 2006
  - *Maximum Logic Resources*

- **LXT Devices**
  - Announced October 2006
  - Extension of LX family
  - Gigabit Serial Transceivers
  - Ethernet MACs
  - PCI Express Endpoint

- **SXT Devices**
  - Announced February 2007
  - *Maximum DSP Resources*

- **FXT Devices**
  - Announced May 2008
  - Embedded System Resources

- **Footprint Compatibility**
  - Among LXT, SXT, & FXT
  - One PCB Design
  - Many Applications
What’s New in Virtex-5?

- Lower Power Dissipation
  - 1.0 volt core voltage with 65 nm Copper Process
- Faster Clock Speeds for Faster Execution
  - Up to 550 MHz
- Advanced Clocking Architecture
  - Up to 18 Clock Generators, PLLs, Jitter Reduction Filters
- Enhanced DSP48E Engine for Improved DSP Execution
  - 18 x 25 Hardware Multipliers – 550 MHz
- Faster Select I/O Technology
  - 800 MHz Single ended – 1.25 GHz Differential
- Dedicated PCI Express Endpoint Engine
  - x1, x2, x4, or x8 Lane Support for Each Block
  - 3.2 GHz and 6.25 GHz Serial GTP RocketIO Physical Interfaces
FPGA Evolution Targets SDR Applications

- Each generation of FPGA adds new features
- Each new feature directly benefits software defined radio

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<th>V-4 SX SX55</th>
<th>V-4 FX FX100</th>
<th>V-5 LX LX330</th>
<th>V-5 LXT LX330T</th>
<th>V-5 SXT SX240T</th>
<th>V-5 FXT FX200T</th>
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Topics

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Typical Software Radio System

- RF Signals are down converted to IF frequencies
- A/D converter digitizes the IF signal
- Mixer and Local Oscillator translates IF to baseband
- Digital FIR low pass defines signal output bandwidth
- DSP performs demodulation, decoding, decryption, error correction, analysis, FFT, control, etc.
Traditional Software Radio Implementations

- **RF TRANSLATOR**
- **LOW PASS FILTER**
- **DIGITAL MIXER**
- **DIGITAL LOCAL OSC**
- **A/D CONV**
- **DIGITAL RECEIVER ASIC**
- **ANALOG RF CIRCUITRY**
- **RF ASIC**
- **ANALOG RF CIRCUITRY**
- **RF ASIC**
- **DIGITAL DOWN CONVERTER (DDC)**
- **CPU or DSP**
- **FORMAT CONTROL OPERATOR I/F**
- **DEMOD DECODE DECRYPT**
- **ANALYZE (FFT)**
- **PULSE COMPRESSION**
- **ERROR CORRECTION CORRELATION**
- **AVERAGE FILTER EXTRACT**
- **DECOMPRESS RECONSTRUCT ENHANCE**
FPGA Software Defined Radio Module

- **Virtex-5 FPGA Functions**
  - Four 200 MHz 16-bit A/D Interfaces
  - SDRAM Controllers 330 MHz DDR2
  - Data Formatting & Routing
  - Timing, Gating, Triggering, & Sync

- **DDC Functions**
  - DMA Controller
  - Gigabit Serial XMC Interface
  - PCI Express Protocol Engine
  - PCI 2.2 Interface

![Virtex 5 SX95T Diagram]

CH A RF In

CH A RF In

CH C RF In

CH D RF In

Clock & SYNC Bus

PCI Bus

512 MB SDRAM

512 MB SDRAM

512 MB SDRAM

Gigabit Serial Interface

PCI Express Engine

PCI 2.2 Interface

DMA Controller

Routing Formatting Control Status

DDC

512 MB SDRAM

512 MB SDRAM

512 MB SDRAM

XMC Connector for Switched Serial Fabric

Pentek Model 7150

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**Spectral Utilization for SDR Systems**

- **Typical applications for DDCs and their required bandwidths**
  - **Communications**
  - **Radar**

![Diagram showing spectral utilization for SDR systems with various bandwidths and channel counts for typical applications like Communications and Radar.](image-url)
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FIR Filter DDC Architecture

- Simplest Digital Down Converter Implementation
- Better for Wideband DDCs with Low Decimation
- Uses More Multipliers for High Decimation – Narrow BW

**Diagram:**

- **Freq Translation**
  - Complex Mixer
  - Wide-Band Input
  - Q

- **Channel Filter**
  - FIR Filter & Rounding
  - Narrow Band Complex Output
  - Q

- **Components:**
  - Sin/Cos LUT
  - Phase ACC
  - Tuning Freq
  - Digital Local Oscillator
  - Coefficients
  - User
Model 7153: 4 Channel Wideband DDC

- 4 Wideband DDC channels, each individually tunable
- Decimation range of 2 to 256, independent per channel
- Power Meters, Threshold Detectors, & Beamforming Summation Block
Model 7153: 2 Channel Multiband DDC

- 2 Cascaded Wideband DDC channels, each individually tunable
- Decimation range of 2 to 65,536 (decimation of each DDCs multiplies)
- Power Meters, Threshold Detectors, & Beamforming Summation Block
7153 2- or 4-Channel Multi-Band DDC PMC

- Channel Bandwidth: 2.5 kHz to 80 MHz (2 Ch) or 625 kHz to 80 MHz (4 Ch)
- Covers 3G and 4G communications wide bandwidths
- Covers many wide-band Radar applications

Diagram showing bandpass settings for various communications standards.
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CIC Filters Save Multipliers
Better for High Decimation Narrowband Channels
Compensation Filter Corrects CIC Frequency Response
But, CIC type DDCs still require significant resources
Achieving High Channel Count DDCs

- **Channel Bank DDC Principles**
  - Divide input signal bandwidth using multiple band pass filters
  - Choose the most appropriate filter for signal of interest
  - Perform fine tuning downconversion using FIR type DDC
  - Fine tuning DDC operates at much lower sample rate
  - Fine tuning DDC hardware is multiplexed across many channels

- **Fundamental Problems of Channel Bank DDCs**
  - Flatness across band pass filter span
  - Response “notches” or dropout between band pass filter bands
    - Restricts free tuning across input bandwidth
  - Challenge: Build flat filters with no dropout between bands !!
Proprietary overlapping filters with flatness compensation
Model 7152: 32 Channel Bank DDC

- 32 Channel Bank DDC channels, each individually tunable
- Decimation range of 16 to 8192, independent for each 8-channel bank
- Power Meters, Threshold Detectors, & Beamforming Summation Block
Channel Bandwidth: 25 kHz to 10 MHz for Fs = 200 MHz
- High channel count
- Covers most communications bandwidths and many Radar bandwidths
Channel Bank DDC with 256 Channels, each individually tunable
Decimation range of 1024 - 9984, common decimation for all channels
Targeted for VP50 FPGA and 125 MHz A/D Converters
7141-430: 256-Channel Narrow Band DDC

- Channel Bandwidths: 10 kHz to 100 kHz for 125 MHz Fs
  - Covers many VHF, UHF, SATCOM bandwidths with one board
  - Covers 1G communications and AMP EDGE bandwidths

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Model 7151: 256 Channel Bank DDC

- Channel Bank DDC with 256 channels, each individually tunable
- Decimation range of 128 - 1024, independent for each 64-channel bank
- Targeted for Virtex 5 and 200 MHz A/D Converters
7151: 256-Channel Medium Band DDC PMC

- Channel Bandwidths: 156 kHz to 1.25 MHz for Fs = 200 MHz
  - Covers all GSM channels with one board
  - Covers 2G and 3G CDMA2000 bandwidths
Comparison: FPGA vs. ASIC

- GSM 2G Receiver Example
  - E-GSM has 175 Channels at 200 kHz spacing
  - Comparison –
    - Prior to 2008 - Pentek 7131
      - 4 – Quad GC4016 ASICs per board
    - Year 2008 - Pentek 7151
      - 1 – Xilinx Virtex-5 SX95T with FPGA Core

175 Channels would require 44 GC4016 or GC5016 ASICs!
Cost / Space / Power Savings over ASICS

- Example: 175 channel GSM-E software radio receiver

- Cost Per Channel
  - ASIC: $563
  - FPGA: $69

- Qty of Boards
  - ASIC: 11
  - FPGA: 1

- System Power
  - ASIC: 88 W
  - FPGA: 30 W

- Higher Channel Count Systems Strongly Favor FPGA Designs
Efficient 256 Channel FPGA DDC Design

- 7151 core design requires approx 30,000 lines of VHDL code
- Entire core fits inside one SX95T device
- Traditional narrow band DCC based on Xilinx CIC and FIR structures requires ten SX95T devices
Overview of New Pentek DDC IP Cores

* Assumes 100-200Mhz Sample Rate.

Bandwidth (MHz)

* Assumes 100-200Mhz Sample Rate.
Presentation Topics

- Military Electronic System Requirements
- New FPGA Technology
- Traditional Digital Downconverter Architectures
- Channel Bank Digital Downconverters
- Summary & Resources
Summary

- **Traditional Filter DDCs**
  - Excellent for Wideband DDCs
  - Simple FPGA design
  - Consumes many resources for higher decimations
  - Not attractive for high channel densities

- **CIC Filter DDCs**
  - Saves hardware multipliers
  - Popular in ASIC devices
  - Not attractive for high channel densities

- **Channel Bank DDCs**
  - Economical for High Channel Count DDCs
  - Suitable for medium to high decimations
  - Extremely challenging channel bank filter design
  - High complexity FPGA design
FPGA Technology for Software Radio

- Pentek (DSP, Software Radio): www.pentek.com
- Pentek (FPGA Resources): www.pentek.com/gateflow
- Xilinx (FPGAs, Fabric IP Cores, Gigabit I/O): www.xilinx.com
- Altera (FPGAs, Fabric IP Cores, Gigabit I/O): www.altera.com