A WIDE BAND SPECTRUM SENSING APPROACH WITH AGILITY AND LOW SNR SENSITIVITY

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ABSTRACT

Sensing-based opportunistic spectrum access is a critical component in cognitive radio applications. The first challenge is to design a signal detector that can quickly search through a wide bandwidth for vacant spectrum in order to establish a new channel. Further, the cognitive radio has to switch agilely to another channel when a primary user appears. Primary users' signals may be at a very low SNR and operate dynamically. Cyclostationary features detection is attractive for detecting primary users, since it is known to be adept at signal detection and classification with high sensitivity. However, a key issue of cyclostationary signal analysis is the high computational complexity arising from the large number of required complex convolution operations. In addition, the computation requirement increases significantly in proportion to the bandwidth to be covered. These factors limit receiver agility and sensitivity.

To reduce the computation requirement, we use parallel computing in cyclostationary feature analysis running on a Cell Broadband Engine (Cell BE), which has a peak performance exceeding 200 GFlops for single precision floating point operation. Our test system is a Universal Software Radio Peripheral (USRP) board connected to a Cell BE powered PlayStation 3 with GNU Radio installed. Our cyclostationary feature computation exploits all six usable Synergistic Processing Elements in the PlayStation 3. The signal detector is implemented in our Public Safety Cognitive Radio node following a newly designed spectrum sensing scheme that incorporates channel monitoring, data transmission, and dynamic spectrum switching. During the data transmission, a channel search is continuously running to collect available spectrum and updating the most recent spectrum in a database, which will be used for dynamic spectrum switching. The test frequency range covers the VHF TV band and the 700 MHz Public Safety band.

1. INTRODUCTION

The limited available spectrum and the inefficiency in the spectrum usage necessitate a new communication paradigm to exploit the existing wireless spectrum opportunistically, such as Dynamic Spectrum Access and cognitive radio networks [1]. A critical requirement for opportunistic spectrum sharing is to sense the spectrum holes quickly and accurately so that non-interference to privileged users is guaranteed. Cooperative sensing among several cognitive radios is necessary to provide fairness by reducing the uncertain impact of other users' transmissions [2]. However, the cooperation gain is built upon individual cognitive radio's spectrum sensing ability. For individual cognitive radios, cyclostationary feature detection has advantages for spectrum sensing due to its ability to differentiate modulated signals, interference, and noise in low signal to noise ratios. It is well suited for signal detection and modulation recognition, signal parameter estimation, and the design of communication signals and systems [3].

Unfortunately, the computational complexity of cyclic spectral analysis (which far exceeds that of conventional spectral analysis) limits its use as a signal and system analysis tool. One way to attack the computation complexity is to use a parallel algorithm and implement it in specially designed parallel computers. Cell BE [4], a specially designed single-chip multiprocessor with low-cost and high parallel computing ability, provides this opportunity. It operates on a shared, coherent memory supporting one Power Processor Element (PPE) acting as the controller for the eight Synergistic Processing Elements (SPEs) processors designed especially for computation-intensive tasks. Cell BE's peak performance for single precision calculation is larger than 200 GFlops [5] and it provides a software development kit for parallel computing. In this paper, we use a PlayStation 3 with 6 usable SPEs to implement the computationally efficient algorithm FFT Accumulation Method (FAM) in order to estimate the Spectral Correlation Function (SCF)[6].

In our system, radio signal is collected through a USRP and digitized into samples which are stored in the local disk of a general processor running the GNU Radio code. The USRP is a relatively cheap hardware device with four high-speed ADCs, one FPGA, and optional RF Front Ends that can facilitate the building of a software radio with an open design, freely available schematics, drivers, and software community [7]. The Cell BE will read those samples and estimate the SCF using FAM algorithm. The cyclostationary feature results are able to detect very low SNR signals in a wide frequency range. We modified the Virginia Tech Public Safety Cognitive Radio [8] to implement our signal detector. We also designed a new spectrum sensing scheme that incorporates channel monitoring, data transmission, and dynamic spectrum switching. In this scheme, the channel search supported by a secondary receiver is periodically running to collect available spectrum and updating the most recent spectrum in a database, which will be used for possible coming dynamic spectrum switching. The test bed frequency range is in the VHF TV band and the 700 MHz Public Safety band.

2. CYCLOSTATIONARY SPECTRAL ANALYSIS

Modulated signals have built-in periodicity, characterized as cyclostationary. This information can be used for detection of a random signal with a particular modulation type in the presence of background noise and other modulated signals. Cyclostationary signals exhibit correlation between widely separated spectral components due to the spectral redundancy caused by periodicity. A signal process $x(n)$ is said to be cyclostationary in a wide sense if its mean and autocorrelation are periodic with a period T_0, i.e.,

$$M_x(t+T_0) = M_x(t) \quad (1)$$

$$R_x(t+T_0,\tau) = R_x(t,\tau) \quad (2)$$

for all t and τ. Therefore, by assuming that the Fourier series expansion of $R_x(t,\tau)$ converges to $R_x(t,\tau)$, we can write [9]:

$$R_x(t,\tau) = \sum_{n=-\infty}^{+\infty} R_x^{\frac{n}{T_0}}(\tau) e^{i2\pi\left(\frac{n}{T_0}\right)t} \quad (3)$$

where the Fourier coefficients

$$R_x^{\frac{n}{T_0}}(\tau) = \frac{1}{T_0}\int_{-T_0/2}^{T_0/2} R_x(t,\tau) e^{-i2\pi(n/T_0)t} dt \quad (4)$$

are referred to as cyclic autocorrelation functions and the frequencies $\{n/T_0\}_{n\in Z}$ are called cycle frequencies. Let α represent cycle frequency when the spectral correlation function (SCF) is defined:

$$S_x^\alpha(f) = \int_{-\infty}^{-\infty} R_x^\alpha(\tau) e^{-i2\pi f\tau} d\tau \quad (5)$$

There are generally two methods to estimate the signal SDC: frequency smoothing and time smoothing. Time smoothing algorithms are considered to be more computationally efficient for general cyclic spectral analysis. Given the signal $x(n)$, all time smoothing algorithms are based on the time smoothed cyclic cross periodogram

$$s_x^\alpha(\mathrm{n},\mathrm{f})_{\Delta t} = \frac{1}{\mathrm{T}} < \mathrm{X_T}\left(\mathrm{n},\mathrm{f}+\frac{\alpha}{2}\right)\mathrm{X_T^*}(\mathrm{n},\mathrm{f}-\frac{\alpha}{2}) >_{\Delta t} \quad (6)$$

where $\mathrm{X_T}(\mathrm{n},\mathrm{f}+\alpha/2)$, also called complex demodulators, is the spectral components of signal $x(n)$. " * " is the complex conjugate operator. The cyclic cross periodogram is calculated by using a data tapering window of length T seconds sliding over the data for a time span of Δt seconds. Mathematically, computation of the complex demodulators is expressed as

$$X_{T(n,f)} = \sum_{r=-N'/2}^{N'/2} a(r)x(n-r)e^{-i2\pi f(n-r)T_s} \quad (7)$$

where $a(r)$ is a data tapering window of length $T = N'T_s$ seconds, T_s is the sample interval, and f_s is the sampling frequency.

After the complex demodulate has been computed, it is correlated with its conjugate over a time span of Δt seconds. The correlation operation is expressed as

$$s_x^\alpha(\mathrm{n},\mathrm{f})_{\Delta t} = \sum_{\mathrm{r}=0}^{\mathrm{N}-1} \mathrm{X_T}(\mathrm{r},\mathrm{f_1})\mathrm{X_T^*}(\mathrm{r},\mathrm{f_2})\mathrm{g}(\mathrm{n}-\mathrm{r}) \quad (8)$$

where $g(n)$ is a data tapering window of width $\Delta t = NT_s$ second.

It is shown in [10] that the time smoothed cyclic cross periodogram converges to the spectral correlation function in the limit, as $\Delta t \to \infty$ followed by $\Delta f \to 0$, if the time windows a(n) and g(n) are properly normalized. Therefore, if $\sum_n a^2(n) = \sum_n g^2(n) = 1$, we have

$$\lim_{\Delta f\to 0}\lim_{\Delta t\to\infty} s_x^\alpha(\mathrm{n},\mathrm{f})_{\Delta t} = S_x^\alpha(f) \quad (9)$$

3. FFT ACCUMULATION METHOD

The signal SCF can be estimated by Equation (6) by two stages: first the complex demodulate of $x(n)$ is calculated through Equation (7), then the demodulate $X_{T(n,f)}$ is correlated over a time period of Δt seconds. The computational efficiency of this algorithm can be improved by decimating $X_{T(n,f)}$. For example, it only gets every other L (L$<N'$) sample for the second stage FFT. Therefore, Equation (8) is modified to

$$s_x^\alpha(\mathrm{nL},\mathrm{f})_{\Delta t} = \sum_{\mathrm{r}=0}^{\mathrm{N/L}-1} \mathrm{X_T}(\mathrm{rL},\mathrm{f_1})\mathrm{X_T^*}(\mathrm{rL},\mathrm{f_2})\mathrm{g}(\mathrm{n}-\mathrm{r}) \quad (10)$$

On the other hand, considering the frequency shifting for the second stage of SCF estimation, for example, from α to $\alpha+\varepsilon$, Equation (8) becomes

$$s_x^{\alpha+\varepsilon}(\mathrm{n},\mathrm{f})_{\Delta t} = \sum_{\mathrm{r}=0}^{\mathrm{N}-1} \mathrm{X_T}(\mathrm{r},\mathrm{f_1})\mathrm{X_T^*}(\mathrm{r},\mathrm{f_2})\mathrm{g}(\mathrm{n}-\mathrm{r})\mathrm{e}^{-\mathrm{i}2\pi\varepsilon\mathrm{r}\mathrm{T_s}} \quad (11)$$

FAM is a computationally efficient algorithm to combine Equation (10) & (11). It further quantizes ε into $\varepsilon = q\Delta\alpha$ [6]. Therefore, the demodulate correlation stage can be implemented in Fast Fourier Transform (FFT) too. The FAM estimation of SCF is shown in Equation (12)

$$S_x^{\alpha_i+q\Delta\alpha}(nL,f_i)_{\Delta t} = \sum_{r=0}^{P-1} X_T(rL,f_k)\, X_T^*(rL,f_l) g_c(n - r)e^{-\frac{i2\pi rq}{P}} \quad (12)$$

Essentially, the FAM algorithm can be described by Figure 1: the input signal is formed as an array with rows which are N' points long with each succeeding row's starting point offset from the previous row starting position by L samples in the original sample sequence (Input Channelization). A window is applied across each row which is then Fast Fourier transformed and down converted to the baseband. The resulting array's columns represent constant frequencies, which are point-wise multiplied with the conjugate of other columns; the final stage is another round of FFT. In the algorithm, the choice of N' must take into consideration that the time-frequency resolution product (N/N') must satisfy $N/N' \gg 1$ for a statistically reliable measurement [6] and that N' is large enough to obtain desired frequency resolution. L is usually chosen to be less than or equal to $N'/4$ [11].

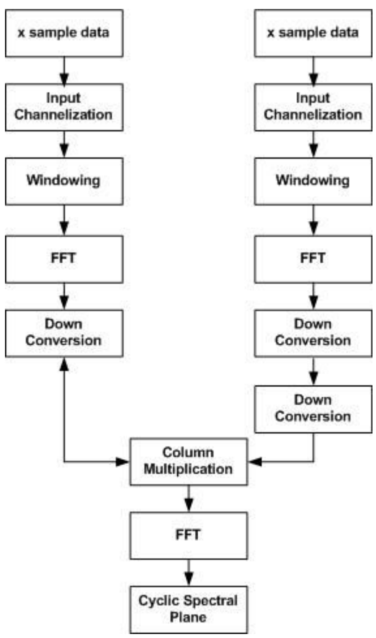

Figure 1. FAM implementation diagram, adapted from Figure 6 in [11].

In [11], FAM is implemented in C on the general processor. A Matlab version is also given by [12]. Following the above algorithm, the computation cost for a signal sequence with N samples is approximately described in Equation (13). Here, the first item represents the Windowing, Downconversion, and Column Multiplication computation cost, and the second item represents the two stages of FFTs computation cost which dominates the total value.

$$(3+2*N')*\frac{NN'}{L}+\left(\frac{NN'}{L}\right)\left(\log_2 N' + N'\log_2\left(\frac{N}{L}\right)\right) \quad (13)$$

Considering the above parameters selection and the Nyquist Sampling Theorem, the computation requirement within one second to cover a frequency range with 10 MHz bandwidth is in the order of 1 Giga Floating point Operations Per Second (GFlops) for the frequency resolution of 50Hz. The computation cost is too high for current general purpose processors (GPPs). For example, the theoretical peak of an Intel Xeon processor running at 3.06 GHz only has a theoretical maximum of 6.12 GFlops [13], while the real performance is usually much worse.

4. IMPLEMENTATION OF FAM IN CELL BE

A key issue in the use of cyclostationary signal analysis is the computational complexity associated with the calculation of a complete spectral correlation density function even when we use a computationally efficient algorithm in GPPs which is shown in Section 3. Another important factor that has to be considered is that GPPs are not optimized for scientific computation. For example, the memory size can make a huge difference for computation performance in cyclostationary analysis [14]. In addition, the memory latency problem will significantly increase the total computation time. Parallel computation can be used to attack this problem and two parallel computation structures are proposed for Digital Frequency Smoothing Method in [15].

4.1. Cell BE Introduction

The slowing pace of commodity microprocessor performance improvements, combined with ever-increasing chip power demands, has become of utmost concern to computational scientists. Cell BE, as shown in Figure 2 for its architecture, uses a conventional high performance PowerPC core, also called the Power Processing Element (PPE), that controls eight simple Single Instruction Multiple Data (SIMD) cores known as Synergistic Processing Elements (SPEs). These SPEs are specially designed for computation- intensive tasks [4].

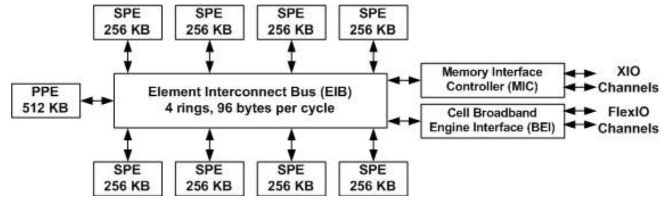

Figure 2. Overview of the Cell BE architecture, adapted from Figure 1-1 in [16].

Cell BE combines the considerable floating point resources required for demanding numerical algorithms with a power efficient software-controlled memory hierarchy. It has significant applications in scientific computing [17]. For example, Cell BE can finish a 16M sample FFT in 0.043 second on one Cell BE [18].

4.2. Parallization of FAM Algorithm in Cell BE

To fully utilize Cell BE's capacity, it is required to efficiently and effectively distribute any computational task over the usable SPEs. This should take into account the Cell BE communication mechanism and memory bandwidth, SPEs' local memory size, SIMD operation, and computational models, etc. [18].

In our signal sensing approach, the FAM algorithm is parallelized to utilize the six usable SPEs and the one PPE in a PlayStation 3. As shown in Figure 1 and Equation (13), the dominating computation cost lies in two stages of FFTs, which are also our focus for parallelization. The first stage has approximately N/L FFTs with the size of N', where the second stage has approximately $(N')^2$ FFTs with the size of N/L. As mentioned in Section 3, we have $N' \ll N$, N' being slightly larger and $L \leq N'/4$. Therefore, the FFT size in the first stage is in moderate size, while the FFT size in the second stage is slightly larger. To estimate both sizes, we use an example. To cover 4MHz bandwidth (BW) with the resolution of 40Hz, we can get a data sample rate of 10Msps to have some frequency margin, N is 2^{18}, and we can have N'=256, L=64, $N/L = 2^{12}$. Considering the SPE's Local Store size (256 KB), above two sizes of FFT can usually be accommodated by one SPE if the covered frequency BW is within dozens of MHz. Therefore, our algorithm will distribute FFTs equally among 6 usable SPEs and the PPE. To reduce the communication cost, we choose slightly larger N' so that each SPE can receive larger continuous data chunks each time, and the total number of parallel tasks is also reduced. The data independency among FFTs in either stage also enables our parallel mechanism.

As above, we discussed the parallelism granularity analysis at the task level supported by SPEs and one PPE. Another level is the data level parallelism supported by SIMD and Vector Multimedia Extension (VMX) instructions. Everything in the SPEs is done in quadword (16 byte) granularity. For single-precision floats that corresponds to 4-way SIMD operation. We use the modified stride-by-1 FFT algorithm proposed in [19] so that the FFT array can be partitioned naturally, without data rearrangement, into vectors that can be executed in parallel by SIMD instructions. The operation of reading in and out the data array and two stages of FFT results are implemented by the command Direct Memory Access (DMA), which can read 128 bytes of data each. Most important, a list of DMA transfers can be asynchronously processed while the SPE operates on previously transferred data. Other implementation details include loop unrolling, pre-computed *sin* and *cos* arrays for FFT, double-buffering, using system-specific large TLB pages, etc. [18].

5. SPECTRUM SENSING SCHEME

The feasibility of spectrum sharing lies in the spectrum sensing ability to identify spectrum holes accurately as well as the spectrum switching capability to change the transmission spectrum to other vacant spectrum quickly once the primary user appears. In [20], a spectrum sensing technique is used for opportunistic spectrum access in cognitive radio networks. However, it uses an interleaved sensing and utilization scheme for primary channel detection and transmission. During a data transmission period the primary user may appear and catch the interference. Yet, the limited idle time of a primary channel can't be fully utilized.

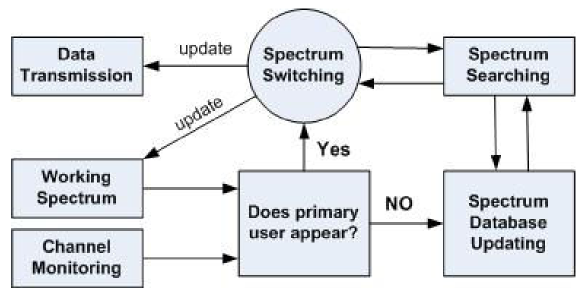

Figure 3. Spectrum sensing scheme

5.1. Spectrum Sensing Design

In this paper, we describe a spectrum sensing scheme which uses two receivers. One is for spectrum monitoring and the other is for a secondary transceiver which fully utilizes the channel idle time of a primary channel. The signal sensor will keep detecting any active signals in the specified frequency range, and will also update a signal database continuously. Once the primary user appears, the secondary receiver will pick the best QoS available channel from the spectrum database to continue previous communication. The spectrum sharing scheme is described in Figure 2.

The channel monitoring will use cyclostationary features to detect any active signals in a specified frequency range. In the present paper, the cyclostationary features are calculated by a Cell BE and transferred back to the general processor that hosts our PSCR system.

5.2. Signal Detection

In the present paper, we use the crest factor (CF) for signal detection and feature extraction by exploiting cyclic frequency domain profile (CDP) shape [21]. To evaluate any signal's existence, we used the following simple model

$$x(t) = s(t) + \phi(t) \qquad (14)$$

where $x(t)$is the continuous form of $x(n)$, $s(t)$ denotes any transmitted signal, and $\phi(t)$ denotes Additive White Gaussian Noise (AWGA). A threshold C_{TH} is defined when no signal is present, i.e., when $s(t) = \phi(t)$, for sampled signals:

$$C_{TH} = \max\left(\frac{I'(\alpha)}{\sqrt{\frac{\sum_{\alpha=0}^{N} I'^2(\alpha)}{N}}}\right) \qquad (15)$$

where $I'(\alpha) = \max_f |S_x^\alpha(f)|$ for $x(t) = \phi(t)$.

Similarly, we have

$$C_I = \max\left(\frac{I(\alpha)}{\sqrt{\frac{\sum_{\alpha=0}^{N} I^2(\alpha)}{N}}}\right) \qquad (16)$$

where $I(\alpha) = \max_f |S_x^\alpha(f)|$ for $x(t) = s(t) + \phi(t)$.

To test signal existence in AWGA, the following binary hypothesis testing is performed.

$$H_0: \quad x(t) = \phi(t)$$
$$H_1: \quad x(t) = s(t) + \phi(t)$$

Based on threshold C_{TH}, we can test the signal's existence as follows

$$C_I \le C_{TH}: \quad Declare\ H_0$$
$$C_I \ge C_{TH}: \quad Declare\ H_1$$

For any cyclic spectrum with H_1 declared, the corresponding spectrum frequency is compared to the current secondary working spectrum. If two matches are found, the spectrum switching will be triggered and the secondary user spectrum is updated; otherwise, it will be used to update in the spectrum database.

5.3. Signal Coverage BW Adjustment

In our current system, we use USRP to receive radio signals, digitize them, and store signal samples in a local disk. Then the signal samples will be sent to a Cell BE which will compute the spectral correlation density function by FAM.

The current version USRP exchanges data with the host GPP by a USB2.0 which has a limited data rate (maximum 480 Mbit/second). The data rate significantly limits the frequency bandwidth that can be covered in one RF front end frequency tuning. Considering the Nyquist Sampling Theorem and some required marginal frequency, we get signal samples with 4MHz BW for each tuned frequency. A GNU Radio program stores the data samples in the local disk for Cell BE's reading. To cover a wider frequency range, we can hop the tuned center frequency following a sequence of frequencies. For example, every other tuning frequency should be increased by 4MHz. Our separate sensing receiver enables adjustable sensing time for each tuned frequency.

6. DISCUSSION AND CONCLUSION

Essentially, a secondary spectrum sharing radio needs a system level consideration to achieve the best optimal performance. As SDR gets code as close to the antenna as possible, the computation complexity analysis and data movement in computing components is becoming significant for a system level design. In this paper, we primarily focus on two perspectives for a robust spectrum sharing system.

Current GPPs have difficulty in handling wideband signal detection by cyclostationary analysis because the computation cost is too high and a memory latency problem. We use parallel computation in Cell BE to attack this difficulty. Based on cyclostationary features' ability to accurately detect low SNR signal, we build a spectrum sensing scheme to detect a primary user signal appearing earlier. It can also guarantee a more efficient utilization of the primary signal's idle time.

However, our current system's agility is limited by two factors. For one, GNU Radio is not ported to the Cell BE, therefore, the signal samples are stored in one GPP and then read by the Cell BE, this causes a significant latency. Two, current USRP uses USB2.0 which limits the data rate, and therefore the signal bandwidth.

The GNU Radio community is working on porting GNU Radio into PlayStation 3. Once it is finished, the present spectrum sensing/sharing system will also be ported to the PlayStation 3. Therefore, the data storing/reading latency can be omitted. In addition, USRP 2 is under its way to the market. USRP 2 will use a Gigabit Ethernet interface which allows for 25 MHz bandwidth RF BW each way. It can cover a much larger frequency range in one center frequency hop, and dozens of MHz BW in a few hops. Further, the cyclostationary feature detector could be implemented as a signal processing block. This way, the signal sample data will not go to the disk, so that some storing/reading disk time is saved. As a result, the agility will be much better.

Furthermore, the system can be implemented in other software and hardware system such as the Software Communication Architecture (SCA) or the Space Telecommunications Radio System (STRS) for SDR framework; FPGA, DSP chip, or ASIC for computation component; Lyrtech Small Form Factor (SFF) SDR Development Platform for RF front end and signal processing. In addition, if we put the system mostly in a single chip, the data communication speed from the ADC to the following digital and computation chain can be significantly improved, therefore we can achieve much better agility.

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