ALL DIGITAL FPGA BASED FM RADIO RECEIVER

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ABSTRACT

This paper presents the design and implementation of the field-programmable gate array (FPGA) based all-digital frequency modulation (FM) radio receiver with a general-purpose RF front-end. The objective of this paper is to build a FPGA based, fully digitized FM radio receiver including a digital tuning function. This receiver consists of a simple analog RF front-end, an Analog-to-Digital converter (ADC), a FPGA chip and a Digital-to-Analog Converter (DAC). The Virginia Tech software defined UWB board is used as the hardware platform of the radio receiver in this project. This board is built by Dr. Chris Anderson, and equips with an 8-bit 1GSPS ADC and a Virtex2pro70 FPGA. A DAC evaluation board and a radio scanner are used to output the audio. A personal computer (PC) plays the role of the controller to tune the receiving frequency through the *RS-232* port.

1. INTRODUCTION

The goal of software defined radios (SDR) is to be able to switch between waveforms simply by executing a software change. Achieving this goal requires a highly flexible RF front-end, capable of reconfiguring and adapting to different wireless standards, a performance requirement that can be prohibitively expensive. An alternative is to design the RF front-end to be as general as possible, where the ideal RF front-end consists of only an antenna and low noise amplifier [2]. All the signal processing will therefore be performed in the digital domain. In the past, such an implementation has been impossible because both the analog-to-digital converter (ADC) and the processor had an insufficient level of performance or required an exorbitant cost. With the increase in silicon device performance over the past few years, under certain conditions, the ideal RF front-end is viable today.

This paper describes how a radio system can be software defined. FM radio receiver is a good example for this purpose. In this work, filtering, mixing and demodulating, the major tasks of the receiver are perfectly done digitally in FPGA and can be reconfigured in real-time by PC. However, a new problem that does not exist in analog FM receiver appeared in the development of this project. The multipliers of the FPGA can not run at *240MHz* to handle some signal processing operations such as filtering. Hence a parallel signal processing design is applied to make slower multipliers can handle the faster input data rate.

In the following sections, the section 2 explains the design of the FM radio receiver. Several design problems and solutions will be discussed. The viability and detail implementation of the designs are described in section 3. Finally, the section 4 draws a conclusion of this work.

2. FM RADIO RECEIVER DESIGN

Frequency modulation is a form of modulation which represents information as variations in the instantaneous frequency of a carrier wave. FM is commonly used at VHF radio frequencies for high-fidelity broadcasts of music and speech. Normal (analog) TV sound is also broadcast using FM. Figure 1 shows the block diagram of the all digital FM radio receiver. The detail designs, problems and solutions are discussed in the following sub-sections.

2.1. RF Front-End

As shown in Figure 1, the RF front-end consists of three components: an antenna, a low noise amplifier and a low-pass filter. The function of this RF front-end is to amplify the RF signal and reject upper image signals. Other functions those were achieved in the RF front-end are moved into the FPGA now. Hence, this RF front-end can be applied to other communication systems with an adjustable low pass filter.

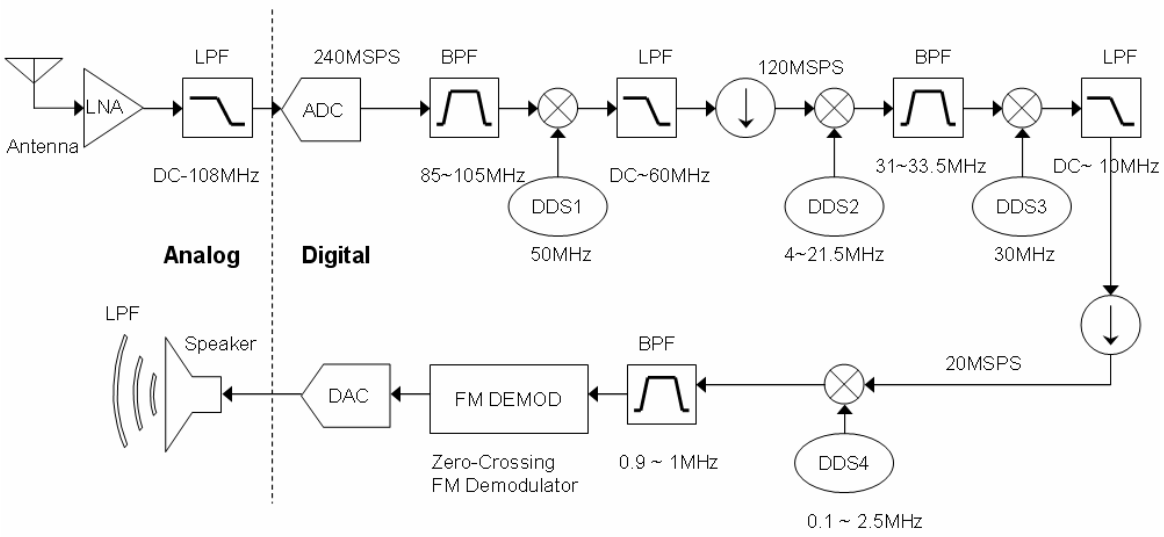

Figure 1 Block Diagram of the All Digital FM Radio Receiver

2.2. Parallel Multiplications

To achieve *240MHz* multiplication by multipliers running at *120MHz*, a parallel-multiplier structure shown in Figure 2 is deployed. In Figure 2, the sampling rate of the input data is *240MHz*. After the de-multiplexer, the odd numbers of the samples are fed to one multiplier; and the even numbers of the samples are fed to the other one. Therefore, each of the multiplier needs to process *120MSPS* input data, which meets the speed constrains of the multipliers. After the multiplications, the output data are re-formed in the original order by a multiplexer. By this structure, higher-rate data mixing and filtering can be achieved with lower speed multipliers.

2.3. Serial Multiplications

In a FPGA, the dedicated multipliers are very limited. For a filter running at *20MHz* sampling frequency, it costs over *100* multipliers to achieve a *200KHz* bandwidth with a *30dB* depression in stop band. However, each multiplier only needs *20MHz* speed to get the job done. Hence the multiplier reusing structure shown in Figure 3 can reduce the requirement of the multiplier number by six times. This structure does a reverse way comparing with the parallel multiplications structure. A multiplexer combines n-way parallel input signals to a serial signal. After the multiplication, the serial signal is separated to n-way signals by a de-multiplexer. This structure can work properly as long as the total input data rate of the n-way signals is slower than the speed of the multiplier.

2.4. FM Demodulation

In general, the FM signals may be demodulated in various ways. In digital domain, an efficient way to demodulate a FM signal is Zero-Crossing demodulation (ZCD) technique. ZCD is applicable to many worldwide mobile and personal communications systems. In addition, ZCD offers lower power consumption, simpler implementation and better bit-

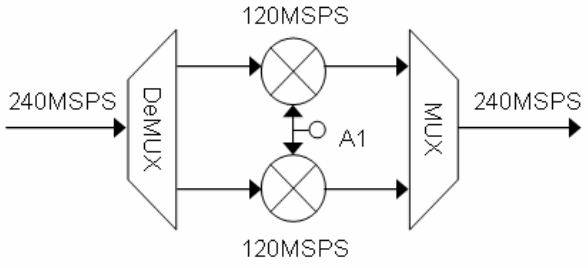

Figure 2 Parallel Multiplications Structure

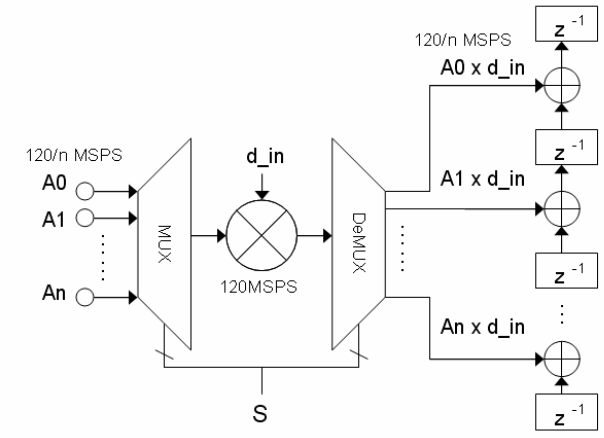

Figure 3 Serial Multiplications Structure

error rate (BER), compared to the conventional analog implementation such as limiter-discriminator integrator (LDI) and the conventional digital implementation such as the cross-differentiate-multiply demodulator (CDM)[2]-[5]. Another advantage of this method is high linearity. In the demodulator, a counter counts the number of zero-crossing points within a unit time. This number is compared with a reference number that represents zero-amplitude signal. The difference of two numbers is the amplitude of the signal within this unit time. By this way, the base-band signal can be recovered.

2.5. Tuning Control

To control the receiving frequency band, a control signal decoder is designed to map the input frequency selective data to the control data of the Direct Digital Synthesis (DDS) modules. The desire frequency band can be correctly shifted to pass all the filters and fed to the FM demodulator by controlling the output frequency of the DDS. The control signals input from a PC via *RS-232* port.

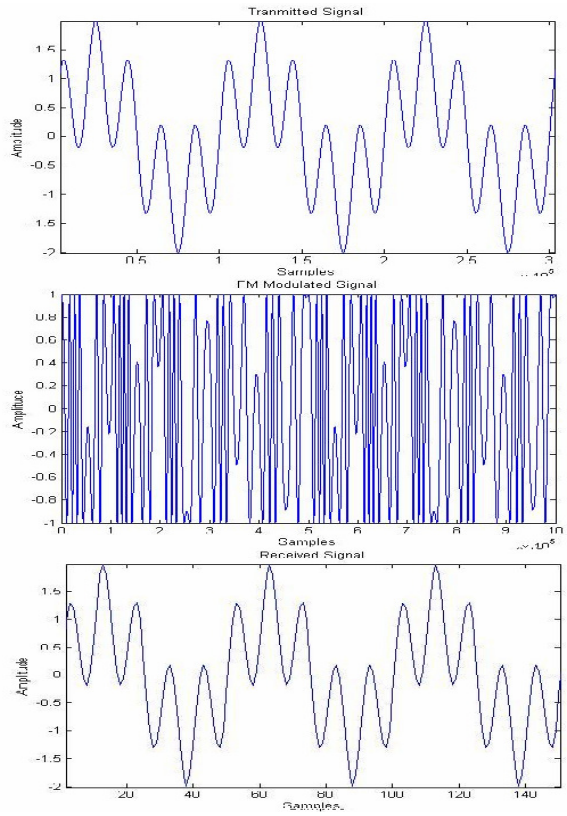

Figure 4 Simulation Results of FM Demodulation

3. SIMULATION AND IMPLEMENTATION

In this section, the simulation results of the zero-crossing demodulation and the detail implementation of the receiver designs are presented.

3.1 The Simulation result of FM Demodulation

A simulation of the FM demodulation is done in Matlab to verify the functionality and performance of the design of the FM demodulation. It can be observed in Figure 4 that this demodulation method recovered the FM signals successfully.

3.2 RF Front-End implementation

Table 1 shows the components used to build the RF front-end. For simplicity, commercially available off-the-shelf components have been chosen for the components of this Front end.

3.3 Audio Output Chain

Since an audio DAC is not available in lab, a *14-bit* TI *DAC5672* DAC is used to substitute the audio DAC. However, the minimum output frequency of this DAC is *10MHz*. To overcome the limitation, the demodulated base-band audio signal is up-converted to *40MHz* by amplitude modulation (AM) method, and output through this DAC. A radio scanner receives this AM signal and plays it back. Figure 5 shows the block diagram of the output chain; and Figure 6 shows the pictures of the DAC evaluation board and radio scanner set.

4. CONCLUSIONS

SDR is currently being applied to many communication systems since it provides a number of benefits over traditional single-function radios, however, the inflexibility of the RF front-end is a major limiting factor in the further development of SDR technologies. There are two approaches to achieve a higher level flexibility,. The first approach is to use better analog components with immense

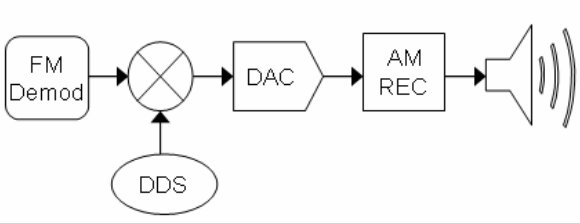

Figure 5 Audio Output Chain of the FM Receiver

Figure 6 Hardware of the DAC and Radio Scanner

flexibility and high performance for all variety of signals. The other way is to simplify the front-end and move signal processing function into the digital domain. Nowadays, a lot of attention and interest has been focused on the second approach since it leads to lower cost and more stable performance. As a result of the powerful parallel data processing ability of FPGAs, it is possible for a SDR system to process the received signal directly from RF stage using a parallel algorithm. The result is a more general-purpose RF front end, allowing SDR systems to operate with a wider variety of waveforms.

5. Reference

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Table 1 RF Front-End Components of FM Receiver

ITEM	PART #	BANDWIDTH	QTY.
ATTENNA	N/A	FM BAND	1
AMPLIFIER	ZFL-500LN	0.1 – 500MHZ	3
LPF	SLP-100	DC – 108MHZ	1