AN EFFICIENT UE MODEM PLATFORM ARCHITECTURE FOR 3GPP LTE

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I. Abstract

Recently, a high-data-rate, low-latency and packet-optimized radio-access technology has been intensively studied in 3GPP Long-Term Evolution (LTE) standard group. The 3GPP LTE system should support instantaneous downlink and uplink peak data rates of 100Mb/s and 50Mb/s within 20 MHz downlink and uplink spectrum allocations, respectively. In this paper, we propose an efficient UE modem platform architecture which considers the trends and necessary conditions in the 3GPP LTE specifications. Based on the proposed structure, a hardware platform is implemented. The experimental results demonstrate that the developed platform is able to be used as 3GPP LTE UE modem.

II. Introduction

The 3GPP radio-access technology will be highly competitive for several years. However, to ensure competitiveness in an even longer time frame, i.e., for the next 10 years and beyond, a long-term evolution of the 3GPP radio-access technology needs to be considered.

Important parts of such a long-term evolution include reduced latency, higher user data rates, improved system capacity/coverage, and reduced cost for the operator. In order to achieve these performances, an evolution of the radio interface as well as the radio network architecture should be considered.

Considering a desire for higher data rates and taking into account future additional 3G spectrum allocations, the long-term 3GPP evolution should provide a support for wider transmission bandwidth than 5 MHz. At the same time, support for transmission bandwidths of 5 MHz and less than 5 MHz should be investigated in order to allow for more flexibility in whichever frequency bands the system may be deployed [1].

Considering the trends and necessary conditions in these 3GPP LTE specifications, This paper presents an efficient UE modem platform architecture for 3GPP LTE systems and verifies the functionalities of the implemented platform. The following steps were followed:

- definition of the requirements of LTE;
- development of the UE modem architecture;
- implementation of the UE modem apparatus;
- analysis of experimental results;
- description of conclusion and future work.

III. Requirements of LTE

The objective of Evolved UTRA and UTRAN is to develop a framework for the evolution of the 3GPP radio-access technology towards a high-data-rate, low-latency and packet-optimized radio-access technology.

The peak data rates may depend on the numbers of transmit and receive antennas at the UE. The targets for downlink (DL) and uplink (UL) peak data rates are specified in terms of a reference UE configuration comprising:

- downlink capability – 2 receive antennas at UE;
- uplink capability – 1 transmit antenna at UE.

For this baseline configuration, the system should support an instantaneous downlink peak data rate of 100Mb/s within a 20 MHz downlink spectrum allocation (5 bps/Hz) and an instantaneous uplink peak data rate of 50Mb/s (2.5 bps/Hz) within a 20 MHz uplink spectrum allocation. The peak data rates should then scale linearly with the size of the spectrum allocation.

E-UTRA shall be operated in spectrum allocations of different sizes, including 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz, 15 MHz and 20 MH,. in both the uplink and downlink. Operation in paired and unpaired spectrum shall be supported [2].

IV. Proposed UE Modem Platform Architecture

A. Platform Architecture Design

The proposed modem platform architecture is focused on the evalution of conditions required to 3GPP LTE.

Additional advantages of the proposed architecture over the previous ones include: (i) a high-performance interface between terminal and L2 using CardBus [3] interface; (ii) a high-performance interface between L2 and L1 using FPGA [4] and EMIFA-bus of DSP [5]; and (iii) a high-performance interface between L1 and DIF using Serializer and Deserializer (SER/DES) [6].

Considering Fig. 1, the proposed modem platform architecture consists of the following:

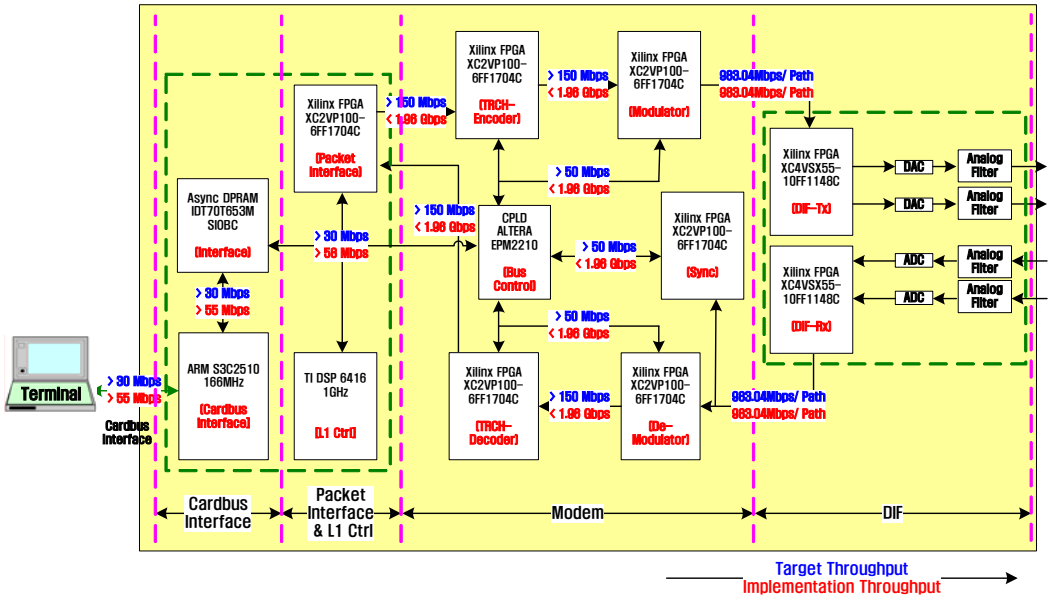

Fig. 1. Architectural template of the UE modem.

- control block for CardBus interface[7], L2 interface (packet interface) and the function of L1 control;
- modem block for the function of LTE UE modem;
- DIF block for 2 receive path and 2 transmit path.

In the control block, L2 interface consists of traffic path and control path. The traffic path is used for data link control functionalities using packet interface with FPGA [8]. The control path is used for control link control functionalities using EMIFA-bus of DSP.

In modem block, modem block consists of TRCH (transport channel)-encoder module, TRCH-decoder module, modulatior module, demodulator module, and synchronization module. When the implementation of LTE UE modem is finished, the number of used FPGAs can be decreased. However, not to limit the number of used FPGAs in the development of LTE UE modem, FPGAs is used respectively. Interface of DSP and FPGAs is shown in Fig. 2, whree control signals deal with interrupt handling by means of DSP, CPLD and FPGAs [9].

In the DIF block, 3GPP LTE describes that the peak data rates may depend on the numbers of transmit and receive antennas at the UE: 2 receive antennas (DL) and 1 transmit antenna (UL). Considering the use of the DIF block for Base Station (BS), a superheterodyne-based RF architercure with 2 receive path and 2 transmit path is presented, instead of a zero-IF-base RF architecture.

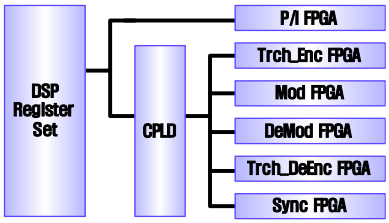

Fig. 2. Interface of DSP and FPGAs for control link.

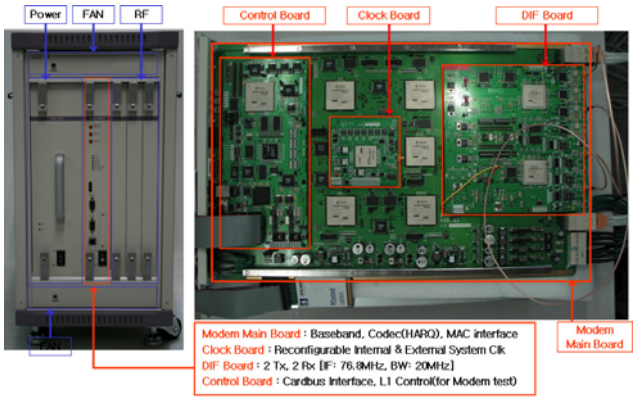

Fig. 3. developed UE modem platform.

B. *Platform Implementation*

We have developed the modem platform based on the proposed architecture. As shown in Fig. 3, the modem main board gears with control daughter board, clock daughter board, and DIF daughter board.

In the control daughter board, ARM S3C2510 (166 MHz) is used for CardBus interface to use the CardBus driver on chip. TI DSP6416 (1GHz) is used for L2/L1 control link interface and L1 control function which is processed per 0.5ms. and Xilinx FPGA XC2VP100-6FF1704C with 99,216 logic cells is used for L2/L1 data link interface.

In the clock daughter board, we use a Xilinx FPGA XC2VP20-7FF896C with 20,880 logic cells, and built-in digital clock management (eight DCMs) to generate a flexible system clock and a various system tick. In addition, several IDT74FCT3807/A clock drivers are used for supplying a pure system clock for modem main board and each daughter board.

In the modem main board, each logic module hosts a Xilinx FPGA XC2VP100-6FF1704C with 99,216 logic cells, and built-in digital clock management (twelve DCMs). Some

TABLE I
BASIC TRANSMISSION PARAMETERS

Parameter	Test program	
Tx BW	5 MHz*	20 MHz**
Sub-carrier spacing	15 kHz	15 kHz
Sampling frequency	7.68 MHz	30.72 MHz
FFT size	512	2048
Number of occupied sub-carriers***	305	1220

* Basic transmission parameters of single band scheme(BW: 5 MHz) for multi-band scheme.
** Basic transmission parameters of four-band scheme.
*** Includes DC sub-carrier which contains no data.

clock drivers on clock daughter board provide synchronized system clocks for DCM blocks of these FPGA. Trch-encoder module and TRCH-decoder module use DPRAM (IDT70T3539MS166BC) to process Hybrid Automatic Repeat request (HARQ) respectively.

In the DIF daughter board, we use several DS90CR483/484 to guarantee a steady interface of L1 and DIF. Even if zero-IF-base RF is developed, this interface will be used as it is. Two Xilinx FPGA XC4VSX55-10FF1148C chips with 512 XtremeDSPTM slices are used for high-performance signal processing.

V. EXPERIMENTAL RESULTS

A. Test Program for Performance Verification

The performance analysis of the developed platform is divided in two parts: (i) the interface performance between terminal and control boards, and (ii) DIF performance. The interface performance between terminal and control boards is measured by a general method. To verify the DIF performance of the developed platform, we have programmed GUI test program which is divided into two parts: Tx baseband signals generation and Rx baseband signals analysis. The timing OFDM [10] parameters of GUI test program are given in Table 1.

In the Tx baseband signals generation, if a transmission scheme uses a single-band within a 5 MHz spectrum allocation, the basic transmission parameters for a single-band are used as it is. Also if a transmission scheme uses a four-band within a 20 MHz spectrum allocation, to generate Tx baseband signals, the following steps are followed:

(i) Tx baseband signals generation for single-band transmission scheme. In this case, the sampling frequency is 7.68 MHz;

(ii) over-sampling step (i) four times the rate. In this case, the sampling frequency is 30.72 MHz (4 x 7.68 MHz);

(iii) shifting the center frequency of step (ii) to N MHz (N= -7.5, -2.5, 2.5 and 7.5);

(iv) synthesizing the shifted Tx bansband signals. In this case, the sampling frequency is 30.72 MHz (4 x 7.68 MHz) and transmission bandwidth is 20 MHz.

In the Rx baseband signals analysis, for four-band transmission scheme, to analyzer a received baseband signals, the following steps are followed:

(i) selecting a wanted single band;

(ii) shifting the center frequency of step (i) to zero MHz;

(iii) filtering an unnecessary bands. In this case, the sampling frequency is 30.72 MHz (4 x 7.68 MHz) and selected bandwidth is 5 MHz;

(iv) down-sampling step (iii) four times the rate. In this case, the sampling frequency is 7.68 MHz and selected bandwidth is 5 MHz;

(v) performance analysis of step (iv) by Error Vector Magnitude (EVM).

EVM is simply defined by eqn.1 and eqn.2

$$EVM\,[\%] = \sqrt{\frac{\sum_{n=1}^{N} \frac{1}{N}(\Delta I_n^2 + \Delta Q_n^2)}{I_{\max}^2 + Q_{\max}^2}} \times 100 \qquad (1)$$

$$EVM[dB] = 20 \times \log(\frac{EVM[\%]}{100[\%]}) \qquad (2)$$

B. Performance Analysis

This paper describes three experimental results: (i) the performance of the interface of terminal and control board, (ii) the path test of each FPGA on modem main board, and (iii) the DIF performance of the developed experiment. The interface performance between terminal and control boards is as shown in Fig. 1. This performance includes a processing time for performance analysis application at terminal and depends on CPU throughput of terminal and the number of multi-tasking besides.

To test the path exam of each FPGA for modem main board, packet interface FPGA on control daughter board generates count signals and transmits to TRCH-encoder FPGA. These count signals circulate through modulator FPGA, demodulator FPGA and TRCH-decoder FPGA. Finally, packet interface FPGA receives it from TRCH-decoder FPGA. Then, as shown in Fig. 4, we could guarantee the stability of the digital paths for each board.

Fig. 5 shows the frequency spectrum of DIF Tx which is four band OFDM signals. The transmission bandwidth of Each band is 5 MHz. accordingly, the total BW is 20 MHz.

To verify the performances of DIF Rx, we have consider three cases which could be seen in Table 2: the analysis of simulation, the result using the commercial equipment, the measurement of the throughput of a developed experiment. In each case, Tx baseband signals by GUI test program is used.

In the analysis of simulation, we have remodeled a Tx baseband signals into Rx baseband signals by offsetting the frequency 1000 Hz, phase 123 degree and gain 1/4. Next, we have analyzed the performance of it using the GUI test program.

TABLE II
DIF RX RESULTS

EVM[dB], (input power: -25dBm)

Modulation	Simulation	Equipment	Experiment
QPSK	-49.4265	-41.7421	-42.8614
16QAM	-42.2448	-39.8651	-39.6964
64QAM	-38.1771	-36.7349	-36.4005

In the result using the commercial equipment, Tx baseband signals is transmitted as Tx IF analog signals (center frequency: 76.8 MHz) by Agilent E4438C ESG and it is received and converted Rx IF analog signals into Rx baseband signals by Agilent E4440A PSA series. Next, we have analyzed it alike.

In the measurement of the throughput of a developed experiment, modulator FPGA transmits a Tx baseband signals to DIF-Tx FPGA which converts it into TX IF analog signals (center frequency: 76.8 MHz). then, by means of loop-back composition, DIF-Rx FPGA receives it and converts Rx IF analog signals into Rx baseband signals. Next, we have analyzed it as well.

Finally, we could confide that the throughput of a developed experiment is equal to the result using the commercial equipment.

Fig. 6 shows the constellations 64QAM modulation schemes for the developed experiment. Tx constellations are the data of Tx baseband signals and Rx constellations are the data of demodulated Rx baseband signals at the developed experiment.

VI. CONCLUSIONS

In this paper, we have proposed an efficient UE modem platform architecture which considers the trends and necessary conditions in the 3GPP LTE specifications. Based on the proposed structure, a hardware platform has been implemented. Experimental results have demonstrated that the developed platform are able to be used as 3GPP LTE UE modem.

Finally, we wish to note that the LTE UE modem is able to be implemented using the developed platform.

Our next goal is to research and develop the processor block and the zero-IF-base RF. The processor block executes L2, L3, and applications as well as the CardBus interface and L1 control. If the design of the processor block considers chips such as Intel PXA270 [11], Tensilica Diamond [12], and CEVA-X1620 [13], the performance of the processor block can be improved. The further study is to implement the LTE UE system as soon as possible.

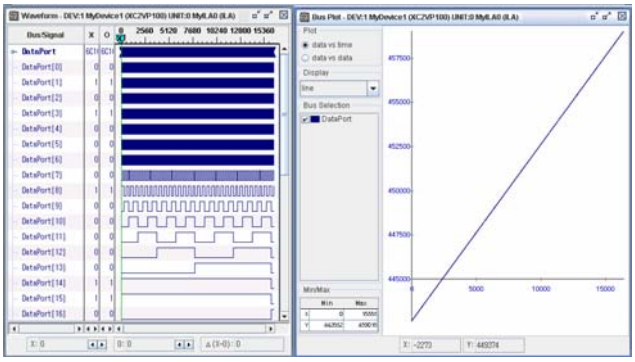

Fig. 4. Real-time verification for traffic path using ChipScope by Xilinx, Inc.

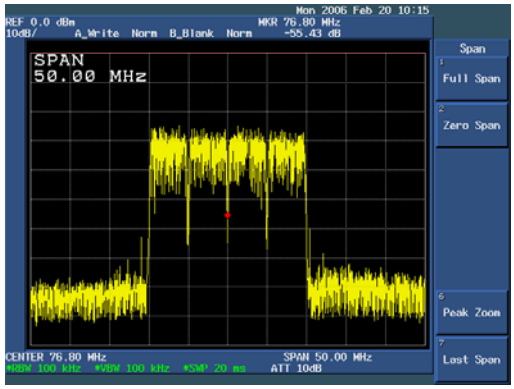

Fig. 5. Frequency spectrum of OFDM signals (IF : 76.8MHz, BW: 5 MHz * 4, sampling frequency: 30.72MHz).

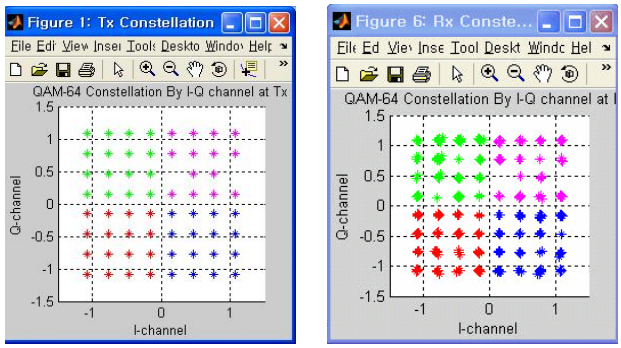

Fig. 6. Constellation of Tx 64QAM and Rx 64QAM.

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