MEDIUM TERM EVOLUTION FOR RECONFIGURABLE RF TRANSCEIVERS

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ABSTRACT

This paper presents approaches to reconfigurable RF transceivers that are pursued in the EU IST project e2R. This work can be divided into two parts. On the one hand, specific work on the architecture and building blocks for highly reconfigurable RF transceivers. On the other hand, the concrete design and implementation of a prototype RF transceiver. Concerning the first part, the work is focused on an advancement of the well-known direct conversion receiver and transmitter. In the proposed solution, digital signal processing functions are incorporated directly into the RF ICs to increase its flexibility. A key enabler for this architecture change is the step towards CMOS technologies for RF ICs. Concerning the prototyping activity, the key features of the targeted prototype are presented.

I. INTRODUCTION

TODAY, a multitude of radio access technologies (RATs) for wireless communications coexist and compete with each other. While GSM is well-established and offers the best coverage world-wide, new standards like W-CDMA, TDCDMA, or CDMA2K 3xRTT offer higher data rates paving the way for applications such as mobile office, usic/video download, video telephony, mobile TV, cheap voice calls, etc. Other RATs from the wireless local area network (LAN) / metropolitan area network (MAN) family (IEEE 802.11a/b/g/n, WiMAX) are low-cost but onetheless have the potential to rival the cellular standards. In such a heterogeneous radio environment, a user terminal that supports a multitude of RATs at the same time, i.e. concurrently, is desirable. Thus ideally, the RF transceiver for a multi-standard terminal would be composed of a number of receive paths and a number of transmit paths as depicted in Fig. 1, where the following two properties would apply.

1. *Unlimited reconfigurability of each path to any RAT*
2. *Independency of each path from all others*

By making a transceiver reconfigurable – a concept known as software defined radio (SDR), on the one hand the bill of materials (BOM) can be lowered by component-reuse, and on the other hand the design effort can be reduced if an additional standard has to be accommodated. Moreover, SDR would allow flexible spectrum allocation (FSA). These benefits vanish when a dedicated transceiver is provided for each RAT. Although the latter approach is found in today's commercial multi-standard transceivers (e.g. in [2]), it is neither anticipated to be a very cost-efficient nor a scalable solution if more than three RATs have to be supported.

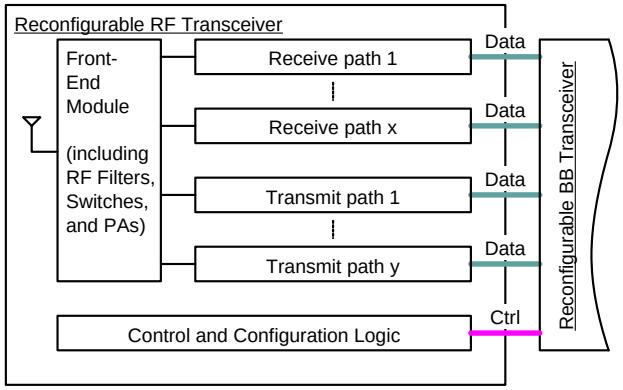

Fig. 1. RF transceiver with x *concurrent* receive and y *concurrent* transmit paths.

In this paper, an overview of key findings for highly reconfigurable RF transceivers is given within the context of end-to-end reconfigurability as considered by the E2R project [1]. This paper however, keeps the focus on multi-standard terminals. Since base station RF transceivers receive and transmit an entire band or sub-band as a whole, channelization is fully done by software and the requirements on the RF and analog hardware are somewhat different. Section II of this paper reviews the provoking vision of an ideal SDR and discusses its feasibility. Section III provides an overview of key RF requirements imposed by current RATs. Based on the findings of section II and III, an advancement of the well-known, purely analog, direct conversion receiver and transmitter is proposed in section IV as a compromise between max. reconfigurability – as evidenced by the ideal SDR – and technical feasibility. Section V subsequently highlights critical receiver building blocks,

namely the front-end module, the LNA, and the ADC. Concerning the prototyping activity, the key features of the targeted prototype are presented in section VI and finally, section VI draws conclusions.

II. THE IDEAL SOFTWARE RADIO AND ITS FEASIBILITY

Making a transceiver reconfigurable is generally limited by the radio-frequency (RF) and analog blocks as they do not lend themselves as easily to reconfiguration as the digital blocks: Tuning of analog blocks is typically limited to a few 10%; and if analog blocks are switched in and out, the area overhead can be large and the parasitic capacitance added to the node may be intolerable.

An ideal SDR was proposed by J. Mitola in the early 90's [3]. In its essence, the ideal SDR is depicted in Fig. 2. The receiver of Fig. 2(a) achieves some gain by a low-noise amplifier (LNA), followed by an anti-aliasing filter and subsequently by the analog-to-digital converter (ADC) – still at RF. The received signal is then further processed in the digital domain by a receiver digital front-end (RX DFE). The architecture of the RF transmitter of Fig. 2(b) by analogy to Fig. 2(a) consists of a TX DFE, a digital-to-analog converter (DAC), a power amplifier (PA), and a reconstruction filter.

The basic idea of the architecture of Fig. 2 is to shift as much signal processing as possible from the analog domain to the digital domain as digital blocks can be made reconfigurable more easily. Unfortunately, the architecture of Fig. 2 is not realizable for current RATs (cell phones, WLAN terminals, etc.) since the required performance on block-level is just way too demanding. On the receive side, sampling at RF leads to excessive power consumption – if possible at all. Moreover, the dynamic range required for the ADC of Fig.2(a) given current RAT bandwidths is excessive and not realizable today by its own. On the transmit side, the necessary clock rate of the DAC again results in unrealistic requirements for a carrier frequency in the GHz range. Moreover, it is unknown how to realize a broadband match between the PA and the reconstruction filter; and how the latter could be made frequency tunable. Therefore, the first property desired in section I for the transceiver of Fig. 1cannot be achieved realistically. The requirements in terms of selectivity, sensitivity, and power consumption mandate the introduction of combined filter-gain stages, both at RF and baseband. Even with added filtering in the receive and transmit paths, transmitted signals can (a) appear as excessively large blocking signals violating the blocking mask of other receivers, and (b) corrupt received signals when mixed by a non-linear block – if multiple transceivers are operated concurrently as in Fig. 1. Therefore, the second property desired in section I cannot be achieved either. To avoid these problems, the transceiver of Fig. 1 can be limited to a single transmit path and e.g. two receive paths.

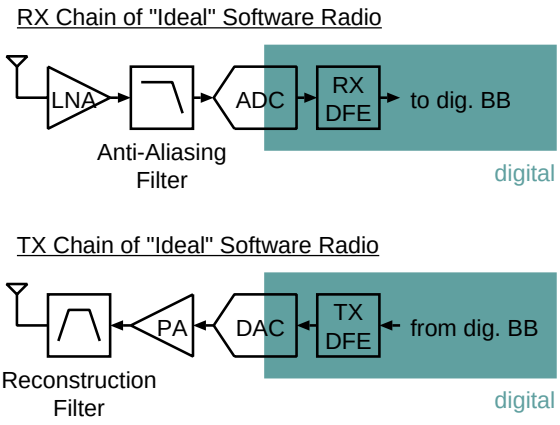

Fig. 2. *Ideal* SDR receive (a) and transmit (b) paths.

III. RF REQUIREMENTS OF WIRELESS SYSTEMS

Requirements relevant to RF reception have been collected for 18 radio access technologies (RAT) [4]. The minimum/maximum requirements for the downlink frequency bands, signal bandwidths, reference sensitivities and the maximum input signal levels for the most pertinent standards have been investigated. From these figures, we may conclude that an SDR RF transceiver should

- cover a frequency range from *below 100 MHz to 6 GHz* (if not 10 GHz)
- be able to handle bandwidths *from 200 kHz to 20 MHz*,
- deliver a controlled output power range from -50 dBm up to 40 dBm (*90 dB output power dynamic range*!),
- have an input power range from -1 dBm down to -135 dBm (*134 dB input power dynamic range*!), and
- be able to handle a multitude of modulation schemes, which may have very different peak-to-average ratios.

Clearly, no single RF transceiver can meet these requirements to date. Therefore, only a subset of the investigated RATs can be supported by a single RF transceiver. For the 18 investigated RATs, the frequency range can be confined to 174 MHz – 2690 MHz by (i) limiting the broadcast services to the VHF band III, (ii) using only wireless MAN frequencies below 3 GHz, and (iii) refraining from the 5 GHz wireless LAN standards, which relaxes the requirements on frequency tuning significantly.

IV. PROPOSED E2R RF TRANSCEIVER ARCHITECTURE

A. Enhanced Direct Conversion Receiver and Transmitter

Fig. 3 and 4 show an advancement of the well-known, purely analog, direct conversion RF receiver and transmitter. The proposed receiver and transmitter architectures are a compromise between maximum reconfigurability – as evidenced by the ideal SDR – and technical feasibility taking into account RAT requirements. The receiver and transmitter comprise an analog front-end (AFE) from the antenna down to the converter ADC/DAC), which is flexible enough to meet the requirements of multi-standard operation, and a digital front-end (DFE). By introducing a DFE, the hitherto analog data interface to the digital BB IC is replaced by a digital one. The step towards a digital interface requires signal decimation and filtering in the DFE to reduce the excessive data rates at the ADC outputs.

B. Introduction of a Digital Front-End

Since analog blocks are not well suited for reconfiguration, some analog signal processing tasks like channel selection should be shifted to the digital domain to obtain more flexibility. As a consequence, the requirements on the ADC are increased. The DFE closes the gap between traditional baseband processing and the high data rates at the output of the ADC. Cellular receivers mainly employ ÓÄ ADCs with sample rates in the range of one hundred MHz or more. Thus, the resulting data rates at the ADC output are in the range of several hundred Mbps. The DFE reduces the sample rate to two or four times the symbol rate of the RAT under consideration. The integration of the ADC onto the RF IC is a key enabler for a fully digital baseband IC that does not require an analog macro. Thus, the digital baseband IC can easily be shrunk to up-coming CMOS technology nodes.

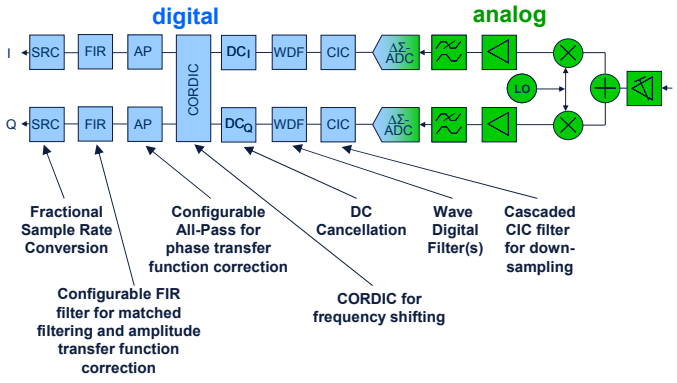

Fig. 3. Proposed E^{2}R RF IC *receiver* architecture.

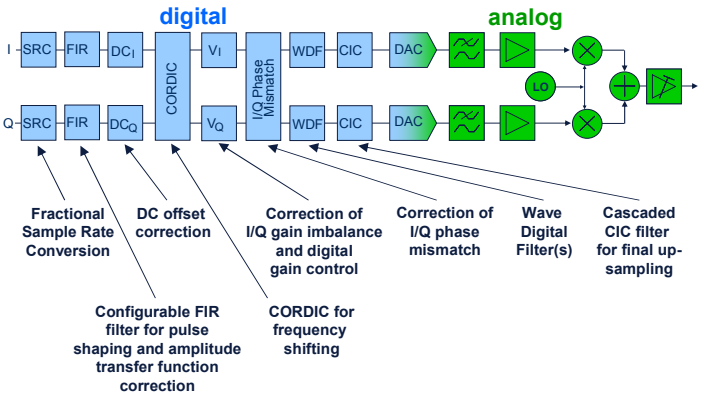

Fig. 4. Proposed E^{2}R RF IC *transmitter* architecture.

V. CRITICAL RF RECEIVER BUILDING BLOCKS

A. Front-End Modules (FEMs)

The dynamic range requirements for RF receivers make RF band pass filters indispensable. A quick overview of tunable RF band pass filters is given in [5]. However, none of the investigated approaches being suitable for low-power environments (≤ 5 V) is capable of delivering a tuning range of about 30%, which is necessary to cover at least the cellular frequency bands from 750-950 MHz and the ones from 1.7-2.2 GHz. Although micro-electronic-mechanical system (MEMS) filters are able to achieve a tuning range of about 30%, they require switching voltages in the range of several tens of volts making them unsuitable for battery-driven devices. Due to the lack of tunable RF filters, a filter bank of untunable RF filters as depicted in Fig. 5(a) is suggested here as a pragmatic medium term solution. Supporting another RAT means adding another set of filters and power amplifiers (PAs) driving up costs considerably. Moreover, commercial components for multi-mode radios (like switchplexers) are hard to find to date. Given the mentioned limitations, both the number of receive and transmit paths and the number of supported RATs per receive/transmit path is likely to be limited by the cost and area consumption of the front-end module.

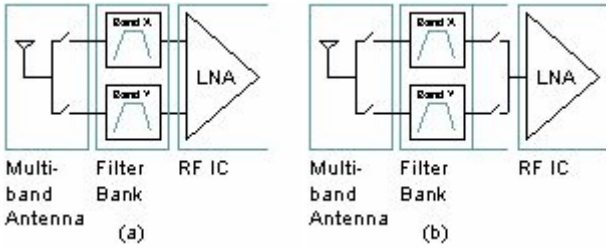

Fig. 5. A possible realization of a multi-standard (GSM900, WCDMA, and 2.4 GHz WLAN) and possible interfaces to the RF IC (a), (b).

Therefore, tunable RF filters and PAs are really key building blocks for SDR. However, as they are far away

from being commercialized at the moment, a substantial research effort is necessary if the front-end module should not become the show-stopper of SDR.

Complementing the multi-band antenna by another one allows taking advantage of rich scattering environments to enable multiple-input multiple-output (MIMO) transmission on the downlink if two receive paths and corresponding support from the base station is available. For the case of two antennas, the following configurations are possible:

1. MIMO: Antenna 1 – RX1/TX1, Antenna 2 – RX2
2. Max. TX/RX iso.: Ant.1 – RX1/RX2, Ant.2 – TX1

The additional isolation from the transmit to the receive paths can be maximized if e.g. orthogonal polarizations of the antennas are chosen.

B. Low Noise Amplifiers (LNAs)

The architecture proposed in Fig. 3 makes use of a direct conversion receiver (DCR) for frequency translation. As opposed to e.g. the heterodyne receiver, a DCR evidences a high integration level (less off-chip components) and better flexibility. However, the demands on the individual building blocks, i.e. the LNA and the down-conversion mixer, are increased. In contrast to the down-conversion mixer, which is inherently broadband, the LNA usually must be made narrowband [6] to attain the required performance (input match, gain, noise figure, linearity, stability, power consumption). Therefore, making LNAs capable of multistandard operation is a challenge. Four fundamental approaches are conceivable:

(i) Multiple narrowband LNAs
(ii) A broadband LNA [7][8]
(iii) A narrowband LNA with multiple pass bands [9]
(iv) A narrowband LNA that is tunable/reconfigurable [10].

Fig. 5(a) and (b) show two different interfaces to the LNA. While the LNA of Fig. 5(a) has a separate interface for each receive band, the one of Fig. 5(b) has a common interface and the filter outputs must either be combined off- or on-chip. Thus, Fig. 5(a) is suited when multiple narrowband LNAs are employed and Fig. 5(b) fits for the approaches (ii) and (iii) of the above list. For approach (iv), either interface is conceivable. Only recently, broadband LNAs similar to the one in Fig. 6 have been proposed [7][8]. By preceding an inductively source-degenerated cascaded amplifier by an LC-ladder filter (e.g. based on a Butterworth or Chebychev prototype), a broadband match can be achieved while the noise figure is not compromised as is e.g. the case for resistive shunt-feedback broadband amplifiers. In [8], a competitive noise figure of 2.5 dB has been measured between 3 and 6 GHz for an LNA using a 2nd-order Butterworth filter to achieve the broadband match. Nevertheless, as broadband LNAs may not be competitive enough for established cellular standards (GSM, W-CDMA, etc.), a possible solution is to use approach (i) or preferably (iv) for multi-standard operation of cellular standards, and to use broadband LNAs to cover less demanding RATs (e.g. of the wireless LAN/MAN family).

C. Analog to Digital Converters (ADCs)

Recent ADC developments for wireless terminals show 60-90 dB dynamic range of the ADC at an acceptable power consumption when compared to the rest of the receiver. An architecture that can trade speed for resolution is the ΣΔ modulation ADC, making it an attractive converter architecture for multi-standard applications. ΣΔ modulation uses oversampling in combination with noise-shaping to increase the resolution [11]. Due to its noise-shaping behaviour, ΣΔ ADCs offer an attractive approach to realize high performance data conversion without relying on the use of high precision and accurately trimmed analog components.

Discrete-time (DT) ΣΔ modulators potentially consume more power than continuous-time (CT) implementations because they require amplifiers with high bandwidth to satisfy the settling requirements. On the other hand, CT ΣΔ modulators are more sensitive to clock jitter than their DT counterparts. However, DT loop filters scale with the sampling frequency unlike their CT equivalent. This makes a cascaded and/or multibit DT ΣΔ ADC most attractive for multi-standard applications.

VI. FLEXIBLE RF TRANSCEIVER PROTOTYPE

The DFE introduced in section IV is implemented and integrated with a flexible RF transceiver prototype in the frame of the E^2R project. This prototyping work is complementary to the more architectural studies that were presented in the above sections. It allows of course the validation of the proposed RF/BB architectures, but more than that, it allows the validation of the key concepts and scenarios developed in the overall E^2R project. From a RF point of view, the main objective of the proposed prototype is to show that a highly reconfigurable RF transceiver is possible with existing available components.

A. Key features

First of all, the targeted prototype (see Fig. 6) is very ambitious in term of frequency bands, since the objective is to address from 400 MHz to 7.5 GHz, with a maximum bandwidth of 20 MHz. Hence, we will be able to receive and transmit almost all the existing commercial Radio Access Technologies. Concerning the transmitted power, the target is comparable to existing GSM terminals (+21 dBm). On the receiver side, the objective is to have a noise figure from 8 to 12 dB, depending on the frequency band. Since E^2R is also considering Multiple Antenna

Processing, the RF equipment will include up to 4 antennas and 4 RF chains. Finally, three keys features of the targeted prototype are:

- It will integrate advanced re-sampling functionalities as described in previous sections
- It will allow to communicate at the same time in different bands and different waveforms
- The board by default is Time Division Duplex based. It means that we use the same frequency band for Rx and Tx on one chain, and that a switch is used at the front end. In other words, one can only either transmit or receive. In order to implement a FDD system, one has to use 2 chains, one for the uplink, and one for the downlink.

B. Local oscillators

Since we address a very wide frequency band, the local oscillator generation is a key feature of the RF transceiver. The LO generation is based on a wide band frequency synthesizer (1.9 to 4.1 GHz) and a frequency doubler. Hence the LO range is from 3.8 GHz to 8.2 GHz. The drawback of this solution is that the frequency step is quite large, but it can be compensated digitally on the base band signals.

C. Transmitter section

The base band signal (zero IF) is in I/Q format, and fed to a quasi direct modulator. The chosen component allows one to generate a signal directly from base band to a frequency range from 4 to 8 GHz. The modulated signal is then filtered and amplified. Afterwards, a switch is used to separate low and high frequencies, if the signal shall be transmitted between 4 to 7.5 GHz

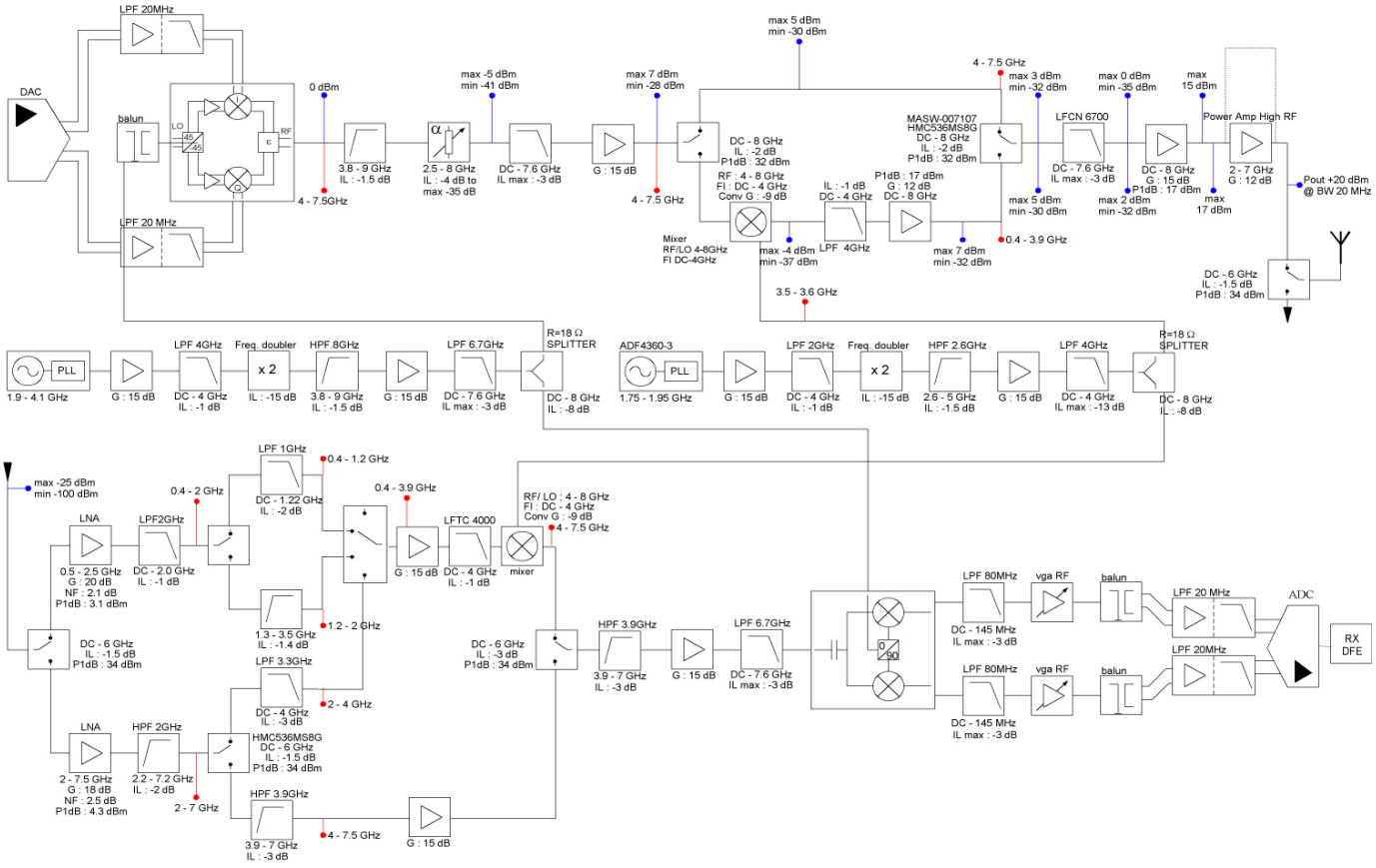

Fig. 6: Proposed prototype architecture.

D. Receiver section

This part is certainly the most difficult one, due to the very wide addressed frequency band (from 400 MHz to 7.5 GHz). As explained in section V, the LNA is a critical part, since the performance of existing wide band LNAs are not yet adequate (relatively high noise figure, non

constant gain vs. frequency). Hence, the overall frequency band is divided (by a switch) into 2 sub-bands, one from 400 MHz to 2 GHz, and another one from 2 GHz to 7.5 GHz. After the LNA stage, the signal is filtered and the frequency bands are again spitted in 2 sub bands. It gives us 4 sub-bands :

- 400 MHz to 1.2 GHz
- 1.2 GHz to 2 GHz
- 2 GHz to 4 GHz
- 4 GHz to 7.5 GHz.

This approach is used to decrease the amount off outer band interference (one has to keep in mind that basically all existing RATs are received at the antenna level, sometimes with huge level of signal). After this part, the architecture uses basically the same principle as for the transmitter section. We up convert the signal into a frequency range of 4 to 7.5 GHz and the signal is converted into base band thanks to an I/Q MMIC mixer. The base band signal is finally filtered and amplified.

VII. CONCLUSION

The provoking vision of an ideal SDR remains a "wish" for the foreseeable future due to the very limited ability for reconfiguration at RF. However, a highly reconfigurable RF transceiver seems possible (a) by retaining the paradigm of shifting as much signal processing from the analog to the digital domain – namely the channel selection – and (b) by employing broadband analog signal processing where RAT requirements allow. Along this line, a digitally enhanced frequency agile receiver architecture based on an analog DCR, an integrated ADC, and enhanced by a DFE was proposed. For such a receiver, the reconfiguration capabilities are mainly limited by the components of the front-end module, i.e. RF band pass filters, PAs, and antennas [13]. Prototype architecture is presented to try to overcome those problems, but surely further investigations are needed to reduce the complexity of a highly reconfigurable transceiver.

ACKNOWLEDGEMENT

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