IMPLEMENTATION OF A 2 MBPS SCA-ENABLED OVER-THE-AIR MILITARY SATELLITE COMMUNICATIONS TERMINAL

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ABSTRACT

MDA Corporation is the prime contractor for the Advanced SatCom Terminal (AST) Technology Demonstration Project (TDP), a project being developed for, and in collaboration with Defence Research and Development Canada (DRDC). The AST TDP is focusing on demonstrating the potential of replacing legacy communications terminals with a reconfigurable terminal capable of supporting multiple satellite communication waveforms at data rates above 2 Mbps.

The aim of this Technology Demonstration Project is to demonstrate a reconfigurable SatCom terminal based upon the Software Communication Architecture (SCA), which was developed by the United States Joint Tactical Radio System (JTRS) program and adopted by the SDR Forum. The two-year project is focusing on various configurations that complement the existing communications infrastructure in use by the Canadian Forces (CF) while adding new features and flexibility. The waveforms use general purpose processing and FPGA cores in conjunction with a full-featured SCA core framework to deliver SCA waveforms suitable for Satcom purposes.

1. INTRODUCTION

The goals of the AST TDP are to demonstrate the feasibility of extending software defined radios into high data rate satellite communications, to create within the CF an informed community on SDR, to position industry for possible future acquisitions by the CF, and to address key issues that would affect a CF decision to invest in SDR technology. This project will be the first step toward implementing SDR technology into CF operations, allowing increased allied interoperability and reduced life cycle costs.

The contract started in February 2004 and will complete in July 2006. Major milestones include the development and demonstration of the Intelsat waveform over the Telesat Anik satellite in October 2005, a demonstration of a military anti-jam waveform in January 2006, and the demonstration of a fully reconfigurable terminal in March 2006. MDA is acting as the prime contractor for the project, with Spectrum Signal Processing of Burnaby, Canada providing SDR hardware and SCA support, and QinetiQ Ltd. of Malvern, UK providing additional waveform design and development expertise.

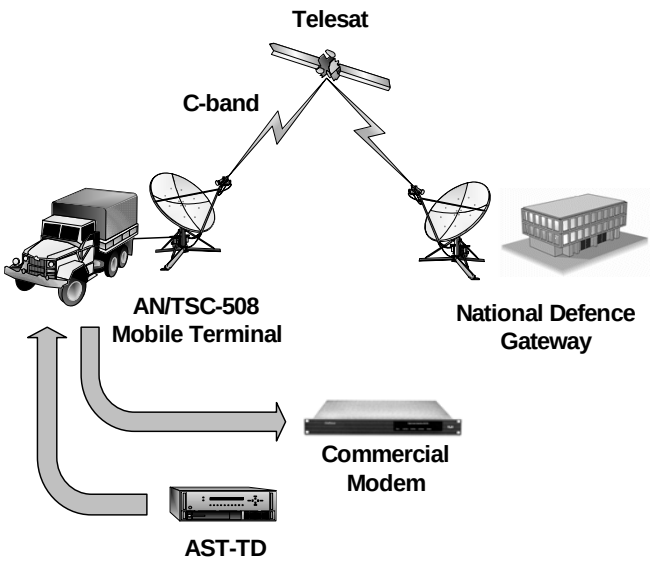

Figure 1. AST-TD Over-the-air Demonstration

Figure 1 provides a conceptual overview of the main over-the-air demonstration of the AST-TD, scheduled for October 2005. The AST-TD will be integrated into the AN/TSC-508 Mobile Ground Terminal, which is used by the Canadian Armed Forces on overseas deployments. This terminal provides a number of services to deployed units, including PBX (voice), teleconferencing, and data (via remote WAN access). The AST-TD will replace the commercial Intelsat modem normally used within the

AN/TSC-508 by connecting to the legacy terminal equipment via its IF ports and its V.35 baseband interface.

A Telesat C-band transponder will be used to establish a communications link between the ground terminal and the National Defence Gateway, located in Ottawa, Canada. The various services of the AN/TSC-508 will then be demonstrated over this link to prove that a reconfigurable, SCA-enabled SDR modem has the capability to transparently replace legacy radio modems and thus complement existing CF communications infrastructure.

2. WAVEFORMS

Since one of the primary aims of the AST-TD project is to show compatibility with existing CF military equipment, it was necessary to implement waveforms currently in use on CF equipment. As a result, it was decided to implement several waveforms compliant with the Intelsat IESS-309 specification [1]. The primary waveform, which is the waveform used in the over the air demonstration, is a QPSK Intelsat Business Standard (IBS) variant. This IBS variant also includes convolutional encoding, Viterbi decoding, IBS framing, and Reed-Solomon error correction. A number of software-controllable parameters were implemented in this waveform:

- Data rates from 128kbps to 2.048 Mbps
- FEC rates of ½ and ¾
- Selectable transmit and receive frequencies in steps of 100 Hz
- Output power control
- Internal data clock versus recovered data clock.

All waveform components were developed to meet IESS-309 requirements, and the completed waveform was fully tested in all modes with a commercial modem to ensure full functional compatibility with the standard. Output spectra were also examined to ensure that the transmitted waveform met the IBS specification for spectral shaping and carrier-to-noise levels.

In addition to the Viterbi/Reed-Solomon variant, an IBS QPSK variant was developed with Turbo coding as the forward-error correction scheme (compliant with IESS-315 [2]). This waveform also had a number of software-controllable parameters, similar to those in the Viterbi-based waveform. As the specification allows modem manufacturers to choose their own Turbo modes in their implementation, it was decided to test the Turbo-based waveform in loopback, rather than attempt to reverse engineer the Turbo parameters used in the commercial modem.

Two other waveform variants were developed in addition to the IBS variants. The first was a 16-QAM variant operating at 2 Mbps, and the second was a direct-sequence spread spectrum variant.

3. ARCHITECTURE

The AST-TD architecture (hardware, software and firmware) made heavy use of existing off-the-shelf technology, allowing us to focus more heavily on the design, waveform development and real-world demonstrations. By using COTS components wherever possible a number of benefits were realized:

- The development schedule would not be driven by hardware development cycles, allowing more time for waveform development.
- Procuring COTS hardware could be done more cheaply than developing hardware
- An off-the-shelf, supported SCA implementation and commercial board support packages allowed the team to focus more on the waveforms and less on the overall system integration
- IBS-compliant firmware modules meant that common, yet complex components, such as the Viterbi decoder and Reed-Solomon FEC would not have to be developed from scratch, but could be bought and integrated.

3.1. SDR Platform

The core hardware component of the AST-TD is the SDR-3000 software defined radio platform from Spectrum Signal Processing, Inc. of Burnaby, Canada. In its base configuration, the SDR-3000 provides three compact PCI boards within a 2U chassis. These three boards provide a number of PowerPC 405 and PowerPC 7410 processors, as well as four Virtex-II FPGAs, each containing approximately 6 million transistor gates. The I/O portion of the SDR-3000 has two bidirectional analog ports, each capable of transmitting and receiving waveforms at sampling rates up to 204.8 MHz.

In addition to its high processing throughput, the various processors and FPGAs within the SDR-3000 are connected together using a serial RapidIO-based fabric interface known as flexFabric. flexFabric supports sustained data transfers between processing components at rates up to 320 MB/s. As part of the total SDR-3000 package, Spectrum offers board support packages for all three of its boards, as well as QuicComm, a high-performance library for controlling all board-level functions.

A prime benefit of using the SDR-3000 is that it comes off-the-shelf with a fully integrated SCA v2.2 implementation, which includes Core Framework components specific to the SDR-3000. Other tools provided with the SCA package provide assistance with developing XML files for deploying developed applications, as well as a user interface for deploying and controlling waveforms during development. Spectrum has also modified its board support package to transparently establish high-speed flexFabric connections between components instead of using CORBA.

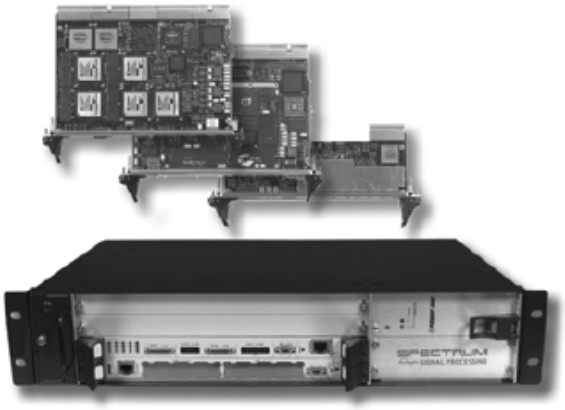

Figure 2. The Spectrum SDR-3000 Software Defined Radio Platform

3.2. Software/Firmware Architecture

As mentioned earlier, the SDR-3000 provides a number of general-purpose processors (GPP) and FPGAs, among which radio applications may be partitioned. In the AST-TD, higher-speed processing functions such as mixing, forward-error correction, modulation, and demodulation were allocated to the FPGAs, while lower-speed functions such as baseband data I/O and application control were allocated to the GPPs (see Figure 3). Data transfer between the GPPs and the FPGAs were implemented over flexFabric.

Application control for the firmware running on the FPGAs was established by implementing a memory-mapped, register-based control interface between the software and the firmware.

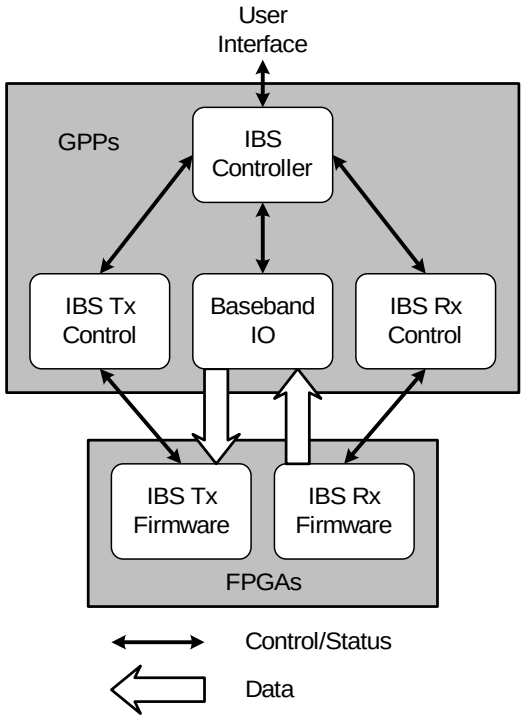

Figure 3. The AST Software/Firmware Architecture

4. DEVELOPMENT ENVIRONMENT

At the core of the waveform development environment for AST-TD is MATLAB, specifically System Generator from Xilinx. System Generator allows users to develop and test their DSP application within Simulink and automatically generate code for the design. The generated design can then be synthesized with XST or Synplify and implemented on FPGAs using Xilinx tools.

AST designs generated from System Generator were first prototyped on the XtremeDSP Development Kit from Xilinx. The XtremeDSP uses a Virtex-II FPGA that allows for easy portability between the prototyping board and the SDR-3000 (both provide Virtex-II FPGAs). The prototype board has analog inputs and outputs and is specifically designed for DSP application prototyping. Once AST-TD designs are successfully prototyped, they can be regenerated for the SDR-3000 with minimal changes.

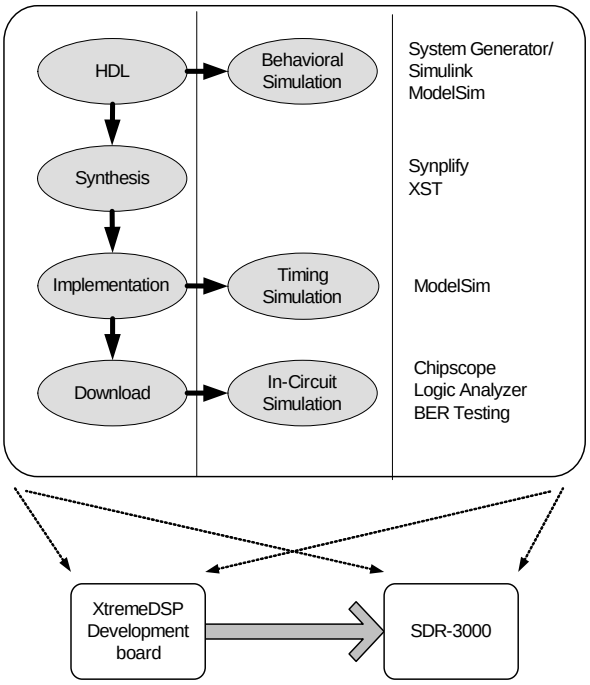

Figure 4. The AST Firmware Development Flow

ModelSim was used when necessary to simulate the interface between the waveform firmware and the rest of the SDR-3000 hardware by using a test bench provided by Spectrum Signal Processing. The System Generator design was integrated with an FPGA wrapper provided by Spectrum and the overall design was implemented using Xilinx tools. Final testing of the waveform on both hardware platforms was performed using Xilinx ChipScope.

4.1. Simulink and System Generator

Mathwork's Simulink software package allows for graphical block-based design within the MATLAB environment. The MathWorks provides various toolboxes for Simulink that allow developers to customize the available pre-built processing blocks and analysis tools to meet a specific application. System Generator is a toolbox designed by Xilinx to provide a DSP development environment for FPGAs within Simulink.

System Generator allows a user to design an application using pre-built Xilinx cores as the basic building blocks. For AST-TDP, almost the entire waveform was designed using these low-level, pre-built cores. On the rare occasion where these blocks were not sufficient, System Generator also enables the user to import custom VHDL code as a design block that can then be simulated and compiled within the overall design. Complex blocks such as FEC cores are also provided by Xilinx or can be black-boxed and easily placed within the waveform design.

Using System Generator, the design cycle was greatly shortened by simulating designs in Simulink before any code was written. System Generator provides bit-true and cycle-true DSP designs for specified hardware, allowing most testing to be completed in simulation. Once generated, these designs can then easily be placed in a larger overall design. The amount of testing of internal waveform components after generation is greatly reduced compared to a traditional FPGA design flow. Verification of the design is also simplified with System Generator's built-in support for ChipScope and ModelSim.

5. PROGRESS

The primary AST waveform (IBS variant) was completed in late summer 2005 and laboratory-based testing and evaluation was begun. The receive performance was measured by injecting a modulated signal into the AST from the commercial modem, with white noise added. Data rates up to 4 Mbps were assessed. The bit-error-ratio (BER) of the link was measured by using a standard BER tester. The BER versus Eb/No performance is shown in Figure 5. From the graph, it can be seen that the Rx performance is a full 1 dB below the Intelsat specification limit, and consistent with commercial modem performance. Transmit performance was measured by transmitting a modulated signal from the AST into the commercial modem, and verifying the BER performance at that end of the link. A spectrum plot of the AST transmitted signal and its related carrier can be seen in Figure 6. It can be seen on this plot that the AST Tx noise floor is over 65 dB down from the signal peak and approximately 80 dB down from the carrier peak.

The AST modem was integrated into the AN/TSC-508 ground terminal in September 2005 and evaluated over the air by exchanging traffic with the National Defence Gateway. Transmit and receive performance was measured by using BER testers at each end of the link and varying the transmitted power levels. The measured over-the-air performance was equivalent to the performance measured in the laboratory. When the transmitters at each end of the link were set to their normal operating power levels, no bit errors were encountered.

Further testing with the AN/TSC-508, incorporating the baseband digital services, will ensue in the late September/early October timeframe. Subsequent work will focus on increasing the data rate without affecting performance and the development of the frequency-hopped, military anti-jam waveform.

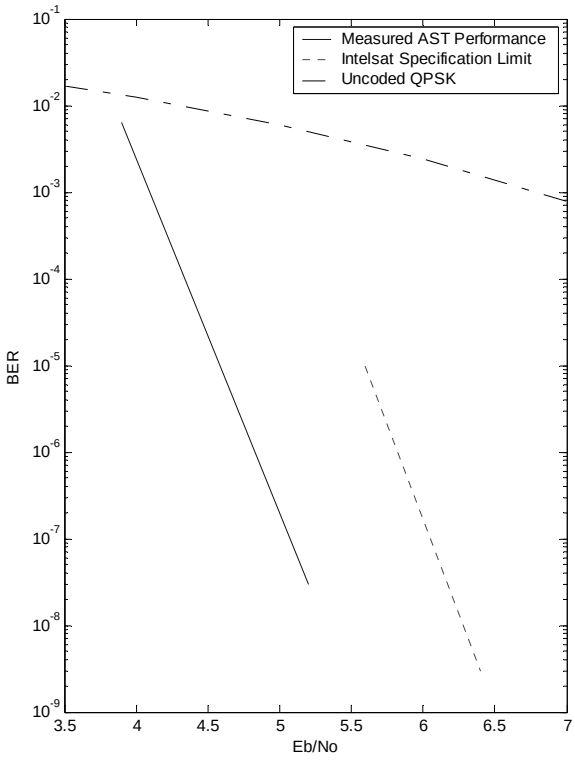

Figure 5. AST-TD BER Performance Graph

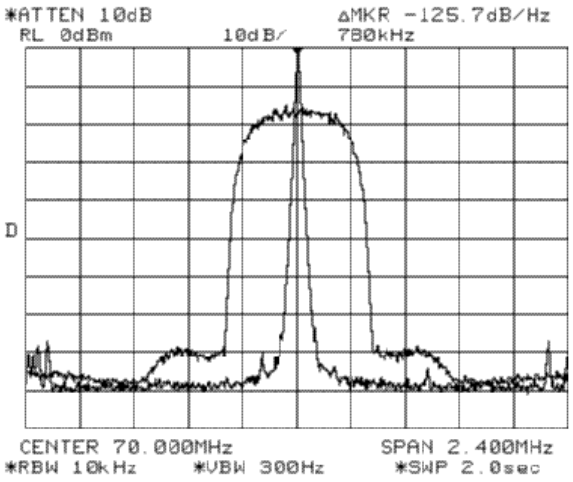

Figure 6. AST-TD Transmit Spectral Plot showing modulated signal and related carrier

6. REFERENCES

[1] Intelsat Ltd., "Intelsat Earth Station Standards (IESS), Performance Characteristics for Intelsat Business Services (IBS)," Document IESS-309, Rev. 8, 24 October 2003.

[2] Intelsat Ltd., "Intelsat Earth Station Standards (IESS), Performance Characteristics for VSAT Service using Turbo Coding with QPSK/OQPSK Modulation," Document IESS-315, 20 December 2002.