A Practical Transmit/Receive System for Software Radio

SDR Forum Technical Conference 2004

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- The Design Task
- System Components
- Design Partitioning
- Test System
- Results and Conclusions

Pentland Systems

- Design:
  - Test system to switch between two disparate modulation schemes under software control

- Evaluate:
 - Design Partitioning
  - Power Efficiency
  - FPGA Usage

![Pentland Systems]

- Digital RX/TX
  - Reconfigurable
  - Flexible
  - Modular
    - Mezzanine card (PMC)
    - PCI Bus
- Embedded DSP

Design Partitioning

Pentland Systems
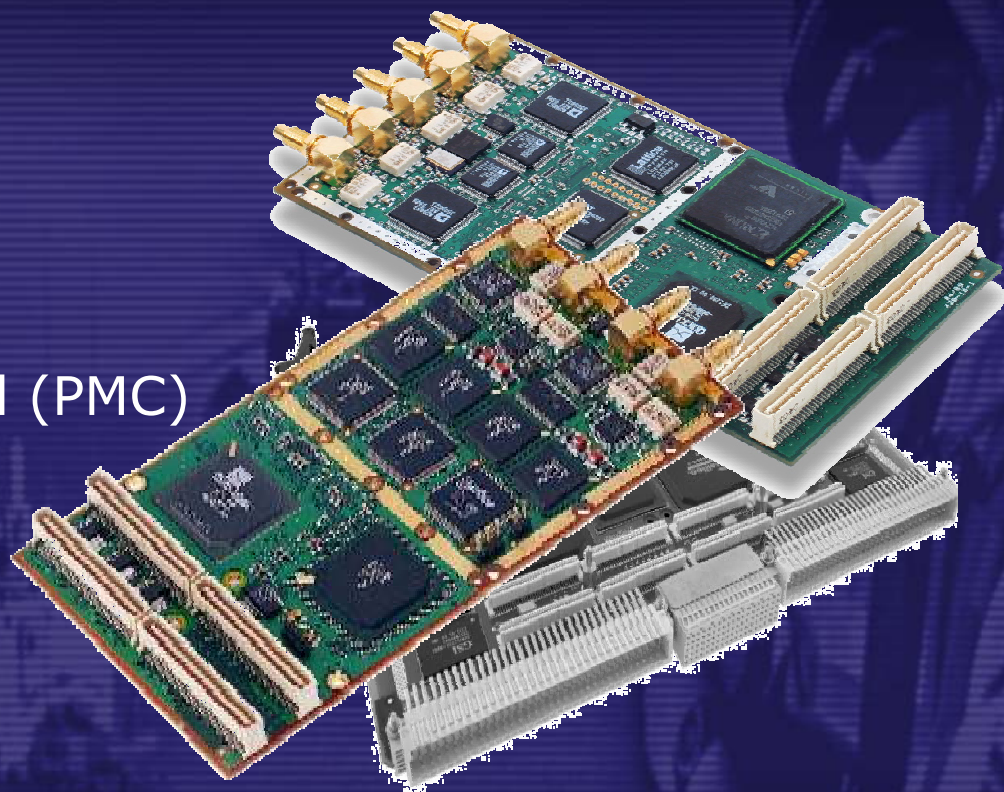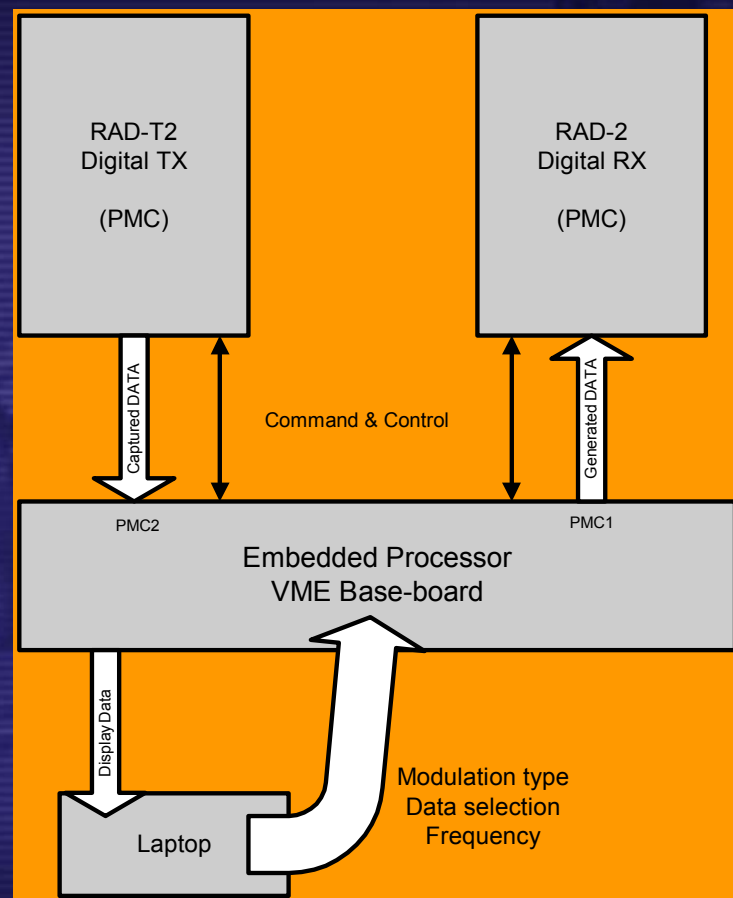
- FPGA or DSP
  - Flexibility vs Speed
  - Power Considerations
    - Battery Restrictions
    - Conduction Cooled environment
  - FPGA availability
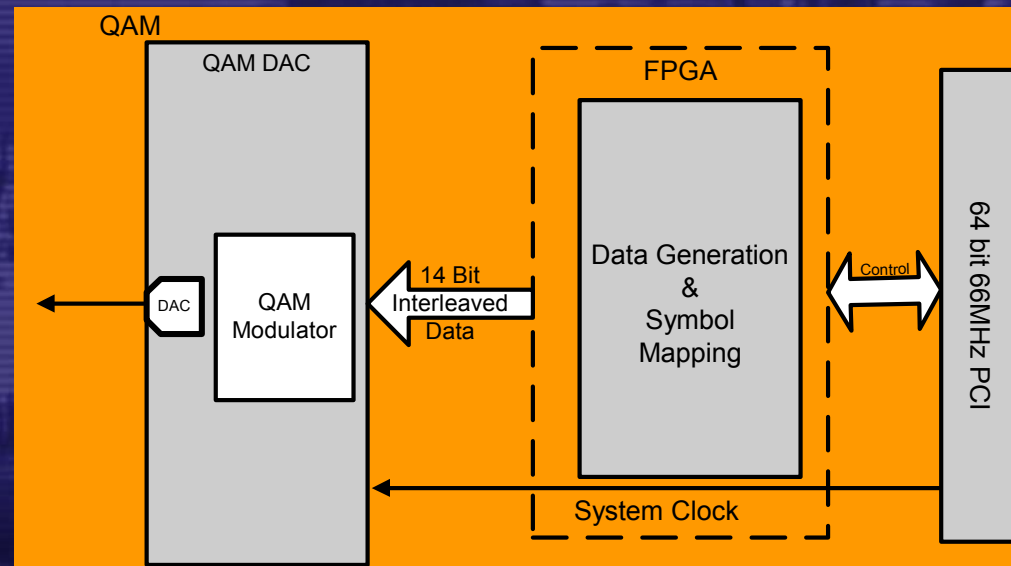 - Data Rates
    - Decimation/Oversampling

FPGA   DSP

DIGITAL RECEIVER   →   BASEBAND PROCESSING

Test System
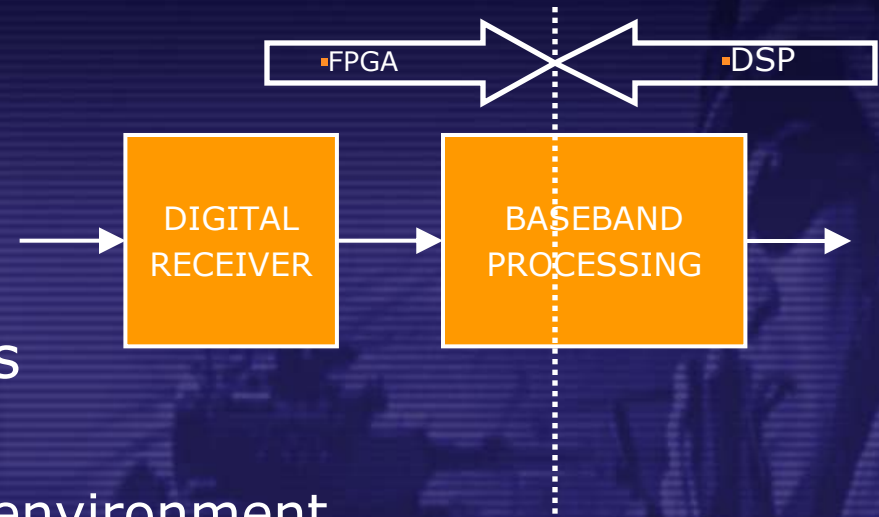
- **Modulation:**
  - QAM and FSK
  - Widely used
  - Disparate schemes
- **Design:**
  - Maximum Use of PMCs
  - No complex coding
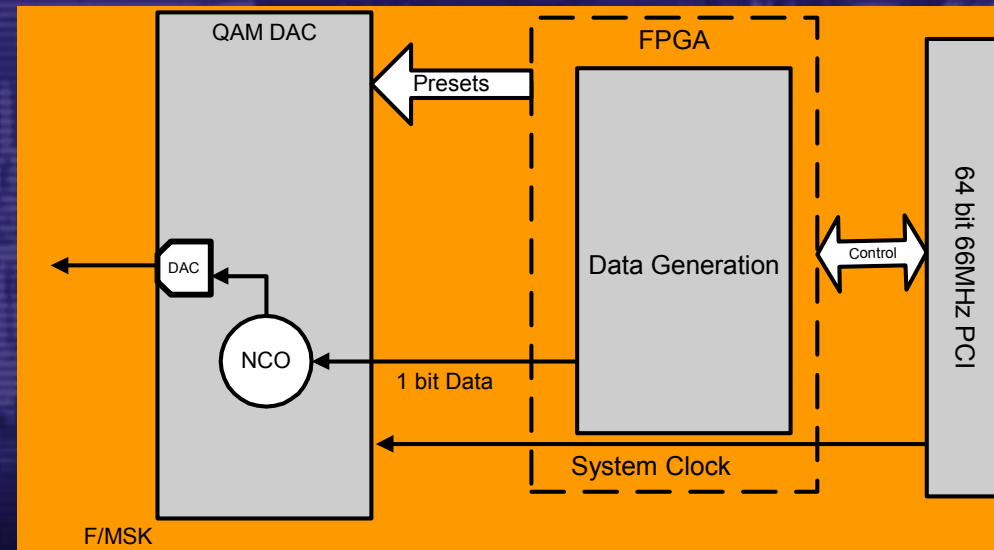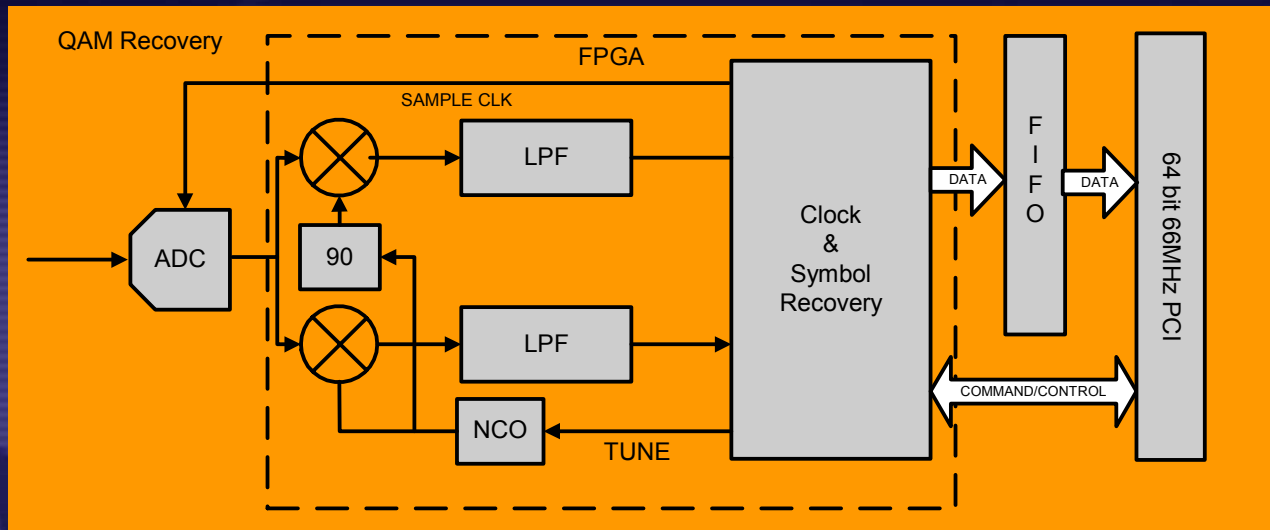 - Command line control – via laptop.

QAM

- DAC intrinsic capability
- FPGA
  - Data generation
  - Symbol mapping
  - Interleaving
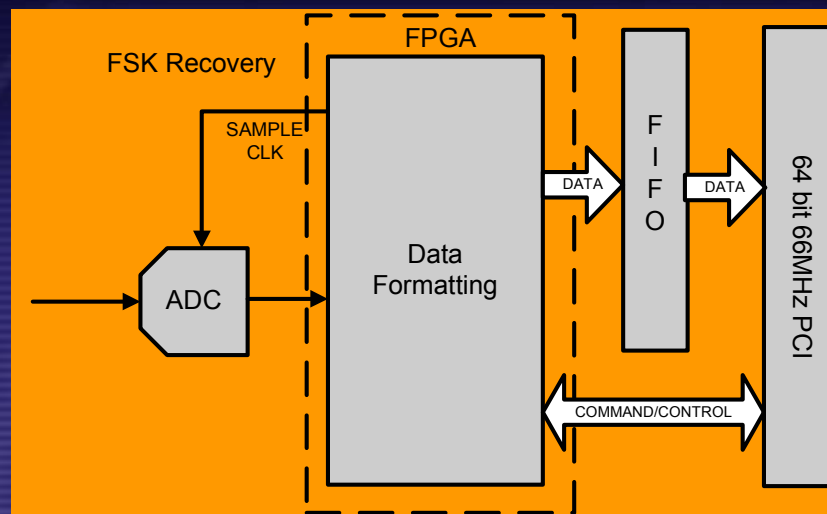 - Pre-Conditioning

FSK

- Modulating internal NCO
- FPGA
  - Preset Frequencies
  - Generate Data
  - MSK

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- QAM demodulator
  - Standard design
  - Single channel, 16-bit, 66MHz Fs
  - Decimation and filtering on-board

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- MSK 'demodulator'
  - could use QAM demod
- Straight digitizer
  - tests max data rates

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- Power
  - < 7W dissipation before modifications
  - QAM demod exhibits most power dissipation
    - Maximum additional power 2W

- Real Estate
  - ~10% of 3M FPGA in use before modifications
  - QAM demod largest circuit requirements
    - Adds 7% to circuit design

- Signal Performance

- Signal conditioning required close to conversion

- Careful consideration of design partitioning
  - Speed
  - Flexibility
  - Power
  - Real-Estate
  - Available Time

- PMC format good vehicle to deliver digitising and conditioning
  - Multiple DSP/FPGA cards available in VME.

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Come and talk to us in the Exhibits room