Sample Rate Converter for Digital Modulator

Zhuan Ye, John Grosspietsch
Motorola Labs
Why SDR needs SRC

- Many standards: many symbol/ship Rates
- SDR prefers common DAC/ADC clock source
- Example: GSM/EDGE/WCDMA Modulator
  - 270.833 ksym/s (GSM/EDGE)
  - 3.84 Msym/s (WCDMA)
Time-domain Interpolation

\[
\begin{align*}
(n-2)T_s & \quad (n-1)T_s & \quad (k-2)T_{out} & \quad (k-1)T_{out} & \quad nT_s & \quad kT_{out} & \quad (k+1)T_{out} & \quad (n+1)T_s \\
& & & & & & & \\
& & & & & & & \\
& & & & & & & \\
& & & & & & & \\
& & & & & & & \\
\end{align*}
\]

\[\mu T_s\]

\[t\]

\[=\] original samples

\[=\] interpolated samples
A Hybrid Analysis Model

\[ X(n) \xrightarrow{1/T_s} DAC \xrightarrow{X(t)} H_a(t) \xrightarrow{Y(t)} \text{Low Pass Filter} \xrightarrow{Y(k)} 1/T_{out} \]

- original samples
- interpolated samples
- resample process
All Digital SRC

\[ y(kT_{out}) = \sum_{i=-M}^{+N} x[(n_k - i)T_s]h_a[(i + \mu_k)T_s] \]

Sample interval

basepoints

Fractional interval

Basepoint index

(n_k-2)T_s \quad (n_k-1)T_s \quad n_kT_s \quad kT_{out} \quad (n_k+1)T_s
Traditional FIR Implementation

- Each output is an FIR operation
- FIR coefficients vary with fractional interval $\mu_k$
- Large memory requirements when $\{\mu_k\}$ gets large:
  - 4 basepoints
  - $\mu_k$: 8 bits representation
  - Coefficients: 16 bits representation
  - ROM size: $4 \times 16 \times 2^8 = 16384$ bits
Why Polynomial Based SRC

• Filter response is piecewise polynomial of $\mu_k$ in each sample interval
• Coefficients can be calculated on line based on $\mu_k$
• Hardware efficient implementation structure: Farrow structure
• Example: Lagrange polynomial based SRC
Impulse Response of Linear Phase Lagrange Polynomial Based SRC
Farrow Structure: Nested Polynomial Evaluation

\[ y(k) = \sum_{i=-M_1}^{M_2} x(n-i) \sum_{l=0}^{N-1} b_l(i)(\mu_k)^l \]

\[ = \sum_{l=0}^{N-1} (\mu_k)^l \sum_{i=-M_1}^{M_2} b_l(i)x(n-i) \]

\[ = \sum_{l=0}^{N-1} (\mu_k)^l v(l), \quad v(l) = \sum_{i=-M_1}^{M_2} b_l(i)x(n-i) \]
Farrow Structure: Implementation

\[
X(n) \rightarrow Z^{-1} \rightarrow b_2(1) + b_2(0) + b_2(-1) + \cdots
\]

\[
\{b_1(i)\} \rightarrow v(2) \times v(1) \times v(0)
\]

\[
y(k) = [v(2)\mu_k + v(1)]\mu_k + v(0)
\]
SRC Implementation: Key Pieces

- The basepoint index $n_k$
- The fractional interval $\mu_k$
- The Farrow structure for computation
Numerically Controlled Oscillator: SRC Control

- FCW = \( F_{in}/F_{out} \) \((F_{in} < F_{out})\)
- NCO register overflows at the rate of \( F_{in} \)
- \( N \) determines the frequency resolution
Digital Modulator Architecture

- Arbitrary $F_{DAC}$ not related to $F_{sym}$
Techniques Used in References

- F_{out} needs to be at least twice higher than F_{in}
- Different clocks for different stages of upsampling filters: difficult for software implementation
Why $F_{out} \geq 2F_{in}$

- MSB is assumed to toggle when NCO overflows

Clock ($F_{out}=100\text{MHz}$)

NCO overflow ($F_{in}=12.5\text{MHz}$)

NCO MSB ($F_{in}=12.5\text{MHz}$)

NCO overflow ($F_{in}=87.5\text{MHz}$)

NCO MSB ($F_{in}=87.5\text{MHz}$)
New SRC Architecture

NCO

Buffer read control

Fractional interval extraction

÷M

buffer

x(n)@F_{in}

y(k)@F_{out}

Increase n_k

From upsampling filters

Request for data (F_{sym})
Why the Buffer

- Decouples the upsampling filter from output clock rate
- Allows upsampling filters to be implemented using software
- “request for data” signal guarantees the balance of the buffer
**Basepoint Index** $n_k$ and **Fractional Interval** $\mu_k$

**Even number of basepoints** ($N=4$)

- Perform interpolation in the center interval
- Guarantee linear phase property of the interpolation filter

**Odd number of basepoints** ($N=3$)
$n_k$ vs. NCO

$T_{out}/T_{in}$

NCO register value
$n_k (N=even)$
$n_k (N=odd)$

SRC Control for Even Number of Basepoints

Buffer read address

To Farrow structure

NCO

Extract MSBs

carry

M

M

N

L

Fout

reg

Buffer read address

To Farrow structure

Extract MSBs

NCO

carry

M

N

L
Odd Number of Basepoints: Whether to Increment $n_k$

- **Case 1**
  - $n_0$
  - $t = T_{out}$

- **Case 2**
  - $n_1$
  - $t = T_{out}$

- Depends on these factors
  - Previous NCO register value $\geq 0.5$?
  - Current NCO register value overflows?
  - Current NCO register value $\geq 0.5$?
### Control Logic for $n_k$ Increment

<table>
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<th>Case #</th>
<th>$\text{NCO}_{k-1} \geq 0.5$</th>
<th>carry$_k$</th>
<th>$\text{NCO}_k \geq 0.5$</th>
<th>Increase $n_k$</th>
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</table>
Fractional Interval Extraction (N = Odd)

NCO \rightarrow \text{Extract MSBs} \rightarrow \text{Prepend} \rightarrow \text{MSB} \rightarrow L \rightarrow L+1 \rightarrow \mu_k \in [-.5,.5) \rightarrow \text{To Farrow structure}

\begin{align*}
\text{NCO} & \quad \text{Extract MSBs} \\
N & \quad MSB \\
\mu_k & \in [-.5,.5) \\
L & \quad L+1 \\
\text{To Farrow structure}
\end{align*}
A Digital Modulator Example

- Digital video broadcasting system (ITU J.83 Annex B standard)
- 64QAM: ~5.057 Msym/s
- 256QAM: ~5.36 Msym/s
- DAC clock = 100 MHz
Dual Channel Modulator Performance

- Two channels: 64QAM + 256QAM
- Polynomial based SRC (3 basepoints) after 16x interpolation
- EVM < 1%, ACPR > 65dB
Summary

• Sample Rate Converter (SRC) for digital modulator
• Polynomial based SRC and Farrow structure
• SRC architecture and implementation
• Digital modulator design demonstration and satisfactory performance