PERFORMANCE EVALUATION OF AN SDR SIGNAL PROCESSING BOARD USING A RECONFIGURABLE PROCESSOR

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ABSTRACT

Software defined radio (SDR) mobile terminals that can access multiple wireless communication systems are the trend of the future. An SDR wideband mobile terminal must be capable of high-speed data processing and low power consumption. Reconfigurable processors with these features show promise for SDR wideband mobile terminals. We have developed a signal processing board using a reconfigurable processor for an SDR mobile terminal and software for the IEEE 802.11a wireless LAN baseband part. We evaluated the power consumption and communication characteristics of the signal processing board, and confirmed the potential of SDR mobile terminals using a reconfigurable processor. This paper describes the configuration of the signal processing board using a reconfigurable processor and shows its performance evaluation results.

1. INTRODUCTION

Wireless communication systems, such as wireless LAN and cellular phone systems, have become popular all over the world, and the development of a software defined radio (SDR) mobile terminals that can access multiple wireless communication systems has rapidly accelerated. In 2002, we developed and evaluated an SDR prototype that uses conventional programmable devices, CPUs, DSPs, and FPGAs [1]. Although the developed SDR prototype supported Japanese personal handy phone systems (PHS, a 2G mobile system) and IEEE 802.11 wireless LAN, it could not support additional wideband systems. In addition, the conventional programmable devices were inappropriate for SDR mobile terminals due to their high power consumption and large size. Since an SDR wideband mobile terminal must be capable of high-speed data processing and low power consumption, a new approach that uses a reconfigurable processor with these features, is promising for SDR mobile terminals [2][3]. A reconfigurable processor has the following features: reconfigures circuit constitution dynamically in a few clocks, homo/hetero constitution multiple processor elements for high-speed parallel signal processing, and mounted high-speed data buses for high-speed signal processing. To evaluate the performance of reconfigurable processors for SDR mobile terminals, it is important to perform operation tests based on actual wireless communication systems.

NTT has developed an SDR signal processing board that uses a reconfigurable processor and software for the IEEE 802.11a wireless LAN baseband part, which requires high-speed data processing.

This paper presents the power consumption and signal processing performance evaluation results of the signal processing board and is organized as follows: Section 2 describes the configuration of a signal processing board. The results of performance evaluation are shown in Section 3. Section 4 concludes the paper.

2. SIGNAL PROCESSING BOARD CONFIGURATION

Figure 1 shows a developed signal processing board as a prototype of an SDR mobile terminal. The signal processing board uses an Adaptive Computing Machine (ACM) reconfigurable processor [4]. The size of the signal processing board is about 28 x 20 cm. Although four ACM processors are mounted on the signal processing board for high-speed signal processing, only two of them are used for the currently developed software. The ACM processor consists of three kinds of nodes: Programmable Scalar Node (PSN), Domain Bit Manipulation Node (DBN), and Adaptive X Node (AXN). The PSN is a kind of a RISC processor, the DBN can perform bit-intensive algorithms efficiently, and the AXN is a kind of parallel DSP. One ACM chip has two PSNs, four DBNs and four AXNs. To evaluate the ACM processor, we have developed software for IEEE 802.11a wireless LAN baseband part as one of the most

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sophisticated and high-speed SDR applications, and each software of signal process is assigned to the most suitable node [5].

Figure 2 shows a block diagram of the signal processing board. The two ACM processors perform the data processing functions of the PHY and MAC layers for the IEEE 802.11a wireless LAN. The host FPGA controls all of the data flow on the signal processing board, and Xilinx's Virtex-II XC2V6000 is used as the host FPGA. Two signal processing boards can cross-connect through a digital I/O interface, and the two PCs connected to the signal processing boards can communicate with each other on a peer-to-peer network. We evaluated the performance of the signal processing board when file transfer sessions were being carried out on the peer-to-peer network.

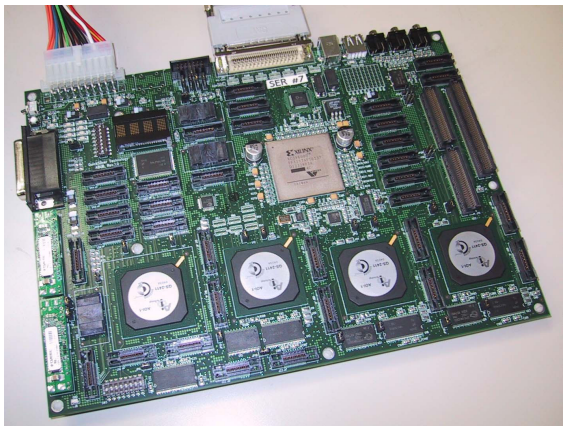

Fig. 1 Signal processing board.

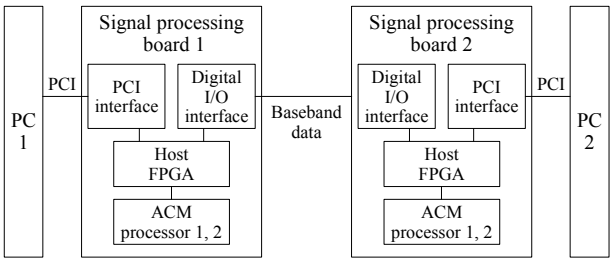

Fig. 2 Block diagram of the signal processing board.

3. PERFORMANCE EVALUATION

To confirm the applicability of the reconfigurable processor for SDR mobile terminals, we evaluated the power consumption and signal processing performance of the reconfigurable processor on the signal processing board.

3.1 Power Consumption

To measure the power consumption of the reconfigurable processor, an ammeter was connected to the processor, and the power consumption of the processor was measured during data communication.

The developed IEEE 802.11a wireless LAN software uses two processors, and each data processing task of the PHY and MAC layer is performed by one processor respectively. The evaluation conditions are shown in Table 1, and the measurement results of the peak power consumption of the reconfigurable processors are shown in Table 2. Table 2 also shows the measurement results of peak-power consumption in the software loading process for the PHY and MAC layers. Since the current version of ACM processor is not optimized from the perspective of power, the measured power consumption is not as small as that shown in Table 2. As a result of detailed power consumption analysis, we ascertained that the clock trees and their drivers consume about 80% of the total amount of power. By improving the power consumption of the clock trees and their drivers, the amount of power consumed by the processor can be reduced.

Table 1 Evaluation conditions.

Software	IEEE 802.11a wireless LAN baseband part
Data rate	54 Mbit/s
Clock speed	200 MHz
Processor assignment	Processor 1: PHY layer processing Processor 2: MAC layer processing

Table 2 Power consumption results.

	Power consumption [W]	
	During operations	During loading (Configuration)
PHY layer processing	1.59	1.56
MAC layer processing	1.09	1.06

3.2 Signal Processing Performance

In order to meet the IEEE 802.11a standards, the baseband processor must be capable of high-speed data processing. The Short Inter Frame Space (SIFS), which is the period from receiving a data packet to sending an ACK packet, is specified as 16 usec and it requires high-speed data processing to fulfill these standards. We have evaluated the SIFS by measuring the latency time of each

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data processing step on simulation software. This simulation software can precisely emulate the operation of the signal processing board. A block diagram of the transmitter and receiver of IEEE 802.11a wireless LAN is shown in Fig. 3. In Fig.3, SIFS is given by the following equation.

$$SIFS = Rx\ RF\ Delay + Rx\ PHY\ Delay + MAC\ Processing\ Delay + Tx\ PHY\ Delay + Tx\ RF\ Delay \quad (1)$$

In equation (1), the latency of the baseband data processing is shown as follows:

$$SIFS\_BB = Rx\ PHY\ Delay + MAC\ Processing\ Delay + Tx\ PHY\ Delay \quad (2)$$

Except for the *Rx RF Delay* and the *Tx RF Delay*, the targeted *SIFS_BB* should be set as 13.5 usec. We evaluated the *SIFS_BB* under the same evaluation conditions shown in Table 1, and the simulation results are shown in Table 3. In Table 3, the total time of *SIFS_BB* is larger than the targeted *SIFS_BB*.

Table 3 Baseband data processing latency.

	Latency [us]
Rx PHY Delay	16.06
MAC Processing Delay	1.43
Tx PHY Delay	1.36
SIFS_BB (Total time)	18.85

3.3 Performance Improvement Estimation

There are methods to shorten *SIFS_BB,* such as improving the software algorithm, changing the constitution of the reconfigurable processor, and increasing the clock speed. Since the current processor can run with a faster clock speed, we assumed the clock speed increase, and evaluated the effects of increasing the clock speed through simulations. The simulation results are shown in Fig. 4. As seen in Fig. 4, the targeted *SIFS_BB* can be realized when the clock speed is more than 280 MHz.

By increasing the clock speed, the power consumption of the processor increases. The simulation results of the power consumption are shown in Fig. 5. In Fig. 5, the power consumption required to process the PHY layer, the MAC layer, and both PHY and MAC layers on one processor is 2.2 W, 1.5 W, and 2.6 W at 280 MHz, respectively. By optimizing the software constitution, both PHY and MAC layers may be integrated into one processor.

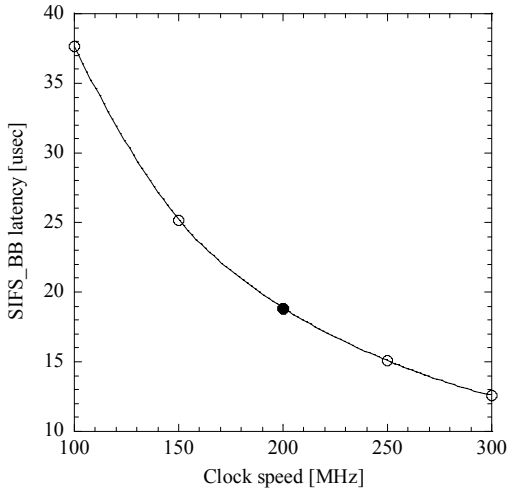

Fig. 4 Clock speed vs. SIFS_BB latency.

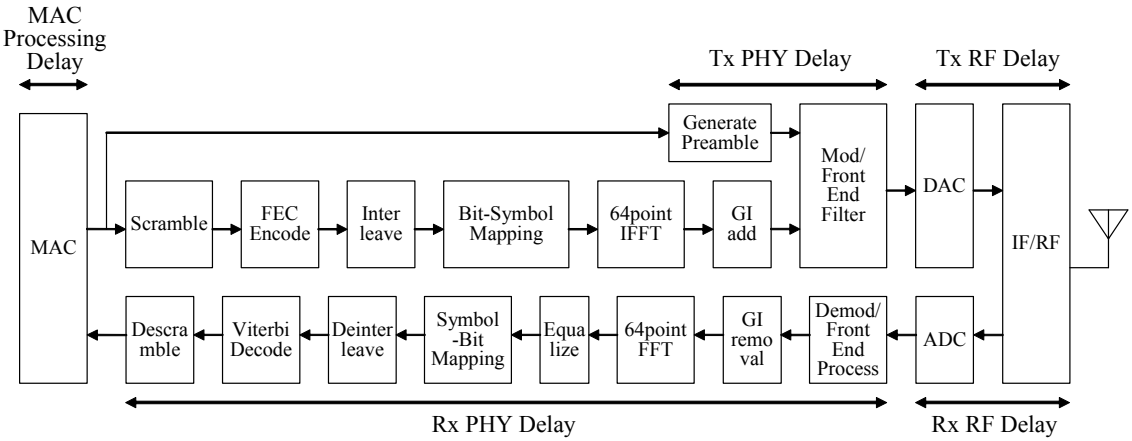

Fig. 3 Block diagram of the transmitter and receiver of IEEE 802.11a wireless LAN.

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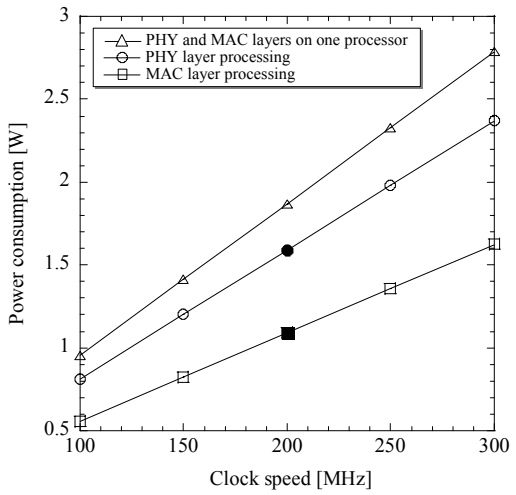

Fig. 5 Clock speed vs. power consumption.

We compared the power consumption of the reconfigurable processor with the high-speed DSP. In reference [6], the baseband data processing for the PHY layer of IEEE 802.11a wireless LAN receiver needed about 85 GOPS. For example, when six high-speed DSPs (Analog Devices Inc.: ADSP-TS201S, 14.4 GOPS) are used in parallel, the power consumption was 13.2 W, while our estimation shown in Fig. 5 was 2.2 W with 280-MHz clock speed for the PHY layer. Therefore, the power consumption of the reconfigurable processor could be reduced to about 1/6 that of the high-speed DSP. However, since the power consumption of the current version of the reconfigurable processor is not as small as for mobile terminals, achievement of even lower power consumption for the processor is expected. Since the clock trees and their drivers consume about 80% of the total amount of consumed power, as described earlier, by improving the power management and process rules, it is expected to reduce the power consumption for applications in mobile terminals in the near future.

4. CONCLUSIONS

We have developed a signal processing board using a reconfigurable processor for an SDR mobile terminal and software for the IEEE 802.11a wireless LAN baseband part. We evaluated the data transmission characteristics and the power consumption, and showed the potential of SDR mobile terminals using a reconfigurable processor. Since the power consumption of the current version of reconfigurable processor is not as small as that required for mobile terminals, achievement of even lower power consumption for the processor is expected.

5. REFERENCES

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