Wideband Modem Design Using FPGAs

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Outline

- Analog Up Conversion
- Digital Up Conversion (DUC)
- Polyphase Digital Up Conversion
- Conclusion
- Questions
Analog Up Conversion

- Current Modems
  - Digital Baseband
  - Digital Intermediate Frequency (IF) → Possibly
  - Analog RF (Possible Direct Up Conversion)

FPGA-based Digital IF & Baseband Processing
Analog Digital Up Conversion

- Impairments are Introduced
  - High Order Mixing Products
    - 3rd, 5th, 7th, ... Order Terms
  - Error Vector Magnitude (EVM) Impairments
    - I/Q Phase & Magnitude Imbalance
  - Carrier Feed-through
  - Harmonics
  - Sideband Noise

- Analog Filter Characteristics
  - Non-Linear Phase
  - Group Delay Variation
Moving from Analog to Digital

Advantages
- Higher Performance
- Lower Implementation Loss
- Time to Market
- Flexibility

Disadvantages
- Incremental Cost
- Higher Power
Digital Up Conversion

- Quadrature Digital IF
- Eliminates I/Q Imbalance (EVM Distortion)
- Single D/A Converter

FPGA
Digital Up Conversion in FPGA

- Current FPGAs are Feature Rich
  - Arithmetic Operators
  - Embedded Memory
  - High-Speed I/O
  - PLL

FPGA Clock Speeds are >300 MHz
  - Bandwidths up to 150 MHz
## Altera’s Stratix II FPGA Family

<table>
<thead>
<tr>
<th>Device</th>
<th>Equivalent Logic Elements</th>
<th>Total Memory Bits</th>
<th>18x18 Multipliers</th>
<th>PLL</th>
</tr>
</thead>
<tbody>
<tr>
<td>EP2S15</td>
<td>15,600</td>
<td>419,328</td>
<td>48</td>
<td>6</td>
</tr>
<tr>
<td>EP2S30</td>
<td>33,880</td>
<td>1,369,728</td>
<td>64</td>
<td>6</td>
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<tr>
<td>EP2S60</td>
<td>60,440</td>
<td>2,544,192</td>
<td>144</td>
<td>12</td>
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<tr>
<td>EP2S90</td>
<td>90,960</td>
<td>4,520,448</td>
<td>192</td>
<td>12</td>
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<tr>
<td>EP2S130</td>
<td>132,540</td>
<td>6,747,840</td>
<td>252</td>
<td>12</td>
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<tr>
<td>EP2S180</td>
<td>179,400</td>
<td>9,383,040</td>
<td>384</td>
<td>12</td>
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</tbody>
</table>
Digital Up Converter

- Stratix II Common Building Blocks
- Speeds at >300 MHz
- Nyquist Bandwidth of ~150 MHz

<table>
<thead>
<tr>
<th>Component</th>
<th>Maximum Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIR Filter</td>
<td>339 MHz</td>
</tr>
<tr>
<td>NCO</td>
<td>404 MHz</td>
</tr>
<tr>
<td>FFT (256 point)</td>
<td>314 MHz</td>
</tr>
</tbody>
</table>
Polyphase Approach

- Current D/A converters Have Sample Rates of >1 GSPS
  - Bandwidth of >500 MHz
- Standard DUC Approaches Limit Bandwidth to ~150 MHz
- Polyphase DUC can Take Advantage of D/A Sample Rates
  - Bandwidths up to DAC Nyquist
Polyphase Approach

- Familiar Polyphase Decomposition
- Each Sub-Filter Processes a Different Phase of the Input Signal
- Output Commutator Supplies Up-Sampling
Polyphase Digital Up Conversion

- Polyphase Decomposition of Up-Conversion
- Sub-DUC Replaces Sub-Filters
- Low Voltage Differential Signaling (LVDS)
  - Serializer Mux
  - Replaces Commutator
Sub-DUC Construction

- Mixer
- Filter
  - Normal Polyphase Decomposition
- NCO
  - Frequency
  - Initial Phase
  - Spectral Inversion Compensation
NCO Frequency

Set frequency Based on Desired Alias

\[ F_{a\_gen} = \begin{cases} 
F_{gen} & \text{for } F_{gen} < F_{s\_nco}/2 \\
F_{gen} - (F_{s\_nco} \times \text{alias}) & \text{for } F_{gen} > F_{s\_nco}/2 
\end{cases} \]

Where:
- \( F_{a\_gen} \) is alias frequency setting for the NCO
- \( F_{gen} \) is the desired output frequency
- \( \text{alias} \) is the Nyquist zone number
NCO Phase

Phase Set for Alias Frequency

\[ \phi_N = \frac{360 \times F_{\text{gen}}}{F_{s\_dac} \times N} \]

Where:
- \( N \) is the number of sub-DUCs
- \( F_{s\_dac} \) is the clock speed of the DAC
- \( F_{\text{gen}} \) is the desired output frequency
Conclusion

- FPGAs are Well Equipped for Digital Up Conversion
- D/A Converters with GHz Sampling Rates are Available
- Using Polyphase Decomposition & Aliasing, FPGAs Can Be Used to Interface to the GHz D/A Converters
Thank You

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