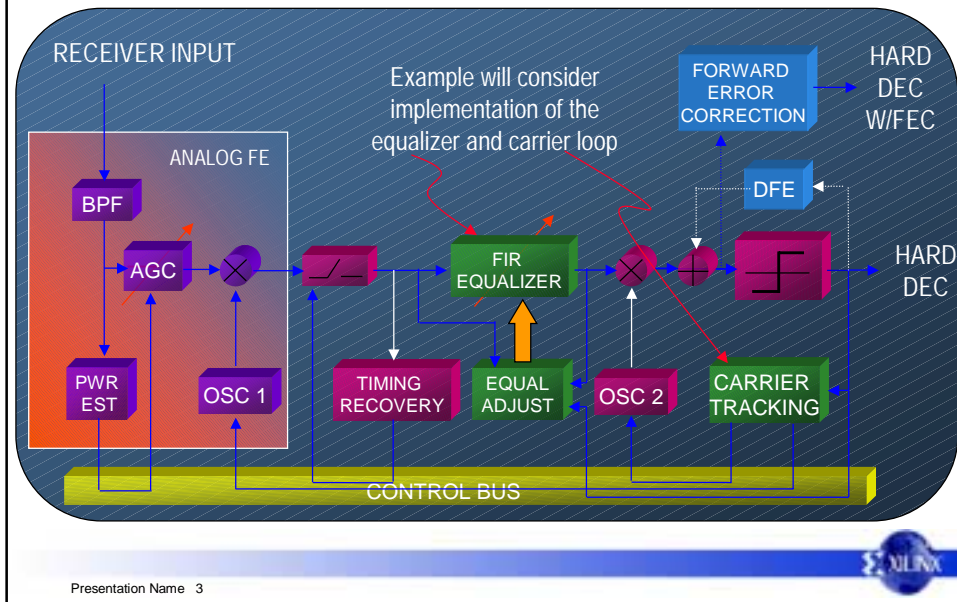
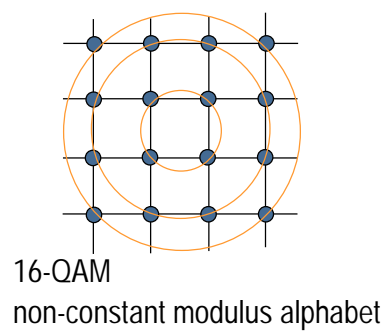
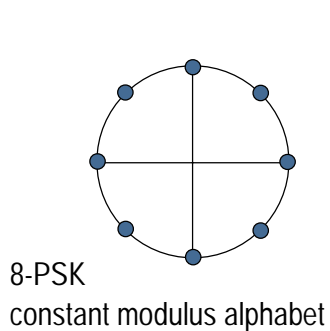


Equalized QAM Receiver



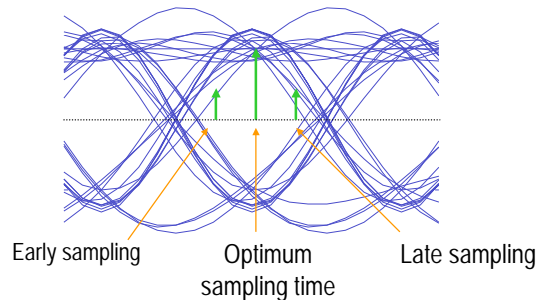
Signaling Set



Presentation Name 4

Timing Recovery

- Various options for timing recovery loop
 - Gardner loop (based on zero crossings in MF output)
 - Minimum variance loop (dither loop)
 - Maximum likelihood estimation (MLE)



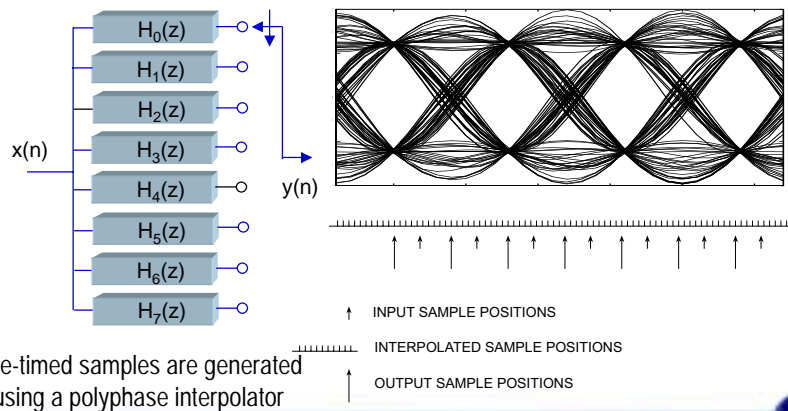
Presentation Name 5



Timing Recovery

Synchronous comm system operating over a bandlimited channel with AWGN must sample matched filter output when eye is maximally open

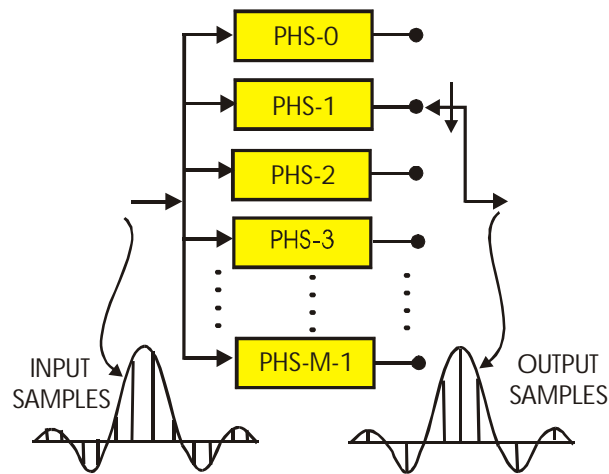
At this time ISI is minimal and SNR is maximum



Presentation Name 6



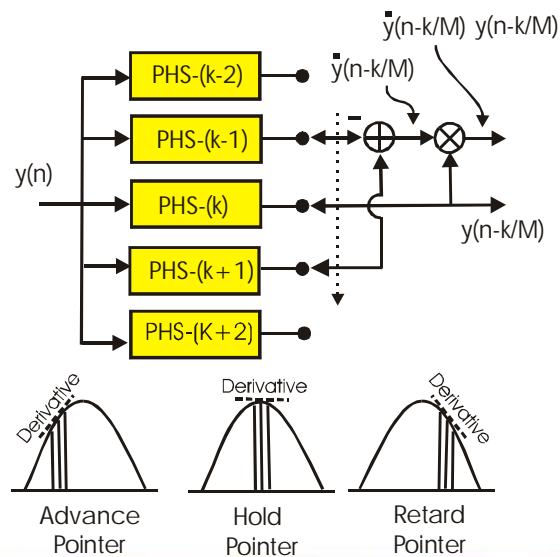
Timing Recovery



Presentation Name 7



Timing Recovery

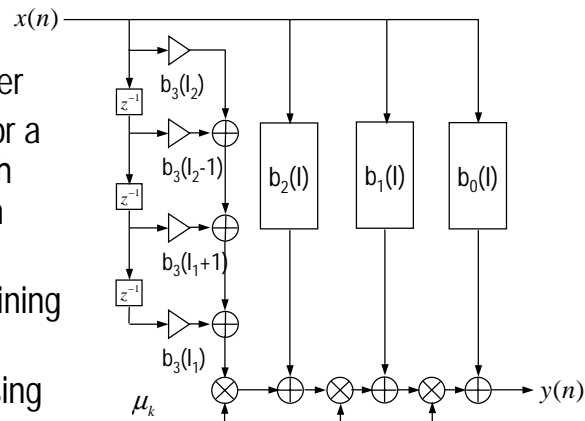


Presentation Name 8



Symbol Timing Recovery

- Farrow filter
- Polynomial based filter
- Figure shows case for a cubic interpolator with coefficients based on Lagrange formulas
- Single control for defining fractional delay
- Nested evaluation using Horner's rule



Presentation Name 9



Cubic Interpolating Polynomial

i	$i=0$	$i=1$	$i=2$	$i=3$
-2	0	-1/6	0	1/6
-1	0	1	1/2	-1/2
0	1	-1/2	-1	1/2
1	0	-1/3	1/2	-1/6

- Filter weights are fixed with this approach
- Could use table based approach for filter segments
- FPGA implementation could exploit
 - Distributed arithmetic
 - Canonic signed digit approaches

Presentation Name 10



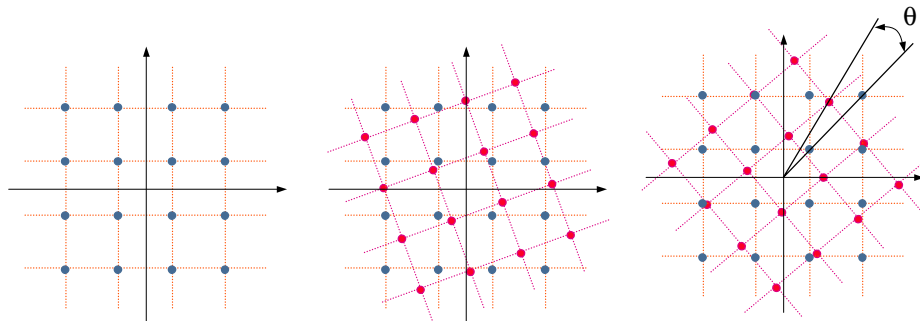
Timing Recovery Loop

- Non decision directed approach used in this implementation
- Embed Farrow structure in a servo control loop using a PI filter
- Drive loop with gradient measure computed around optimal sampling instant
 - Maximum eye opening

Presentation Name 11



Carrier Recovery



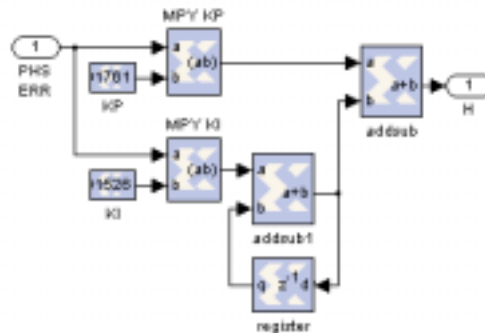
- Signaling waveform experiences rotational motion due to
 - Relative motion between Rx and Tx platforms
 - Mismatch between Rx and Tx analog mixers

Presentation Name 12



PI Loop Filter

- Uses two Virtex-II(P) embedded multipliers
- Small amount of fabric

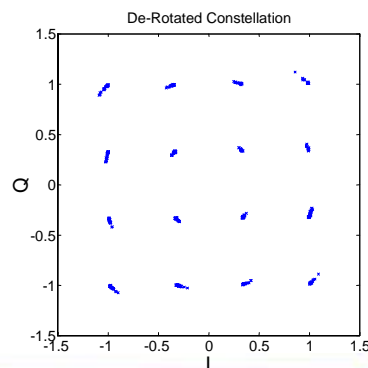
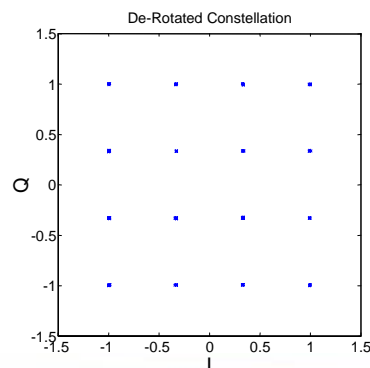


Presentation Name 17



Loop Simulation

- Floating-point reference
- Fixed-point: 4096x8-bit precision LUT
- 2 Virtex-II block ROMs

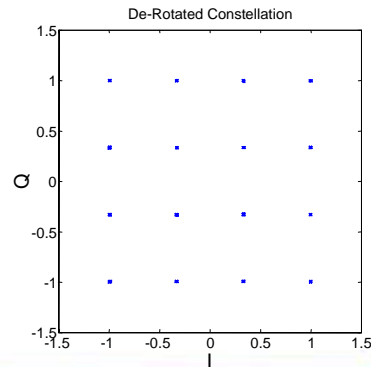
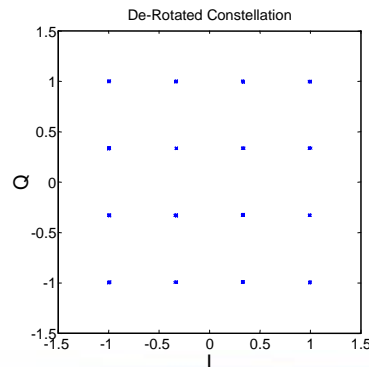


Presentation Name 18



Loop Simulation

- Floating-point reference
- Fixed-point: 16384x8-bit precision LUT
- 8 Virtex-II block ROMs

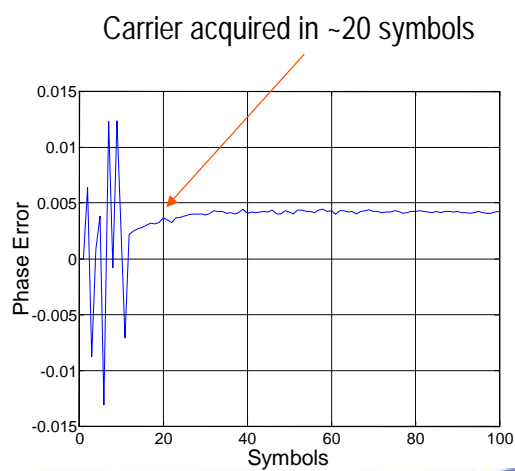


Presentation Name 19



Acquisition Time

- Floating-point
- 0.001 Hz Doppler
- 4 samples/symbol

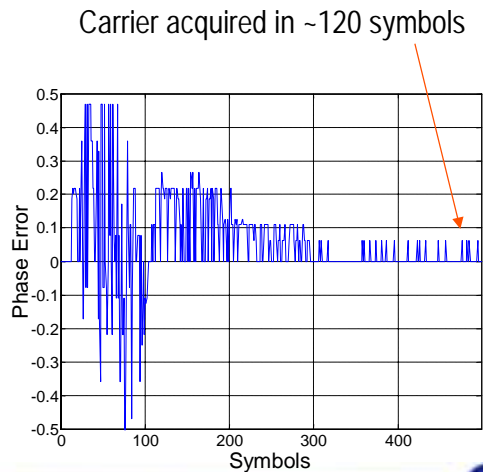


Presentation Name 20



Acquisition Time

- 4096x8 atan2() LUT
- 0.001 Hz Doppler
- 4 samples/symbol

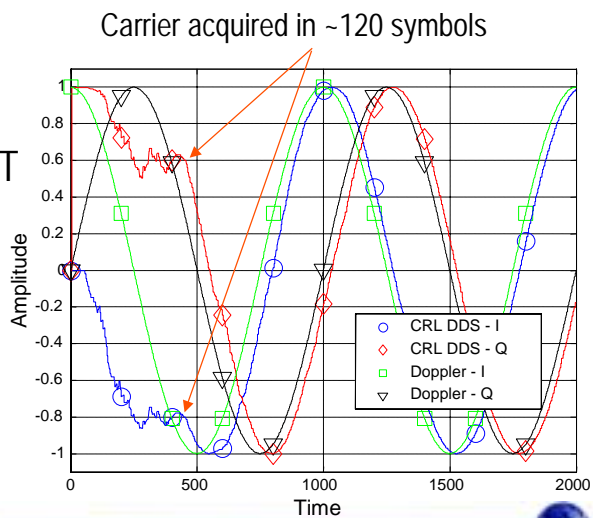


Presentation Name 21



Acquisition Time

- 4096x8 atan2() LUT
- 0.001 Hz Doppler
- 4 samples/symbol

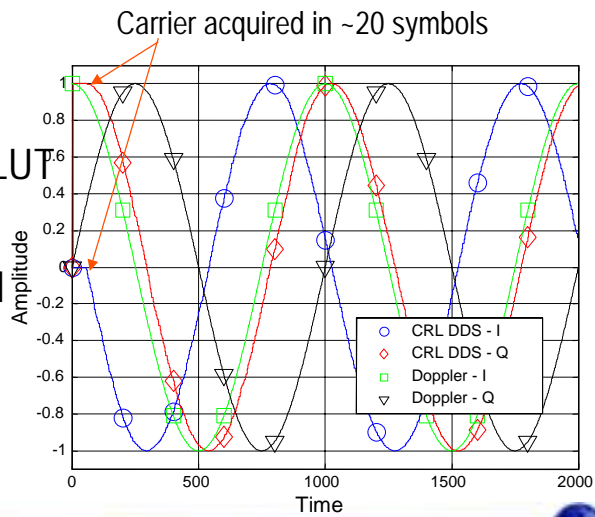


Presentation Name 22



Acquisition Time

- 16384x8 atan2() LUT
- 0.001 Hz Doppler
- 4 samples/symbol

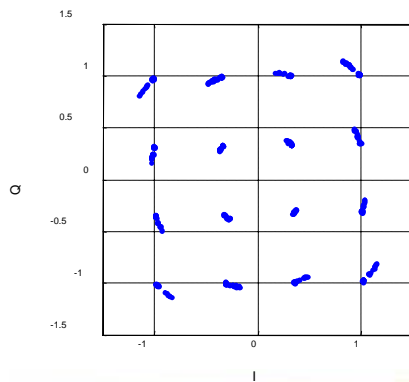


Presentation Name 23

Acquisition Time

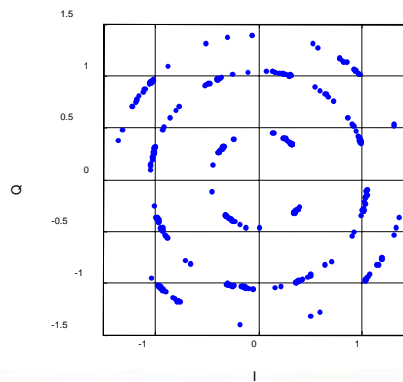
- Loop acquisition phase - symbols 50 to 400

16384x8 atan2() LUT



(a)

4096x8 atan2() LUT



(b)

Presentation Name 24

CRL Resources

Memory-based PD

Function	Slice Count	Block RAMs	Embedded Multipliers
Heterodyne	111	-	3
DDS	5	1	-
Loop Filter	32	-	2
Phase Detector	106	2	3
Total	254	3	8

Presentation Name 25



CORDIC PD

$$i = 0$$

$$z_i = 0$$

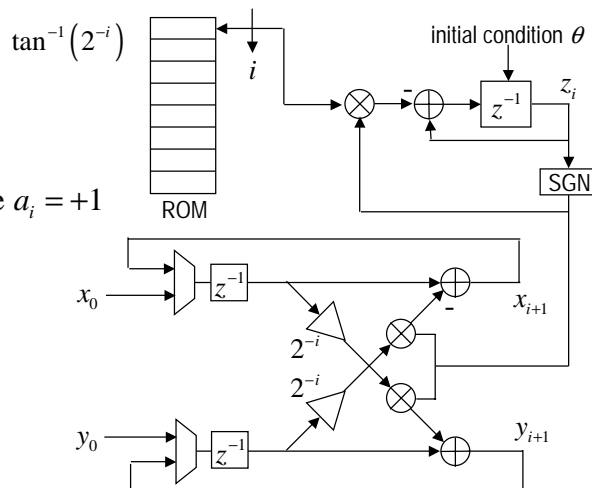
$$a_i = -1 \text{ if } z_i < 0 \text{ otherwise } a_i = +1$$

$$x_{i+1} = x_i + a_i y_i 2^{-i}$$

$$y_{i+1} = y_i - a_i x_i 2^{-i}$$

$$z_{i+1} = z_i + a_i \tan^{-1}(2^{-i})$$

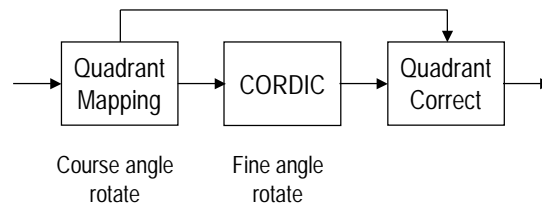
$$i = i + 1$$



Presentation Name 26



Extended CORDIC



- Algorithm converges for angles

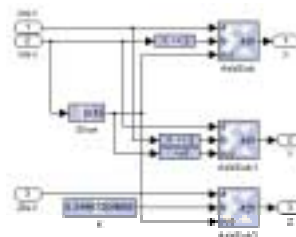
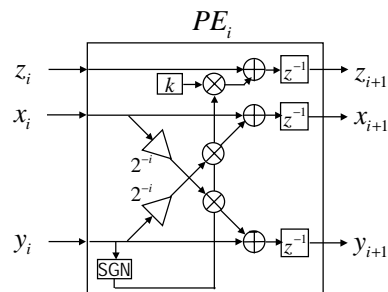
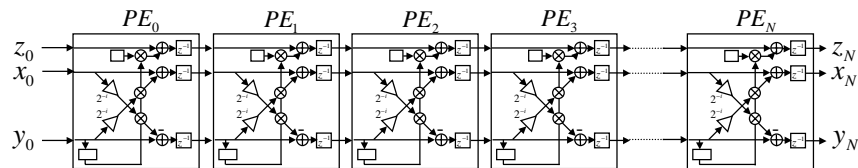
$$\frac{-\pi}{2} \leq \theta \leq \frac{\pi}{2}$$

- Need to map angles to quadrants 1 and 4

Presentation Name 27



CORDIC Fine Angle Processor



System Generator Implementation

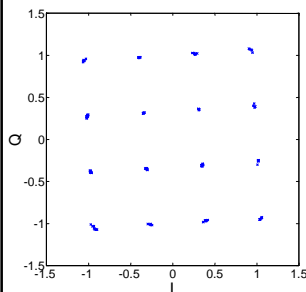
Presentation Name 28



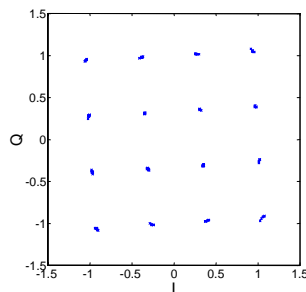
Acquisition Time

- 4 iteration CORDIC

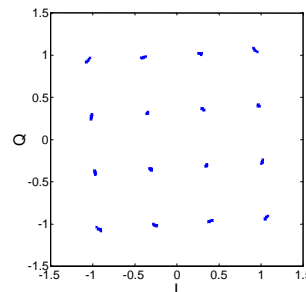
Q16.12 phase angle



Q14.10 phase angle



Q12.8 phase angle



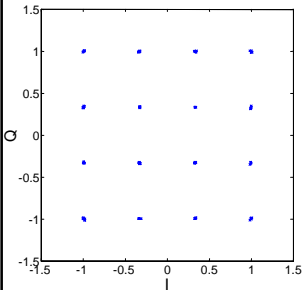
Presentation Name 29



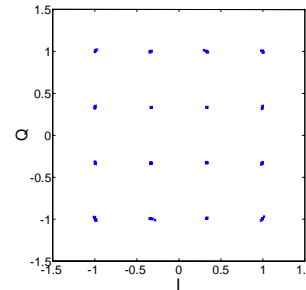
Acquisition Time

- 5 iteration CORDIC

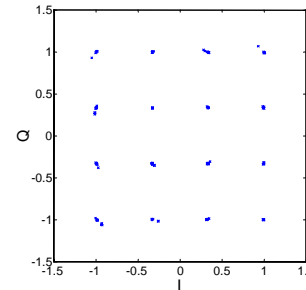
Q16.12 phase angle



Q14.10 phase angle



Q12.8 phase angle

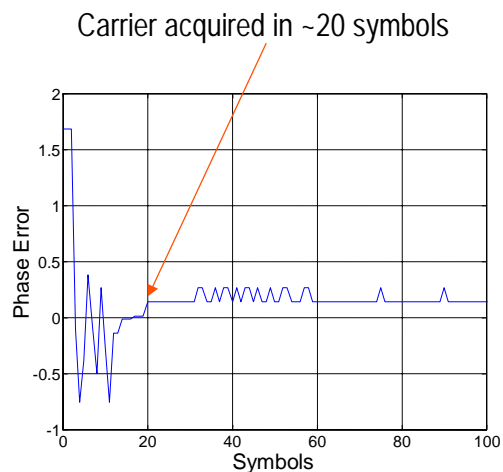


Presentation Name 30



Acquisition Time

- 0.001 Hz Doppler
- 5 iteration CORDIC



Presentation Name 31



CORDIC CRL Resources

Function	Slice Count	Block RAMs	Embedded Multipliers
Heterodyne	111	-	3
DDS	5	1	-
Loop Filter	32	-	2
Phase Detector	270	-	3

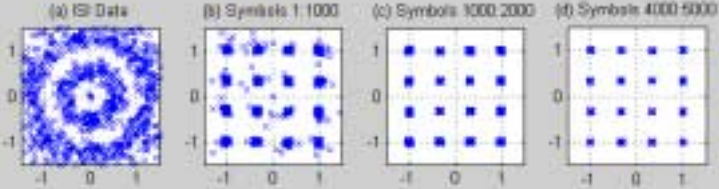
Total	413†	1	8
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† The small slice count discrepancy is due to logic optimizations that occur when the individual CRL components are integrated into the complete system.)

Presentation Name 32



EQ & CRL Simulation



The figure consists of four subplots arranged horizontally, each showing a 2D scatter plot of signal points on a coordinate system ranging from -1 to 1 on both axes. The subplots are labeled as follows:

- (a) ISI Data: Shows a dense, circular cloud of blue points centered at the origin, representing a noisy and distorted signal.
- (b) Symbols 1-1000: Shows a sparse collection of blue points that are beginning to form a grid pattern.
- (c) Symbols 1000-2000: Shows a more defined 4x4 grid of blue points.
- (d) Symbols 4000-5000: Shows a very clear and stable 4x4 grid of blue points, representing a clean 4-QAM constellation.

At the bottom of the slide, there is a blue horizontal bar. On the left side of this bar, the text "Presentation Name 33" is displayed. On the right side, there is a circular logo with the word "Xilinx" inside.

Top Level Design

- Verify demodulator in system level simulation environment

The diagram illustrates a system-level simulation environment for a demodulator. It starts with a '16-QAM DATA BPS (SHAPING & INTERPOLATION)' block connected to an 'M' block. A 'Mod Shaping F.L.T.R. Out' block is also connected to the 'M' block. The 'M' block is connected to a 'Timing Offset' block, which is further connected to a 'Channel' block. The 'Channel' block is connected to a 'DOPPLER' block, which is then connected to a 'Filter In' block. The 'Filter In' block is connected to a 'Filter Out' block, which is finally connected to a 'Control Code' block. The 'Timing Offset' block has a 'Timing Fixed Offset' input and a 'Timing var' input. The 'Channel' block has a 'Channel In' input and a 'Channel Out' input. The 'DOPPLER' block has a 'Doppler In' input and a 'Doppler Out' input. The 'Filter In' block has a 'Filter In' input and a 'Filter Out' input. The 'Filter Out' block has a 'Filter Out' input and a 'Filter Out' output. The 'Control Code' block has a 'Control Code' input and a 'Control Code' output. Arrows indicate the flow of data and control signals between these blocks.

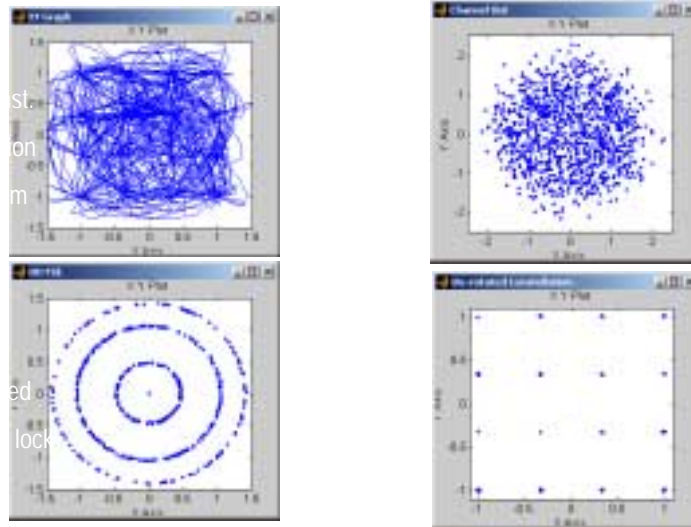
Timing impairment

Channel distortion

Doppler

Selectively enable/disable propagation impairments

System Generator Simulation



Presentation Name 37



Xilinx DSP Eval Board

- Virtex-II (XC2V1000/3000)
- Dual A/D D/A
- PCI & USB interface to host system



Presentation Name 38



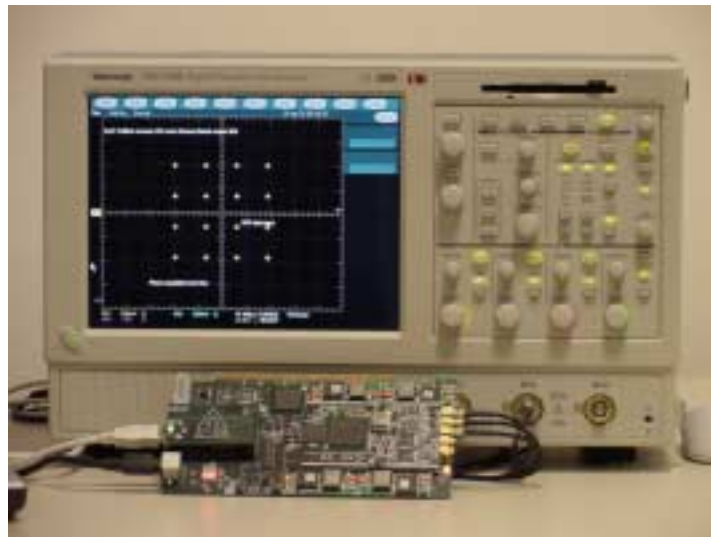
QAM Demod Simulation



Presentation Name 39



Equalized Signal



Presentation Name 40

