

A SOFTWARE DEFINED RADIO CHANNEL-PROCESSOR FOR 2G/3G-SYSTEMS - SOC – DESIGN EXPERIENCE WITH SYSTEMC, MATLAB AND VHDL -

Alfred Blaickner (Carinthia Tech Institute-CTI, Villach/Austria, a.blaickner@cti.ac.at)

Herman Sterner (Carinthia Tech Institute-CTI, Villach/Austria, h.sterner@cti.ac.at)

Martin Bacher (Infineon Technologies, Villach/Austria, martin.bacher@infineon.com)

Liu Shih-Fu (CTI, Austria) / Markus Mueller (Infineon Technologies, Austria)

ABSTRACT

The increasing performance figures of digital signal processing and circuit integration technologies show as well a significant influence on the design complexity of RF-radio systems and their functionality. The migration of typically analog radio functions into pure digital based implementation domains with several modes of operation is currently state of the art. Many reasons can be found in stringent performance and system requirements of various 2G/3G air-interface standards. Future base-station concepts need to provide several access and modulation formats. Within this work a re-programmable software radio channel processor for area efficient frequency translation is presented. For system flexibility and implementation efficiency the bandwidth-, frequency- and sample rate translation is carried out by dedicated multi-rate processing and filter-chains. The overall system performance and the analysis of the bit-true model with real-time results of the implementations on a DSP-/FPGA-based prototyping system are shown. Topics concerning the system design and the tool chain based on system modeling and synthesis techniques e.g. MatLab, VHDL and SystemC are included.

Keywords: Software defined radio-SDR, channel-processor, digital filters, digital down-conversion, DDC;

1. INTRODUCTION

For new digital receiver concepts increased functional specifications need to be mapped to an optimized area and power efficient architecture [2]. A pure software-DSP based solution is the easiest and the original idea of a software radio approach. But many of today's existing algorithms as e.g. IF-data processing are too demanding for the DSP-only software radio solution. Concerning the computational load, a multi-channel frequency translation and channel selection unit is a good example and test-bed for high speed digital processing. A digital channel-processing unit is placed just after the analog/digital-converter and is working at sampling rates in the range of 60 MHz up to 140 MHz.

To cope with the required IF-sampling rate and increased performance figures an alternative concept is proposed that supports the required channel processing functionality. Runtime re-configurable hardware accelerators are merged with DSP-cores in so-called *software defined radio*- architectural platforms. The DSP related computational loads are remarkably reduced and focused to a medium-/low sampling rate domain or even floating- point processing tasks at the near base-band side. The main processing burden remains inside the hard-wired and re-definable accelerator cores [1], an architectural solution that is employed within this project [1][3][4] and the basic concept shown in Figure 1.1.

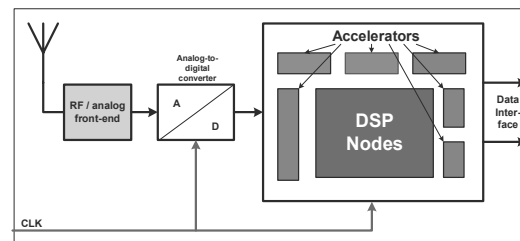


Figure 1.1: DSP-node and HW-accelerators.

In this work we present the design and rapid prototyping implementation of a digital high performance (>40 Msps at 16-20bit) quadrature channel processing unit - digital up-/ down- converter – DUDC. The unit may be individually re-configured and parameterized to both narrow- / broadband-software radio and base station applications [13]. The system signal processing and multi-rate filter-cores are interconnected with a programmable switching and routing network. The flexible switching and routing concept provides several operation modes e.g. simultaneous bi-directional up-/ down- conversion, re-usage and combination of programmable filter cores or adaptive antenna support. Additionally, each filter stage may be by-passed and powered down in the case of low decimation ratios and power efficiency reasons. The presented solution extends the RF-systems flexibility, as shown in Figure 1.2, from baseband to the IF-interface and integrates itself into multi-standard software radio receiver concepts. The overall system architecture with performance analysis results of the bit-true

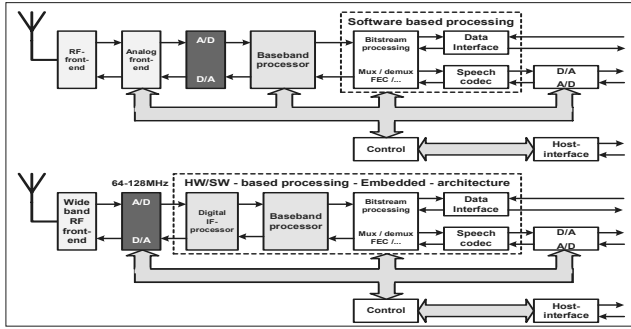


Figure 1.2: Migration of analog to digital RF-processing.

system models including the real-time measurement of the DSP/FPGA-based VHDL-/SystemC- prototyping implementation are shown in chapters (3) to (5).

2. THEORETICAL BACKGROUND

Digital frequency translation and channel selection (up/down-conversion) requires complex phasor rotation and sample rate conversion functions with image/alias-rejections included. The latter tasks may be typically carried out by multi-rate filter stages. Starting with the sampled IF-signal, the receive signal is given by $r_{IF}[m]$, with $[m]$ the sampled data index, $f_{LO}[m]$ the complex unity gain rotating phasor generated by the direct digital frequency synthesizer (DDFS), $T=1/f_s$, the sampling clock interval

$$r_{IF}[m] = r(t) \cdot \sum_{m=-\infty}^{\infty} \delta(t-mT) \quad \text{Eq. 2.1}$$

$$f_{LO}[m] = e^{-j\omega_0 mT} \quad \text{Eq. 2.2}$$

and with ω_0 , the angular intermediate frequency.

The filtered and down converted baseband results in

$$\begin{aligned} s_{BB}[m] &= \sum_{n=0}^{N-1} \{r_{IF}[m-n] \cdot f_{LO}[m-n]\} \cdot g[n] \\ &= \sum_{n=0}^{N-1} \{r_{IF}[m-n] \cdot \cos([m-n])\} \cdot g[n] \\ &\quad - j \cdot \sum_{n=0}^{N-1} \{r_{IF}[m-n] \cdot \sin([m-n])\} \cdot g[n] \end{aligned} \quad \text{Eq. 2.3}$$

with $g[n]$, as the sampled impulse response of the overall multi-rate filter chain.

Eq. 2.3 clearly shows that digital up/down-conversion may be performed with two methods:

Method 1: The mixer function (DDFS) shifts the band of interest to baseband. With several subsequent multi-rate filters the channel centered at zero frequency can be selected now. The performance characteristics as pass-band-ripple, selectivity or adjacent channel blocking attenuation are based on the response of the filter chain.

Method 2: A second approach uses the property, that instead of multiplying the receive signal $r[m]$ the low-pass filter impulse response $g[n]$ is rotated by the phasor $e^{-j\omega_0 mT}$. The operation transforms the filter into a band-pass-filter and the band of interest will be extracted first. With sophisticated decimation and filtering the channel is

implicitly folded down to the baseband or near baseband. The sampling rate and channel center frequencies need to be in a specific ratio, which limits the application range and will not further be addressed here.

For down-conversion we start with the *frequency shifter* (DDFS and quadrature mixer) that translates the band of interest from the IF-section to baseband [6][7]. For the specified characteristics as e.g. low phase noise and a spurious free dynamic range with SFDR ≤ 116 dB, a phase resolution of 32 bit and the usage of the so called *dithering* method is required.

The available output frequency of the DDFS is calculated by Eq. 2.4, with $\Delta\phi$ the phase-increment, f_{clk} the clock frequency and the phase-accumulator size $2N$.

$$f_{out} = \frac{\Delta\phi \cdot f_{clk}}{2^N} \Rightarrow f_{out} = \frac{\Delta\phi \cdot f_{clk}}{2^{32}} \quad \text{Eq. 2.4}$$

The frequency shift function itself is typically carried out with conventional vector rotation (complex multiplication) or alternatively by the CORDIC algorithm (Coordinate Rotation Digital Computer), which is a multiplier-less solution, both investigated within this project [2][7][14].

3. SYSTEM ARCHITECTURE AND DESIGN

The overall system architecture of the digital multi-mode channel processor is shown in Figure 3.1.

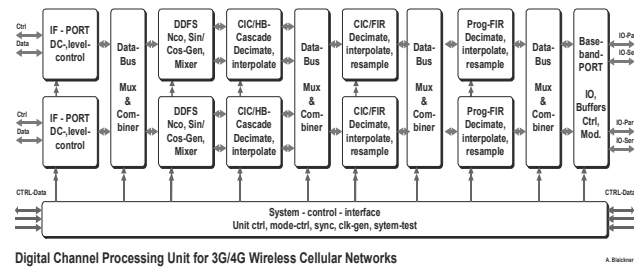


Figure 3.1: Channel processor architecture.

3.1. Channel processor architecture

Each of the channels consist of processing stages: (a) *IF-interface-port*, (b) *quadrature frequency synthesizer-mixer*, (c) *CIC-half-band-filters* (d) *RAM-coefficient-filter-processor* positioned at the low sampling rate side (baseband-side) and a (e) result data formatter. The re-definable operation / switching mode principle is shown in Figure 3.2.

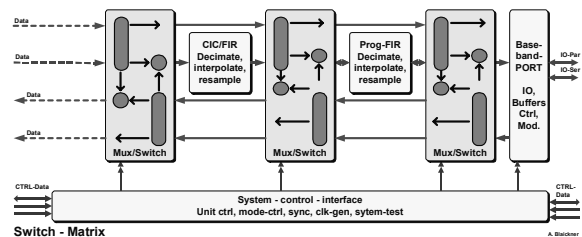


Figure 3.2: Re-definable switching architecture.

3.2. Frequency shifter

Each frequency-shifter (DDFS) includes a numerically controlled oscillator (NCO), a sine-/cosine-generator, a dither generator and a digital quadrature mixer. The NCO tuning resolution is 15-30 mHz at 64-128 Msps at a spurious free dynamic range of ≥ 116 dB. The sine-/cos-generator is based upon look up table- and compression- techniques. For the reached ROM-space savings, see Table 1.

Table 1 ROM-loss-less compression savings.

ROM Compression – Method	Savings [%]	Addr:18/16 bit
Without compression	-	8.388 Mbit
Sine-wave symmetry/2	75	2.097 Mbit
Hutchison method	> 85	1.056 Mbit
Infineon internal method	87.5	1.048 Mbit
Extended Infineon method	93	0,532 Mbit

Figure 3.3 shows the DDFS bit-true results with and without dithering – a randomization method for phase truncation errors.

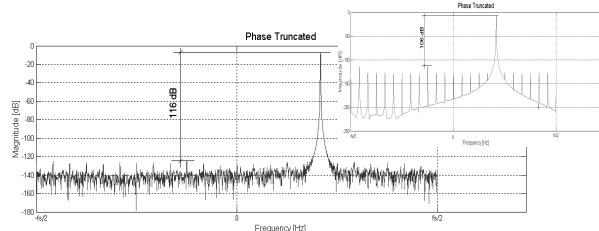


Figure 3.3: DDFS – spectra, ≤ 116 dB.

The CORDIC-processor bit-true results are presented in Figure 3.4.

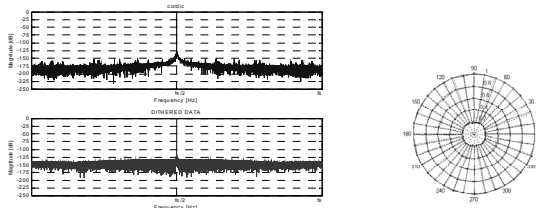


Figure 3.4: CORDIC bit-true analysis.

3.3. Averaging- and half-band-filter section.

Within this filter section either a CIC-filter or a half-band-filter cascade is selected. The CIC-filter is preferred in case of decimation ratios $\geq 1:8$, otherwise a half-band-filter cascade is used instead. The proposed CIC- filter-design is a flexible architecture with selectable filter performance and settings of e.g. the filter order (6 down to 1), a decimation ratio ($2^0 - 2^{16}$). The CIC-filter may also be setup either for interpolation or decimation at run-time and is shown in Figure 3.5.

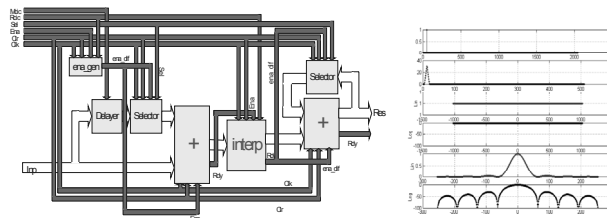


Figure 3.5: CIC— multi-mode architecture and filter response - order: 2, Dec 1:4.

For low complexity reasons, multi rate half band multistage filters are widely used in multiprocessing applications. The typical frequency response of a single half-band filter stage is illustrated in Figure 3.6. The frequency components above $fs/2$ are folded back below $fs/2$, but the range $fs/4$ to $fs/2$ is within the stop-band of the subsequent stage which is shown in Figure 3.7 for a three half-band filter cascade with aligned and zoomed frequency axes.

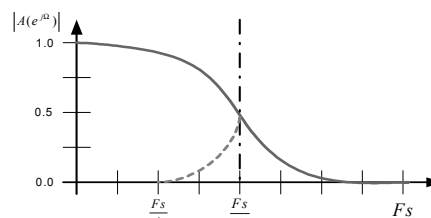


Figure 3.6: Half-band filter frequency - response.

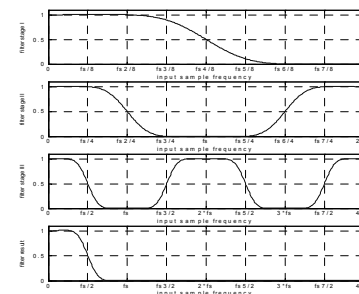


Figure 3.7: Frequency-response of the half-band-cascade.

Figure 3.8 and Figure 3.9 show the architectures used for the implementation in VHDL and SystemC.

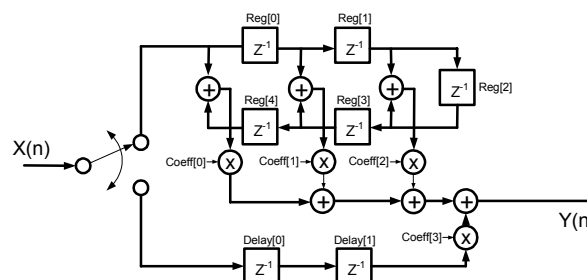


Figure 3.8: Halfband-filter architecture and cascade.

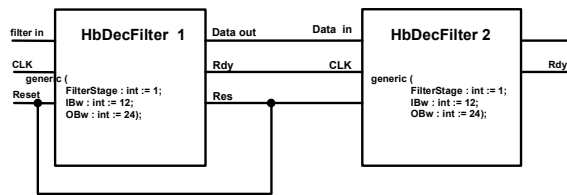


Figure 3.9. VHDL- / SystemC - implementation of the half-band – filter – cascade: Ord_15, Dec_1:2.

The selected setup with synthesis results of the overall filter-cascade are shown below and in Figure 3.10.

Stage - A/B: 7 / 19 coefficients
Input/output bus-width: Bw: 20bit
APEX20KE1500-1: SYSclk: 41.44MHz
Total LEs: 1314 (< 3% of total space)

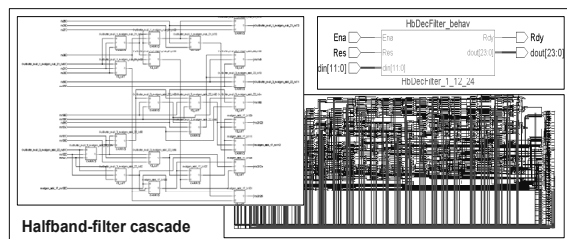


Figure 3.10: HB-filter cascade – RTL-level-netlist.

3.4. Programmable RAM-coefficient-filter unit

Each channel back end section (baseband side) includes a so-called RAM-coefficient-RCO-FIR-processor. The RCO-FIR block allows fractional-N interpolation/decimation ratios and is implemented as a programmable filter-engine. The filter-computes either a single high order FIR-filter or a cascaded polyphase filter chain. The VHDL-model of the filter-processor may be customized for a variable count of multipliers and RAM-slices (1 to 16). The coefficients are provided in a RAM or LUT for various filter responses. The implemented architecture is shown in Figure 3.11, with performance results at bus widths of 18bit in Figure 3.12.

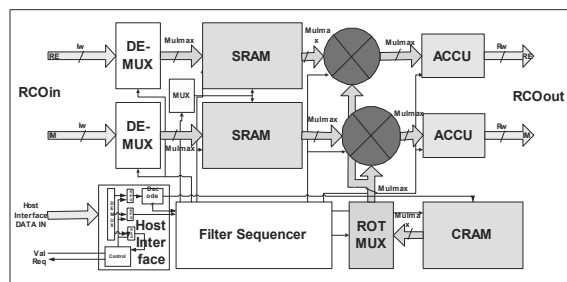


Figure 3.11: RCO-filter – architecture.

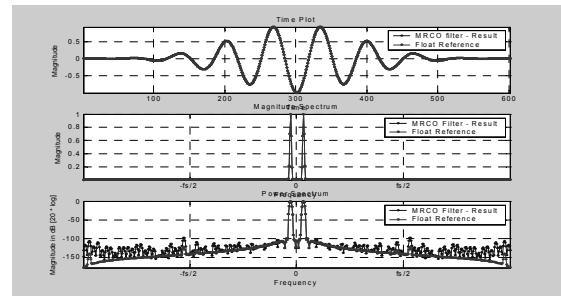


Figure 3.12: RCO-filter results – Bus-width: 18bit.

4. SYSTEM ANALYSIS RESULTS

In the following paragraphs the system bit-true results with real-time measurements are presented. In Figure 4.1 the spectral (magnitude-spectrum), phase (scatter-plot) and timing (eye-plot) characteristic is shown for the up-converter - DUC.

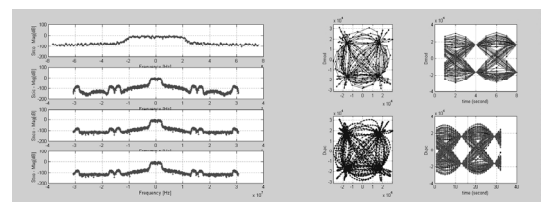


Figure 4.1: DUC-spectral/scatter-/eye-plot

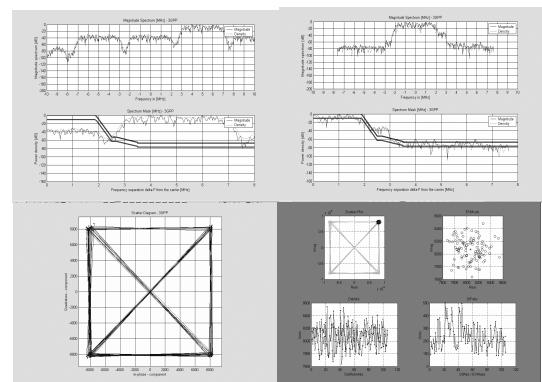


Figure 4.2: DDC-blocking/ EVM-performance.

In Figure 4.2 the down-converter multi-channel performance is shown with a +30dB blocking signal in the adjacent receive- channel The EVM-measurement is used for the overall receiver analysis - see Figure 4.2 (right hand side).

4.1. Design Flow and Methods used

Two designs flows have been used for system simulation and synthesis. The first one is based upon Matlab using an in-house designed bit-true library. Filter sub-designs were generated automatically with a Matlab to VHDL-generation utility – see flow diagrams in Figure 4.3. – or by a SystemC and behavioral-/RTL-synthesis approach, see Figure 4.4.

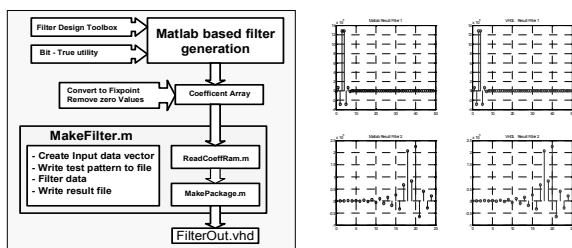


Figure 4.3: Matlab-based filter generation.

In Figure 4.4 the currently implemented design tool chain is shown. After the architectural system model is successfully compiled, timed and scheduled, the Synopsys synthesis tool chain produces the VHDL output. Verification is typically done at several hierarchies from a cycle true validation down to post-synthesis back-annotation and verification of placed and routed designs within the system-model.

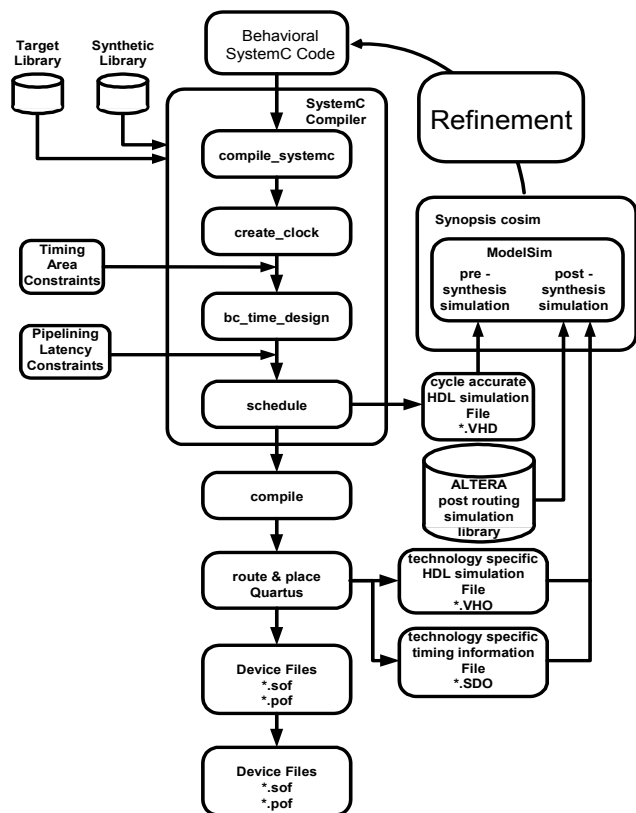


Figure 4.4: Used SystemC- / VHDL- design tool chain.

A comparison of the different design flow results and complexities for the e.g. PFIR-filter processor is shown in Figure 4.5.

	SystemC [LE]	VHDL [LE]
DeMUX	25	36
Mux	1	9
SampleRAM	133	123
CoeffRAM	120	111
PathRotMux	38	32
MULParray	182	132
ACCU	103	81
Filter Sequencer	78	40
Filter Processor	724	578
f_{max} CLK [MHz]	38.98	44.53

Figure 4.5: Example: VHDL / SystemC synthesis results.

5. DSP/FPGA-BASED EMBEDDED-SYSTEM

The VLSI-emulator architecture is shown in Figure 5.1.

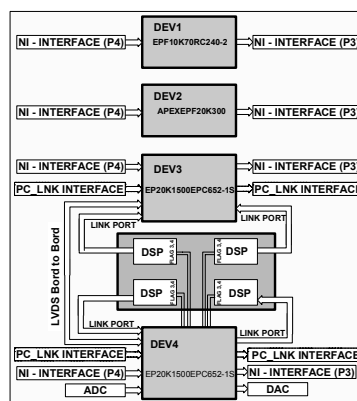


Figure 5.1: VLSI-emulator - architecture.

The main computational burden is covered by a complex FPGA-array – here 2 x Apex-1500 – used for all hardware acceleration tasks. The FPGA-modules are able to communicate either over 1 Gbit/s links (LVDS) or over an interconnected array of floating point digital signal processors – FP-DSPs (4-8 nodes). The data rate of the interconnection network ranges from several kbit/s up to 4 Gbit/s maximum

A photograph with a block diagram of the final VLSI-prototyping system PASS (*Programmable Array System Simulator*) is presented in Figure 5.2.



Figure 5.2: PASS : Prog.-Array-System-Simulator.

For the overall design at an average data path bus width of 16-20 bit a complexity of 25340 LEs (logic elements) (48%) and 299100 RAM- block bits (67%) was required.

6. ACKNOWLEDGEMENT

The work presented in this paper has been supported by the SoC-MOBINET project (IST-2000-30094), an EC funded project. We would like to thank Synopsys for providing synthesis tools through their distinguished university program.

7. CONCLUSION

This work presents the prototyping of a complex DSP-/FPGA-based design in the case of a software definable channel-processing unit. The proposed system includes new architectural concepts for flexible data path routing with the re-programmability of the individual filter stages. The design supports extended multiple operation requirements. The system was pre- and post- analyzed throughout the design flow and verified on a real-time parallel processing test-bed. An efficient design tool chain including optimized hardware generation utilities in MatLab / SystemC were developed and successfully validated throughout the design process.

REFERENCES

- [1] A.Blaickner, H.Grünbacher, "On Re-configurable Methods and Gate Array Based Solutions of Fast Forward Error Correction Systems for Software Radio and Settop-Box Appl.", Proc. Icce 2000, IEEE.
- [2] A.Blaickner, O.Nagy, H.Grünbacher, "Fast Carrier and Phase Synchronization Units for Digital Receivers Based on Re-configurable Logic", 10th int. conference FPL 2000, Springer.
- [3] S.A.Fechtel, A.Blaickner, Efficient FFT and Equalizer Implementation for OFDM Receivers, Proc. Icce 1999, IEEE.
- [4] L.Lundheim and T. A.Ramstad, "An Efficient and Flexible Structure for Decimation and Sample Rate Adaptation in Software Radio Receivers", Proc. ACTS Mobile Comm. Summit, June 1999.
- [5] Henry T. Nicholas III, Henry Samuelli, Bruce Kim, "The Optimization of Direct Digital Frequency Synthesizer Performance in the Presence of Finite Word Length Effects", 42nd Annual Frequency Control Symposium, 1988.
- [6] Bar-Giora Goldberg, "Digital Frequency Synthesis Demystified", pp. 256-259.
- [7] B.H. Hutchison, Jr., "Frequency Synthesis and Applications", IEEE Press, 1975.
- [8] Frederic J. Harris, "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform", IEEE Press, January 1978.
- [9] S. Haykin, "Adaptive Filter Theory", 3rd Ed., Prentice Hall '96.
- [10] Heinrich Meyr, Marc Moeneclaey, Stefan Fechtel, "Digital Communication Receivers", Wiley '97.
- [11] J.G. Proakis, "Digital Communications", 2nd Ed., McGraw-Hill, '89.
- [12] R. E. Crochiere and L. R. Rabiner, "Multirate Digital Signal Processing", '83.

- [13] M. Cummings and S. Haruyama, "FPGA in the Software Radio", IEEE Com., Feb. '99.
- [14] Seunghyeon Nahm, Kyungtae Han, Wonyong Sung, "A CORDIC Based Digital Quadrature Mixer: comparison with a ROM-Based Architecture", IEEE.
- [15] A. Blaickner, H. Grünbacher, "Fast FPGA based Adaptive FIR-Filters for Channel Equalization in Programmable Software Receivers and Cable Modems", AustroChip 2000.
- [16] J. Duprat and J.-M. Muller, "The CORDIC algorithm: New results for fast VLSI implementation", IEEE Transactions on Computers, vol. 42, pp. 168 – 178, February 1993.
- [17] T. Turletti and D. Tennenhouse, "Complexity of a Software GSM Base Station", IEEE Com, '99.

BIOGRAPHIES



Alfred Blaickner, Dr., was born in Salzburg, Austria, in 1958. His research activities started in 1986 within the Department of Communications at Graz University of Technology and the European Space Agency. In 1989 he joined Rohde & Schwarz, Germany. In 1995 he received his Ph.D. degree from Graz University of Technology. He is currently teaching courses in communications engineering, system modeling and signal processing. His research interests include digital communications, signal processing, and VLSI-system design. He is member of IEEE.



Martin Bacher, was born in Bruneck, Italy, in 1972. He received his Dipl.-Ing. degree from the Technical University Graz in 1996. Since 1996 he is with Infineon Technologies in Villach, Austria. His interests are on hardware architectures and algorithms for telecommunications systems with a focus on OFDM and W-CDMA.



Hermann Sterner Dipl. Ing. (FH), was born in Zeltweg, Austria, in 1960. After working several years as software engineer in the industry, he starts study electronics at Carinthia Tech Institute, Austria and received his Masters degree in 1991. He is currently working as project engineer at Carinthia Tech Institute. His interests are, in digital communication systems, signal processing and VLSI design.



Liu Shih-Fu, was born in Taipei, Taiwan, in 1980 and is studying at Carinthia Tech Institute in Villach, Austria. He is currently doing his internship and master thesis at CTI - department of communications. His interests are digital signal processing, telecommunication systems and VLSI.