LOW-POWER, LOW-COST SOFTWARE DEFINED RADIO AND ITS APPLICATIONS

Xiaodong Zhang, General Processor Technologies, Beijing, China, xdzhang@hxgpt.com
John Glossner, General Processor Technologies, Tarrytown, NY, glossner@hxgpt.com

ABSTRACT

Currently, many Software Defined Radio (SDR) products in China focus on research and prototyping of communications systems. However, when mass production is required, the practical design and codes should be optimized to fit into new platforms, e.g. ASICs. Such a development flow requires significant investment and time to enter into the market. In this paper, we introduce China-based production environments of the Sandbridge Sandblaster SB3500 chip and system. It is a heterogeneous SDR platform for wireless communications. The platform consists of heterogeneous radio hardware programmed using mainstream high-level C language tools. The main features include: 1) unified source programming composed of host CPU and kernel DSP codes, 2) flexible and powerful instruction set architecture optimized for digital-communications, 3) unified address space between multiple DSP and CPU cores, 4) unified profiling across heterogeneous cores for functional and timing verification using a system simulator, 5) micro-architectural support for instruction-level, data-level and thread-level parallelism, and 6) extremely low-power interleaved hardware multithreaded implementation. The SB3500 SDR platform has been used in research, prototyping, and most recently in China-based production systems. The software programming model for product development has reduced the typical time to market by more than six months. To-date, many types of custom chips and terminals have been designed for the China market including GPS, PDT (Police digital terminal), LTE, BPLC (Broadband power line communication), and NB-IOT, LORA, Radar and even embedded AI (Artificial Intelligent) chips.

1. INTRODUCTION

In recent years, some important trends have emerged in the design and production of custom chips for dedicated communications, localization/positioning and AI recognition applications, especially with the introduction of wide-area IoT (Internet of Things) networks. The motivation behind such trends usually lies in the fact that custom chipsets will reduce the size of user equipment, significantly lower the overall power consumption and in addition, minimize the total cost for mass production. As a consequence, such a solution will become more and more competitive once the market volume gets large enough.

Unfortunately, most applications do not have enough volume to support a custom ASIC. Hence if each of them requires a customized chip design, there will be little possibility to deliver cost effective products. Instead, a different way should be followed for such cases to provide low-cost chips accordingly; that is, the well-known Software Defined Radio (SDR) solution.

In practice, if SDR is considered for implementation, there are many conditions that need to be taken into account, i.e. small development team, for example, less than 10 engineers; short time to market and limited capital investment. As a feasible and competitive candidate, the Sandbridge Sandblaster SDR platform is able to meet such strict requirements simultaneously. In fact, with the Sandblaster solution, many types of dedicated chips, terminals and devices have been designed for the China market including GPS/Beidou, PDT (Police digital terminal), LTE, BPLC (Broadband power line communication), NB-IOT, LORA, Radar and even embedded AI specific chips that are already delivered in different volumes to the customers.

In Section 2 we describe the Sandblaster SB3500 SDR platform. Section 3 introduces the parallel programming development methodology. Section 4 outlines some applications cases designed with the SB3500 and finally in Section 5, we summarize and draw conclusions for this paper.

2. HETEROGENEOUS SDR PLATFORM

Figure 1 shows a chip diagram of the Sandbridge Sandblaster SB3500 chips [3] . The chip includes three DSP cores and one CPU core integrated together. The cores are interconnected with a high-speed ring network. The original application market for SB3500 was commercial wireless handsets. Therefore, the peripheral interfaces are very complete for many interesting applications and include an LCD display, camera, DigRF, GPIO, SPI, I2S, I2C, UART,

USB 2.0, etc., which are connected to the internal CPU and DSP cores via ARM AMBA buses.

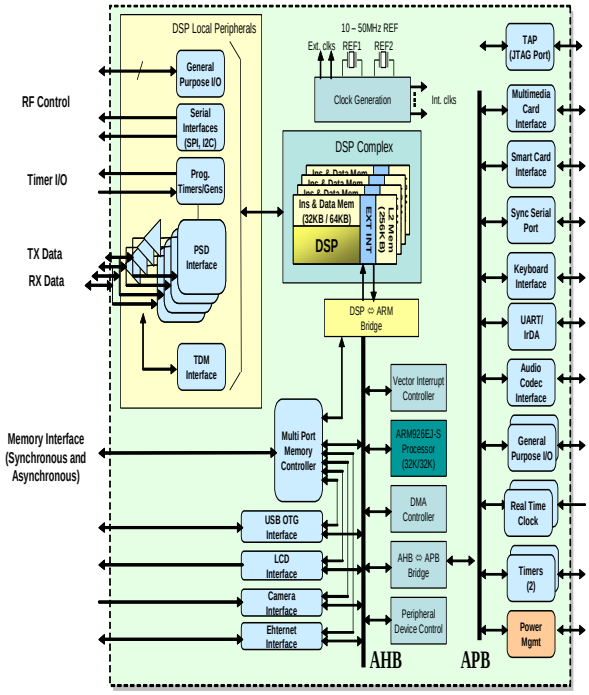

Figure 1. Sandblaster SB3011 Chip

Technology	65nm
Processor Clock	600MHz
Power Dissipation	75mW @ 1V, 25C
On-chip Memory	1.5Mbytes
Peak DSP performance	9.6 GMACs

Table 1. Key Sandblaster Parameters (per core)

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With SB3500 chips and appropriate RFICs, we have designed different development boards according to different applications' requirements. However, to make sure the final delivered products is the most competitive and cost effective for mass production, it is preferred that the integrated RFIC and analog convertors are available commercially. For example, for broadband wireless modem development, the RFICs that have been adopted for 3GPP terminals should be used.

Figure 2 and Figure 3 show the SDR development boards being supplied to developers. Usually they are further separated into their composite series, i.e. the digital core board, the RF/analog board and the digital loopback test board, etc. That is, for generic wireless communications, we present a commonly used development board that is comprised of a digital core and a broadband RF/analog board. But for low-power IoT developments, the wideband RF board must be replaced with appropriate ones for different bandwidths and different radio frequencies. In particular, its sleep mode power management strategy must be carefully optimized for longer battery operation, which is always specified by certain publicly released standard documents. For example, for China Mobile operated NB-IoT terminals, the maximum power consumption that cannot be exceeded for the sleep mode is about 3-5uw in practice.

(a) Generic broadband board

(b) IoT board

Figure 2. SDR development boards for generic wireless communications and IoT

(a) SB3500

(b) Digital core board

(c) RF/Analog board

(d) Digital loopback test board

Figure 3. The SB3500 chip and the associated digital, RF/analog and loopback test boards

With low-cost production in mind, a formal design flow has been established for SB3500 chips, which consists of three stages: 1) fixed-valued algorithm simulation using the SB3500 simulator, 2) prototyping with the SDR board and small-scale field trials, and 3) multi-chip packaging for mass production. These stages are classified as ***Simulator-level***, ***Board-level*** and ***Package-level development stages***, which are illustrated in figure 4. For the algorithm programming and system trials that are encountered in the first and second stages, we encourage our users to use generic development boards and their associated simulation tools, which are already available worldwide. With these boards user coded programs can be profiled and optimized conveniently and quickly to meet real-time requirements. In our experience, the human resource needed for the

development of a GPS-like receiver usually requires 3-5 man-months of effort. Compared to classical hardware design this is a very small investment. In addition, even for small-scale field trials, the number of SDR boards required for system testing is very limited and their price is rarely a concern for most users. As a result, the generic SDR boards will always accelerate the development of most applications, such as the signal processing we apply to communication systems.

Once a design enters into mass production, the development then goes into its third stage, where the packaging of multiple chips starts to become an emphasis. Usually the motivation for this lies in cost reduction and yield improvements of the final products. To achieve such goals, we often use either SIP (System in Package) or MCM based packaging technologies. In reality, most Chinese customers prefer to follow this design methodology because compared to conventional board-level integration such a solution has become more and more competitive in their respective markets. As an example, we have shown a SIP packaged SB3502 with one SB3500 and two AFE dies placed inside in figure 5.

As a result, when SB3500 based packaged chips are used in terminals, our clients are able to directly compete with many mainstream chip vendors in the market, whether in the early low-volume sails or later mass productions.

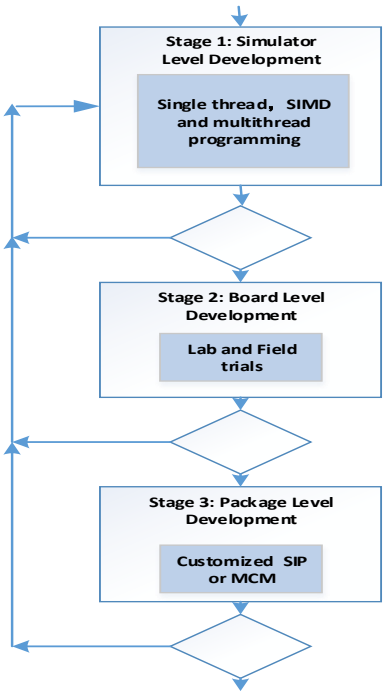

Figure 4. Product Development Flow

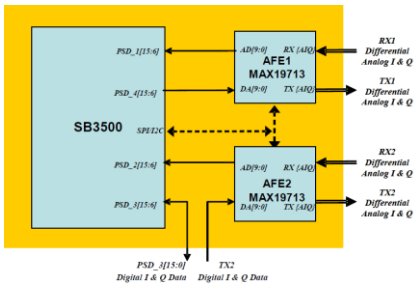

Figure 5. SIP of SB3502 with SB3500 and AFE dies

To-date we have experience with a considerable number of SDR projects using the Sandbridge SB3500 chips. In addition to simplified technology development, providing technical support developers is important. To help our users in the China market we have developed a special website with many design examples, libraries, on-line discussion zones as well as real-time video conference systems, which are shown in figure 6. It is open to anyone requiring technical support at the website www.sdrerc.com.

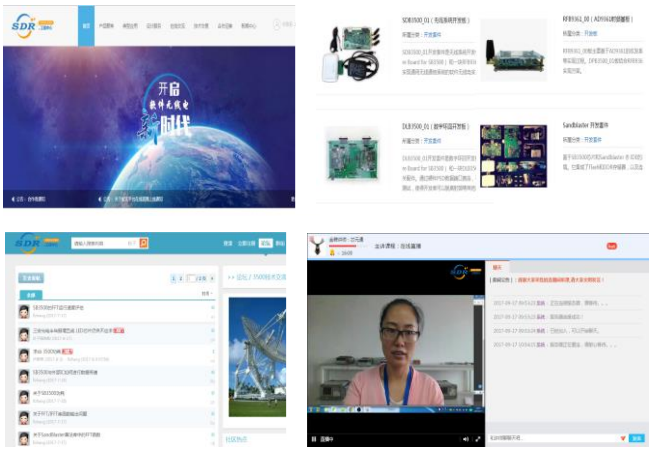

Figure 6. The SDR website (www.sdrerc.com)

3. PARALLEL DEVELOPMENT FLOW

We have developed a tool-chain based on Sandbridge Technologies' tool chain to facilitate the development of SDR applications on the Sandblaster Platform [3] . The software tool chain is primarily dedicated towards generating and simulating efficient code for the Sandblaster processor. The basic philosophy behind the tools is that the user should program in a higher-level language such as C and not need to use any assembly language code. The tool chain consists of an Integrated Development Environment, ANSI C compiler, functional simulator, and a real time operating system.

Figure 7 shows the Integrated Development Environment (IDE). It provides an easy to use graphical user interface to all the software tools. The IDE is based on the open source eclipse integrated development environment [3] . The IDE is the graphical front end to the C compiler, assembler, simulator and the debugger. The IDE provides the ability to create, edit, build, execute and debug an application. In addition, it provides the ability to mount a file system, access CVS, access the web and communicate with the Sandblaster hardware board.

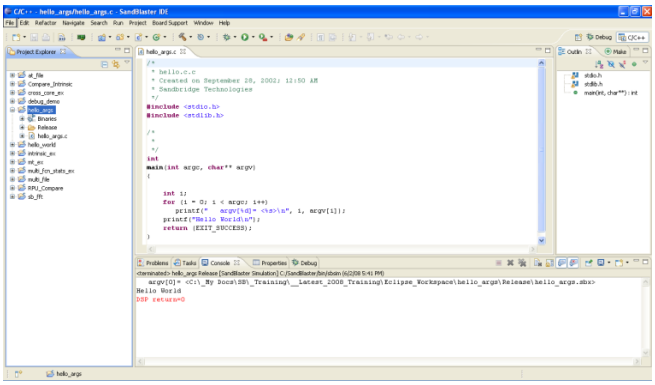

Figure 7. The Sandbridge IDE

The software tool set also consists of an optimizing ANSI C compiler. This C compiler performs many high performance optimizations, including the generation of saturation instructions from out of the box C code. This obviates the need to write assembly language code or to use machine specific intrinsics for saturation code. The compiler has proprietary semantic analysis techniques, which eliminate the need for intrinsics. A programmer writes C code in a processor independent manner and the compiler converts the C code into a dependence flow graph, analyzes the range of the arithmetic operations (specifically the sign bit) in the emulation code, propagates it across code segments, determines if it is a saturating or non-saturating operation and emits the correct assembly code.

Another important technique used by the compiler is the exploitation of SIMD instructions. The Sandbridge architecture uses SIMD instructions to implement vector operations. The compiler performs high performance inner and outer loop vector optimizations that use SIMD instructions to exploit the data level parallelism inherent in signal processing applications. These optimizations include vector load, store and multiply-add-reduce-saturate. In conjunction with loop optimizations, these provide very efficient and tight loops that can provide as many as 16 RISC operations in a single cycle.

Sandbridge has also developed an ultra-fast cycle counting accurate simulator, which improves the programmer productivity. The simulator uses architecture description of the underlying DSP and provides close to accurate cycle counts, but does not model the external memories or peripherals. However, the information provided by it is sufficient to develop the first executable version of an application. The simulator is based on Just-in-Time code generation technology, which has been developed in house.

The tool set also consists of an operating system kernel which provides access to the resources (multiple threads, peripherals, memories etc.) on the processor. This is provided via POSIX threads interface. Keeping with the philosophy of having a standard, user-friendly and efficient programming model, this interface is based on ANSI C and is commonly used in multi-threaded/multi-processor environment.

3.1 Serial to Parallel Code Development

Most users start programming algorithms using serial C code since parallel multithreaded coding can be complicated. This provides quick development but is not performance optimized.

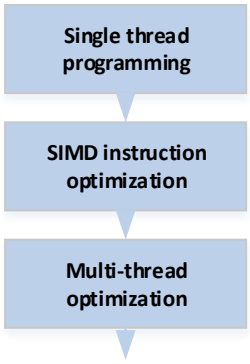

Figure 8. The development from serial to parallel codes

Figure 8 shows a serial to parallel code development flow which significantly lowers the threshold of parallel coding of programs. Using this development flow, users can start from their familiar serial code, and then gradually convert their algorithms into high performance parallel codes. The first optimization is the use of VLIW instructions. Instruction-level parallel operations are performed within each clock cycle. The second parallelization step is the use of intrinsic functions to execute SB3500 data-level SIMD operations. The third step is to transform the code to multithreaded code. The hardware has multiple threads that accelerate multithreaded software. However, to balance the processing workloads between successive threads, the users have to profile and balance the execution cycles and latencies between them, whether it is within a single core or across multiple cores.

3.2 Heterogeneous System Computing

As a further enhancement, the SB3500 also provides a heterogeneous computing environment composed of DSP and CPU cores with one ARM CPU and three SBX DSP cores inside its die. To aggregate all the computing capabilities, Sandbridge provides a hardware architecture and software tools optimized for heterogeneous computing. A single unified address space between all processors is provided along with a high-level C language compiler to program user code, and concurrent profiling and computing engines to optimize upper-layer applications, etc. In fact, this solution has already benefited most clients since it makes user-level programming much easier and shortens the time to market dramatically.

4. APPLICATIONS CASES

In this section, we present four application that are implemented by our clients in China: 1) LTE modem, 2) China Mobile operated IoT devices, 3) high-precision GPS/BD positioning terminals, and 4) China Grid sponsored BPLC terminals and 5) the video recognition CNN terminals.

4.1. Custom 3GPP LTE modems

Figure 9 shows a well-known 3GPP LTE modem. It can be extended in different special-purpose wideband wireless modems such as real-time image transmissions used for UAV communication systems.

Figure 9. LTE module used in UAV

4.2. Narrow-band IoT devices

A new series of wide-area narrow-band IoT systems have been introduced into the 3GPP standards. Their associated communications, operations, devices, and several types of applications have emerged as a new wave of industrial products that are comparable to or even greater than the scale of the currently deployed 4G systems.

To meet these system requirements imposed by IoT applications, we have collaborated with distinguished Chinese companies to offer high-quality, low-cost NB-IoT terminal chips. These chips enable multimode communications, satellite positioning and artificial intelligence algorithms to execute simultaneously.

Figure 10. Prototype of NB-IoT terminal

4.3. GPS/BD positioning devices

GPS positioning functionality has become one of the most important services for smart terminals. However, to offer high-precision positioning information to Chinese clients we usually have two choice – one based on the world-wide GPS or the quickly expanding BD system. Consequently, we have developed code optimized for both GPS and BD receivers inside relevant SDR terminals for our clients.

Figure 11. Dual mode GPS/BD module

4.4. BPLC driven by China Grid

China Grid has launched an aggressive plan in China on energy Internet, to significantly promote their services to nation-wide industries and end users. However, to support such a project, the last-mile accesses from all devices as well as power meters must be guaranteed. Otherwise large portions of the grid could eventually fail. Hence China Grid released its latest broadband power line commutation (BPLC) standards in 2016 and later in this year, 2017, some promising BPLC chips emerged in the Chinese markets. Among them, the SDR based solutions have outperformed most of their competitors so far. In the following figure, we present some of the representative BPLC products that are developed using SB3500 chips that are scheduled to enter mass production in 2018.

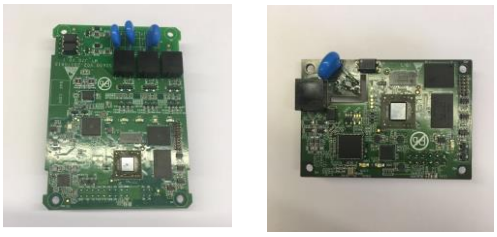

Figure 12. BPLC modules

4.5. Embedded AI accelerator

Recently, artificial intelligence services have shown promise in many IoT applications. In order to lower power consumption for radio transmissions as well as to minimize data throughput transferred from IoT terminals, we suggest that some embedded AI acceleration codes should be coupled closely with satellite positioning, wireless and wireline communication libraries that are present in typical IoT terminals. Using SB3500 DSP cores, our partners have developed their own AI SDK and its associated libraries. For example, the well-known CNN and RNN codes will be available for video and voice detection over SDR terminals. Below is an SDR development environment that is used for CNN acceleration purposes. It is scheduled to be released to the public in the first half of 2018.

Figure 13. DEMO of embedded AI

5. CONCLUSIONS

In this paper, we have introduced a sophisticated SDR solution, the Sandblaster Sandbridge platform and analyzed its basic features. First, the Sandbridge SB3500 chips can be used for designs from the initial prototyping to the final mass production at competitive unit costs. Second, with the powerful heterogeneous computing architecture and a cycle-accurate simulator, users can easily develop and optimize their codes with a small team. Third, many types of reference designs have been released and mature products developed with the SB3500 are available including SIP/MCM packaged chips to small-size terminal modules. Finally, to support product developers, a specific SDR website for the public was developed proving technical support for all users of SB3500 chips.

6. REFERENCES

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