Porting of an FPGA Based High Data Rate DVB-S2 Modulator

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SDR’11 WInnComm

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Outline

- High Data Rate DVB-S2
  - Waveform Description
  - BDR-1 and the Porting Effort
  - Over-the-Air Testing
  - Conclusion
The High Data Rate DVB-S2 Waveform

- **DVB-S2 is the second generation digital video broadcasting standard** from the ETSI (European Standard Telecommunications Series)
  - **Flexible input stream** adapter, suitable for operation with single and multiple input streams of various formats (packetized or continuous)
  - **Powerful FEC** system based on LDPC (Low-Density Parity Check) codes concatenated with BCH codes, operating 0.7 – 1 dB dB from the Shannon limit
  - **Wide range of code rates** (from 1/4 up to 9/10); allows “tunable” power- and spectral-efficiency
  - **Broad industry base** with successful commercially, available, implementations which support data rates up to ~50 Msymbols/s
- **HDR DVB-S2 Implementation** supports a subset of the standard at much higher symbol rates
  - QPSK, 8PSK
  - 1 to 280 Msymbols/s
HDR Waveform Modes and Rates

HDR Waveform Capacity

Data Rate, Mbps vs. Mega Symbols per Second (Mbaud)

- QPSK 1/2  ΔSNR = 0
- QPSK 2/3  ΔSNR = 2.1
- QPSK 3/4  ΔSNR = 3.0
- 8-PSK 2/3  ΔSNR = 5.5
- 8-PSK 3/4  ΔSNR = 6.9
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**HDR Modulator Architecture**

- **Single FPGA solution**: 77% of Virtex 5 SX95T
- **Consumes < 40 Watts at full rate**
  - Includes: Gigabit Ethernet, FPGA, and high-speed DAC
- **Dual SRRC real filters on I and Q channels**
  - Supports rate matching from 1 to 280 Msps, in $2^{32}-1$ steps
- **Direct digital synthesis of L-band IF**
- **Architecture independent FEC Encoder pending**

Extensive capabilities, leveraging modern technology to deliver a portable SWaP-compliant system
External Interfacing

• To enable easier porting the waveform interfaces are generalized
  – System interface
    Clocks, resets, etc.
  – Host interface
  – Data interface
    Input data, DAC signals

• The original development platform design is provided as an example to the porting team

• Porting team is required to develop Gaskets to bridge between their hardware platform and the waveform module
Modulator FPGA Sizing

- The modulator components were successfully targeted to various FPGAs ranging from a Virtex 5 SX240T to a Virtex II Pro 100
- The Virtex 5 SX240T resource utilization is as follows:

<table>
<thead>
<tr>
<th>Module Name and Path</th>
<th>Registers</th>
<th>6-input LUTs</th>
<th>BRAM (32kb)</th>
<th>DSP48s</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx Core, direct conversion DAC, Xilinx FEC</td>
<td>21k</td>
<td>20k</td>
<td>111</td>
<td>20</td>
</tr>
<tr>
<td>/modules/tx_core</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tx Core, direct conversion DAC, AHA FEC</td>
<td>38k</td>
<td>39k</td>
<td>225</td>
<td>16</td>
</tr>
<tr>
<td>/modules/tx_core</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tx Core, I/Q DAC, Xilinx FEC</td>
<td>20k</td>
<td>19k</td>
<td>92</td>
<td>4</td>
</tr>
<tr>
<td>/modules/tx_core_no_cm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tx Core, I/Q DAC, AHA FEC</td>
<td>37k</td>
<td>38k</td>
<td>209</td>
<td>0</td>
</tr>
<tr>
<td>/modules/tx_core_no_cm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Multiple versions, using the same code base, to support a wide variety of possible platforms.
Waveform Implementations of the High Data Rate Modulator

- MIT LL Developer Board
- MIT LL Prototype Board
- Annapolis COTS HW
- Bittware COTS HW Altera Chipset
- Future Operational Specific Modem
- MITRE
- NRL BDR-1
- Multiple Small Form Factor Boards

Capability Relative to Operational Terminal

Suitability for Operational Platform

Successful Ports
Future Migration
WaCoM Software Stack

This illustrates how the WaCoM library is typically situated with respect to other software layers.

The user application (or GUI/CLI) relies on the WaCoM library which in turn relies on the user-supplied platform-specific driver implementation.

The “driver” either communicates directly with the hardware, or indirectly through additional software or operating system layers.

WaCoM is a layered approach which aims for maximum software reuse.
WaCoM Library

Abstracts and encapsulates the software/hardware interface

- C++ library that provides a modulator controller object
- Programmer does not require knowledge of modulator internals
- Below is a simplified example of setting the center frequency

**Instead of this:**

```cpp
// Disable everything
prev = ReadReg32(ENABLES_REG);
WriteReg32(ENABLES_REG, 0x0);

// Write center frequency register
center = ReadReg32(CENTER_FREQ_REG);
center &= 0xffff0000;
center |= freq * multiplier;
WriteReg32(CENTER_FREQ_REG, center);

// Restore previous state
WriteReg32(ENABLES_REG, prev);
```

**WaCoM library allows this:**

```cpp
// Set center frequency
controller.setCenterFrequency(freq);
```
User Interface

• WaCoM library contains no UI code

• Reusable GUI and CLI exist
  – Designed to be used with WaCoM library
  – Usually require adaptation for platform-specifics
    Loading FPGA images
    Connecting to modem
e.g. over a network
  – Can be used as example code or as starting point
# Waveform Artifacts

## Waveform Description

### Description
- **Waveform Functional Specification**
- **Waveform Design Specification**
- **Waveform Development Environment**
  - Waveform-Development-Environment_25Jan11_Rel1.pdf

### Models
- **C++ Model**
  - Waveform_Model-C++_25Jan11_Rel1.zip
- **Mathworks Model**
  - Waveform_Model-Mathworks_25Jan11_Rel1.zip
- **Modulator Model Overview**
  - Modulator-Model-Overview_HY-JH_25Jan11_Rel1.pdf

## Waveform Implementation

### VHDL/HW
- **VHDL**
  - Waveform_VHDL_25Jan11_Rel1.tar.gz
- **VHDL Modulator Firmware Description**
  - VHDL-Modulator-Firmware-Description_25Jan11_Rel1.pdf
- **VHDL Modulator Implementation Quick Start**
  - VHDL-Modulator-Implementation-QuickRef_CKT_25Jan11_Rel1.pdf
- **Modulator Example Implementation**
  - Modulator-Example-Implementation_CKT_25Jan11_Rel1.pdf

### HW/SW Interface
- **Modulator Hardware-Software Interface Spec**
  - Modulator-Hardware-Software-Interface-Spec_25Jan11_Rel1.pdf
- **Modulator Hardware-Software Interface Quick Start**
  - Modulator-Hardware-Software-Interface-QuickRef_CKT_25Jan11_Rel1.pdf
- **Open Core Protocol (OCP) Profiles**
  - Open-Core-Protocol-Profiles_CKT_25Jan11_Rel1.pdf

## Waveform Test

### Test & Support [11010]
- **Test Vectors**
  - Included in Waveform_VHDL_25Jan11_Rel1.tar.gz
- **Modulator Test Plan**
  - Modulator-Test-Plan_25Jan11_Rel1.pdf
- **Laboratory Test Platforms**
  - Laboratory-Test-Platforms_JTD_25Jan11_Rel1.pdf
- **Release and Support Plan**
  - Release-and-Support-Plan_TAB_25Jan11_Rel1.pdf

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It takes more than just good coding to make a waveform portable.
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• BDR-1 and the Porting Effort
• Over-the-Air Testing
• Conclusion
NRL’s Basic Digital Radio

<table>
<thead>
<tr>
<th>FPGAs</th>
<th>2 Virtex 5 SX50T</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth</td>
<td>~300 MHz</td>
</tr>
<tr>
<td>Sample Rate</td>
<td>1.75 GHz</td>
</tr>
<tr>
<td>Supported Waveforms</td>
<td>• NRL Test WF</td>
</tr>
<tr>
<td></td>
<td>• HDR DVB-S2 Mod.</td>
</tr>
<tr>
<td>Dimensions</td>
<td>4”x7”</td>
</tr>
</tbody>
</table>

- Small form factor SDR platform
- Low jitter VCOs for precision signal sampling/generation
- Preexisting GigE control and data plane, with drivers
- Direct L-band output eliminates need for analog additional up/down conversion stages
HDR DVB-S2 Port to the BDR-1 Step 1

- Ascertain the control structure of the BDR-1 platform
- Identify the FPGA specific components required for operation
- Identify the components not required for operation

It is easier to reuse platform specific modules.
HDR DVB-S2 Port to the BDR-1 Step 1

- Ascertain the control structure of the BDR-1 platform
- Identify the FPGA specific components required for operation
- Identify the components not required for operation

It is easier to reuse platform specific modules.
HDR DVB-S2 Port to the BDR-1 Step 2

- Create *Gaskets* to bridge the gap between FPGA specific components and the new waveform modules.
- Generate software drivers to interface with the new platform.

Gaskets reduce configuration management issues by not changing the platform specific and or waveform specific features during a porting effort.
• Insert waveform functionality between the gaskets
• Connect the software with the new driver

The modulator core VHDL was not modified to support the BDR-1 platform. All new code was limited to the gaskets.
Porting Results

- 1st Successful port of HDR DVB-S2 modulator
- BDR-1 FPGA is ~1/2 the size of original development FPGA
- Demonstrated compatibility with multiple commercial DVB-S2 modems (Newtec, ECC’s HIBEAM, Avtec’s HDRM, etc.)

<table>
<thead>
<tr>
<th>Modem</th>
<th>Symbol Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Newtec AZ410</td>
<td>45 Msym/s</td>
</tr>
<tr>
<td>HIBEAM Phase 1</td>
<td>50 Msym/s</td>
</tr>
<tr>
<td>HIBEAM Phase 2</td>
<td>200 Msym/s</td>
</tr>
<tr>
<td>HDRM</td>
<td>218 Msym/s</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Platform</th>
<th>BDR-1</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Registers</td>
<td>26k</td>
<td>21k</td>
</tr>
<tr>
<td>LUTs</td>
<td>22k</td>
<td>20k</td>
</tr>
<tr>
<td>BRAMs</td>
<td>122</td>
<td>111</td>
</tr>
<tr>
<td>DSP48s</td>
<td>20</td>
<td>20</td>
</tr>
</tbody>
</table>
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Over the Air Demonstrations of the BDR-1

- During the weeks of June 6, 2011 & June 13, 2011 the Naval Research Laboratory (NRL) conducted experiments with their Tactical Reach-back Extended Communications (TREC) system.
  - Air to ground line-of-sight (LOS) mobile system
  - Included the use of the HDR DVB-S2 waveform on the BDR-1
  - Used low power small apertures to demonstration 100’s of Mbps over 10’s of nautical miles @ Ka-Band
<table>
<thead>
<tr>
<th>Aircraft</th>
<th>Cessna 210</th>
</tr>
</thead>
<tbody>
<tr>
<td>Antenna</td>
<td>Risley Prism (&lt;6.7” Height &amp; &lt; 5.5 lbs)</td>
</tr>
<tr>
<td>Power Amplifier</td>
<td>0.5 Watts @ 37.0 to 38.5 GHz</td>
</tr>
<tr>
<td>Transceiver</td>
<td>L-band block conversion</td>
</tr>
</tbody>
</table>
| Modems        | BDR-1 (HDR Waveform)  
HI-BEAM Phase 2 (DVB-S2)  
STD-CDL |

- Aircraft altitude for testing was ~15k feet MSL
- UHF LOS used to pass telemetry data for antenna pointing
- Flight path logged via GPS for further analysis
### Ground Terminal

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vehicle</td>
<td>HMWV (stationary)</td>
</tr>
<tr>
<td>Antenna</td>
<td>15” Cassegrain Antenna</td>
</tr>
<tr>
<td>Power Amplifier</td>
<td>0.5 Watts @ 37.0 to 38.5 GHz</td>
</tr>
<tr>
<td>Transceiver</td>
<td>L-band block conversion</td>
</tr>
<tr>
<td>Modems</td>
<td>Newtec AZ410 (DVB-S2) HI-BEAM Phase 2 (DVB-S2) STD-CDL</td>
</tr>
</tbody>
</table>

- Ground terminal was stationary for the testing
- UHF LOS used to pass telemetry data for antenna pointing
- Instrumented to collect data from the modems and GPS
Over-the-Air Test 1 10 June 2011

• BDR-1 in the air, Newtec Azimuth on the ground
  • Modulation settings:
    • 45 Mbaud, 101 Mbps, 8PSK, ¾
    • PRBS enabled
    • Pilots off
  • Downlink: 37.1 GHz, Uplink: 38.0 GHz

• Atmospheric conditions
  • Temperature 93 degrees F
  • Humidity 30 %
Map of $E_b/N_0$ Recorded during Test 1

*This slant range listed in the legend is the longest slant range at which the EbNo recorded was great enough to demodulate Quasi Error Free (QEF)*
*Note this was the final test of the day and on the inbound leg the aircraft was descending in preparation to land
Over-the-Air Test 2 14 June 2011

• BDR-1 in the air, ECC P2 HIBEAM modem on the ground
  • Modulation settings:
    • 134 Mbaud, 300 Mbps, 8PSK, \( \frac{3}{4} \)
    • PRBS enabled
  • Pilots on
  • Downlink: 37.1 GHz, Uplink: 38.0 GHz

• Atmospheric conditions
  • Temperature 75 degrees F
  • Humidity 38 %
Map of $E_b/N_0$ Recorded during Test 2

*This slant range listed in the legend is the longest slant range at which the EbNo recorded was great enough to demodulate Quasi Error Free (QEF)*
$E_b/N_0$ Recorded vs Range during Test 2
Over-the-Air Test 3 14 June 2011

• BDR-1 in the air, ECC P2 HIBEAM modem on the ground
  • Modulation settings:
    • 200 Mbaud, 540 Mbps, 8PSK, 9/10
    • PRBS enabled
  • Pilots on
    • Downlink: 37.1 GHz, Uplink: 38.0 GHz

• Atmospheric conditions
  • Temperature 75 degrees F
  • Humidity 38 %
Map of EbNo Recorded during Test 3

*This slant range listed in the legend is the longest slant range at which the EbNo recorded was great enough to demodulate Quasi Error Free (QEF)
$E_b/N_0$ Recorded vs Range during Test 3
### Over the Air Testing Results

<table>
<thead>
<tr>
<th>Mode</th>
<th>Symbol Rate (Mbaud)</th>
<th>Data Rate (Mbps)</th>
<th>Slant Range (nmi)*</th>
<th>Receiver</th>
</tr>
</thead>
<tbody>
<tr>
<td>8PSK, 3/4</td>
<td>45</td>
<td>101</td>
<td>35</td>
<td>Newtec AZ410</td>
</tr>
<tr>
<td>8PSK, 3/4</td>
<td>134</td>
<td>300</td>
<td>30</td>
<td>HI-BEAM P2</td>
</tr>
<tr>
<td>8PSK, 9/10</td>
<td>200</td>
<td>540</td>
<td>22</td>
<td>HI-BEAM P2</td>
</tr>
</tbody>
</table>

*This value corresponds to the furthest distance at which continuous communications were maintained.*
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Conclusion
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• The porting effort was straightforward and successful
  – Less than a one man month for VHDL port
• There was a high level of software reuse
• Line of sight testing showed robustness of the modulator design and platform
• Interoperability of the waveform demonstrated the level of maturity of the DVB-S2 standard in industry