Software Defined Radio Needs

- **High-Performance Signal Processing**
  - DSP: filtering, FFTs, custom DDC/DUC, modulation, demodulation, etc.
  - Coding: Viterbi, trellis, turbo, space time, convolutional, etc.
  - Beamforming: diversity combining, direction finding, antenna steering, etc.

- **Fast Interfaces**
  - Processor I/O and Interprocessor Communication
  - Real-time I/O Peripherals (A/Ds, D/As, codecs, etc)
  - Memory (data buffers, coefficient tables, workspace, etc.)
  - Dedicated ASICs (digital up/down converters, etc.)
  - Networks (Ethernet, SAN, WAN, etc.)
  - Other System Boards (backplanes and switched fabric)

Low-Latency Control Sub-Systems
  - Dehopping, tracking, countermeasures, Doppler processing, etc.

- **Peripheral Interfaces**
  - Wide variety of different electrical levels, standards, and characteristics

- **Timing and Control**
  - Custom synchronization, gating, triggering and timing functions
What is Series-7

June 2010: Xilinx announced Series-7

- **Low cost / low power** (equivalent to Spartan-6)
- **Mid cost and performance**, decent amount of I/O pins (equivalent to medium to large Virtex-6)
- **Max performance / high cost**
  - lots of gigabit serial I/O
  - (more than all previous Virtex-6)
Xilinx Series-7 Target Markets

**ARTIX**
- Portable/handheld ultrasound
- 3D cameras and camcorders
- D-SLR still cameras
- Software defined radio
- 3D TV
- Portable eReaders
- Automotive Infotainment
- Multifunction printers
- Video surveillance

**KINTEX**
- Wireless LTE infrastructure
- 10G PON OLT line card
- LED backlit and 3D video displays
- Video-over-IP bridge
- Cellular radio
- Medical Imaging
- Avionics imaging
- Set top boxes
- Motor control

**VIRTEX**
- RADAR
- ASIC emulation
- High-performance computing
- Test and measurement
- 400G and 100G line cards
- 300G Interlaken bridge
- Terabit switch fabric
- 100G OTN
- MUXPONDER
Comparing Virtex-4, -5, -6, and -7

Virtex FPGAs Available in a 35mm x 35mm BGA Package

- Virtex geometry & power:
  - Virtex-4 = 90nm, Virtex-5 = 65nm, Virtex-6 = 45nm, Virtex-7 = 28nm
  - Virtex-7 – “Half the Power”
    - Various power management techniques from hardware design to software for optimizing IP
DSP48E1 DSP Engine

- 25x18 2’s complement multiplier
- 48-bit accumulator / synchronous up/down counter
- Pre-adder for A & D inputs optimizes symmetrical FIR filters
- SIMD arithmetic unit for dual 24-bit or quad 12-bit operations
- Logic unit handles ten different logical operations
- Pattern detector for convergent or symmetrical rounding
- Pipelining modes for cascade processing

Quantity: 5280 maximum in Virtex-7
Data Converter Interfaces

- Higher signal bandwidths for wideband communications like LTE and UMTS require faster A/D and D/A converters
- Example: National Semi ADC12D1800 - 3.6 GSample/sec, 12 bits
  - Digitizes up to 1.5 GHz instantaneous bandwidth
- Four 12-bit demultiplexed outputs – each 900 MS/sec
  - DDR transfers – 2 transfers on each edge of a 450 MHz clock
- Virtex-7 DDR I/O
  - Up to 1600 MHz transfer rates
  - Per bit skew adjustments align data bits within each word
  - Digitally controlled termination networks eliminate discrete resistors and boost performance
External Memory Interfaces

- For large storage and buffering requirements that exceed block RAM
- DDR3 SDRAMs: Most dense and least expensive memory devices
  - Volume and pricing driven by enormous PC market
  - PCs use processor interfaces and bridge chips for interface
  - Critical timing with complex adaptive training
- Virtex-7 DDR3 SDRAM Controller
  - Direct glue-less connection to DDR3 SDRAMs
  - Operates at up to 1.866 GHz rates per bit
  - For a 32-bit SDRAM = 7.464 GBytes/sec!
  - New 1:4 ratio for fabric-to-memory clock
  - Phaser clock generator maintains real-time clock-to-data timing to within 7 psec!
Gigabit Serial Interfaces

- Three gigabit serial speed versions: GTX, GTH, and GTZ
- Protocol independent: Ethernet, PCIe, Aurora, SRIO, Infiniband, etc.
- Aurora: Xilinx link-layer protocol – ideal for raw data streaming
- Built-in PCIe Interfaces now include endpoints and root ports
- TEMAC – Tri-Mode Ethernet MAC for 10M, 100M and 1G
- GTZ supports 10G, 40G, 100G and 400G Ethernet line cards

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Virtex-7 T</th>
<th>Virtex-7 XT</th>
<th>Virtex-7 HT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak transceiver speed</td>
<td>12.5 Gb/s (GTX)</td>
<td>13.1 Gb/s (GTH)</td>
<td>28.05 Gb/s (GTZ)</td>
</tr>
<tr>
<td>Qty Transceivers</td>
<td>36</td>
<td>96</td>
<td>88</td>
</tr>
<tr>
<td>Peak bi-directional serial bandwidth</td>
<td>0.900 Tb/s</td>
<td>2.515 Tb/s</td>
<td>2.784 Tb/s</td>
</tr>
<tr>
<td>No. PCIe Interfaces</td>
<td>4</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>PCIe Speed</td>
<td>Gen2 x8</td>
<td>Gen3 x8</td>
<td>Gen3 x8</td>
</tr>
</tbody>
</table>
### Relative Comparisons: Virtex-6 and -7

<table>
<thead>
<tr>
<th>Category</th>
<th>Virtex-6</th>
<th>Virtex-7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum DSP48E1 Blocks</td>
<td>2016</td>
<td>5280</td>
</tr>
<tr>
<td>Maximum Gigabit Serial Rate</td>
<td>11.1 GHz</td>
<td>28.1 GHz</td>
</tr>
<tr>
<td>Maximum Logic Cells</td>
<td>759k</td>
<td>1,955k</td>
</tr>
<tr>
<td>Maximum Block RAM</td>
<td>38 Mbits</td>
<td>85 Mbits</td>
</tr>
<tr>
<td>Maximum PCIe Data Rate</td>
<td>4 GB/sec</td>
<td>8 GB/sec</td>
</tr>
<tr>
<td>Max Configurable Logic Blocks</td>
<td>118,500</td>
<td>305,400</td>
</tr>
<tr>
<td>Relative I/O Power</td>
<td>100%</td>
<td>70%</td>
</tr>
<tr>
<td>Relative Dynamic Power</td>
<td>100%</td>
<td>75%</td>
</tr>
<tr>
<td>Relative Maximum Static Power</td>
<td>100%</td>
<td>35%</td>
</tr>
</tbody>
</table>
Virtex-7 Support for OpenVPX SDR

- All critical resources for a complete OpenVPX SDR module
  - Up to 5280 DSP48E1 DSP blocks for complex signal processing
  - 85 Mbits Block RAM for data buffering and algorithm workspace
  - High-speed A/D and D/A interfaces for wideband signals
  - Fast DDR3 SDRAM memory interfaces for buffering and delay
  - 8 GB/sec PCIe Gen3 x 8 system interface eliminates backplane bottlenecks
  - 1 Gig Ethernet control interface for control and status
  - Aurora interfaces for inter-board and inter-FPGA data streaming
System Requirements

- Airborne 16 Antenna Array
- IF Frequency: 70 MHz
- IF Bandwidth: 40 MHz
- Beamforming Signal Processing:
  - Downconvert 16 IF signals to baseband
  - Apply phase shift to each baseband signal
  - Apply gain adjustment to each baseband signal
  - Sum 16 phase+gain adjusted baseband signals
- Deliver final sum to CPU
- Ruggedized, conduction-cooled 3U OpenVPX chassis
  - VITA 65 controls
  - OpenVPX standard
Functional System Block Diagram

- RF stages convert the antenna frequency down to IF
- A/D converters digitize the IF signals
- DDC downconverts IF to baseband with gain and phase adjustments
- Summation chain adds all 16 baseband signals
- CPU receives the beamformed sum
- CPU adaptively controls frequency, gain, and phase shifts for each antenna
53X61 Virtex-7 3U OpenVPX Beamformer

- Xilinx Virtex-7 FPGA
- Four 200 MHz 16-bit A/Ds
- Four Digital Downconverters (DDCs)
- Each DDC has independent Phase and Gain Adjustments
- PCIe x4 Interface
- Controls module operating modes
- Delivers phase and gain coefficients to the DDCs
53X61 Virtex-7 3U OpenVPX Beamformer

- Summer sums 4 DDC outputs
- Summer accepts Sum In from previous module
- Summer delivers Sum Out to PCIe interface and next module

- Xilinx Aurora Gigabit Serial Engine
  - Accepts 4X Sum In from previous module (2.5 GB/sec)
  - Propagates 4X Sum Out to next module (2.5 GB/sec)
53X61 Virtex-7 3U OpenVPX Beamformer

- Programmable Fabric
- Transparent Crossbar Switch
- User programmable crossbar switch path routing
- Allows flexible routing of Aurora sum and PCIe gigabit serial links to VPX P1 connector

![Diagram of Virtex-7 VX485T FPGA and GIGABIT SERIAL CROSSBAR SWITCH]

- CH A
  - RF In
  - 200 MHz
  - 16-bit A/D
- CH B
  - RF In
  - 200 MHz
  - 16-bit A/D
- CH C
  - RF In
  - 200 MHz
  - 16-bit A/D
- CH D
  - RF In
  - 200 MHz
  - 16-bit A/D

- DDC 1
  - Gain+Phase
- DDC 2
  - Gain+Phase
- DDC 3
  - Gain+Phase
- DDC 4
  - Gain+Phase

- ∑ SUMMER
- x4 PCIe Interface
- Aurora Gigabit Serial Interface
- SUM IN
- SUM OUT
- 4X SUM IN
- 4X SUM OUT

- VPX P0
- VPX P1
- VPX P2

- x4 Gig Serial
- x4 Gig Serial
- x4 Gig Serial
- x4 Gig Serial

- VPX BACKPLANE
Simplified block diagram

Available in both commercial and conduction-cooled versions

Four 4X gigabit serial or FP (“Fat Pipe”) connections to the data plane (DP) on VPX P1 connector

Crossbar switch supports many different backplanes and interconnection topologies
OpenVPX 3U Full Mesh 5-Slot Backplane

- Jointly specified by Pentek and DRS
- Designed and manufactured by Bustronic
- 5 Payload Slots connected as a full mesh
- Each VPX P1 connector has four X4 fat pipe ports (FP) for the OpenVPX data plane
- Each slot has one FP data plane connection to each of the other four slots

OpenVPX Backplane Profile: BKP3-DIS05-15.3.2-n
3U Backplane CPU Connections

- Install the four 53X61s in slots 1 thru 4
- Install the CPU card in slot 5 at the bottom
- The CPU is connected to each of the other four beamformer module slots with a 4X FP on the data plane
- Allows the CPU to send control and coefficients, and to receive data
Three other data plane 4X FPs join the four Virtex-7 beamforming modules in a chain.

This will support the Aurora sum in/sum out propagation between the modules.

Note: the fat pipes of the all Cobalt modules just happen to use DP04 for the CPU connection.

However, the summation chaining links use different DP fat pipes for each Cobalt module.
Mapping OpenVPX to the Virtex-7

- Crossbar switch connects the Aurora and PCIe FPs to the VPX P1 connector
- FP DP04: Used for x4 PCIe control interface maps to the CPU
- FP DP01, DP02, & DP03: Used for Sum In/Sum Out Beamforming Sum
- Crossbar switch allows flexible assignment to any FP port
Install four Virtex-7 3U VPX beamformer modules in payload slots 1 to 4
Install a 3U VPX PCIe CPU in payload slot 5 (bottom)
PCle control and data connections to CPU

- Provides four x4 PCle data plane fat pipes between CPU & each 53X61
- Delivers 16 sets of beamforming coefficients to 16 DDCs
Data plane fat pipes join the four 53X61s to propagate the 4X Aurora beamformed summation data in a daisy chain through the boards.
Final sum delivered via PCIe to CPU

- Final summation flows across x4 PCIe link from last 53X61 module in slot 4 to CPU card in slot 5.
Virtex-7 Delivers Solutions for SDR

- All critical resources SDR applications
  - Up to 5280 DSP48E1 DSP blocks for complex signal processing
  - 85 Mbits Block RAM for data buffering and algorithm workspace
  - High-speed A/D and D/A interfaces for wideband signals
  - Fast DDR3 SDRAM memory interfaces for buffering and delay
  - 8 GB/sec PCIe Gen3 x 8 system interface eliminates backplane bottlenecks
  - 1 Gig Ethernet control interface for control and status
  - Aurora interfaces for inter-board and inter-FPGA data streaming

- Virtex-7 53X61 3U VPX Module
  - Includes all critical beamforming functions
  - Four A/Ds, four DDCs with Phase & Gain Adjustments
  - Summation Block with Aurora Summation over VPX P1
  - Flexible Crossbar Switch Adapts to Many Backplanes
  - PCIe Gen 3 System Interface – 8 GB/sec