

The background of the slide features a blue gradient with abstract white and light blue geometric shapes, including squares and rectangles of various sizes, some of which are outlined. Several small, square inset images are scattered across the upper half of the slide. These images depict various military and technological themes: a tank, a satellite dish, a submarine, a fighter jet, a ship, and a satellite. The Pentek logo is prominently displayed in the upper right corner.

PENTEK

FPGAS TACKLE SIGNAL PROCESSING TASKS FOR VPX BEAMFORMING SYSTEMS

SDR'10

Wireless Innovation Conference

30 Nov – 3 Dec, 2010

Rodger Hosking

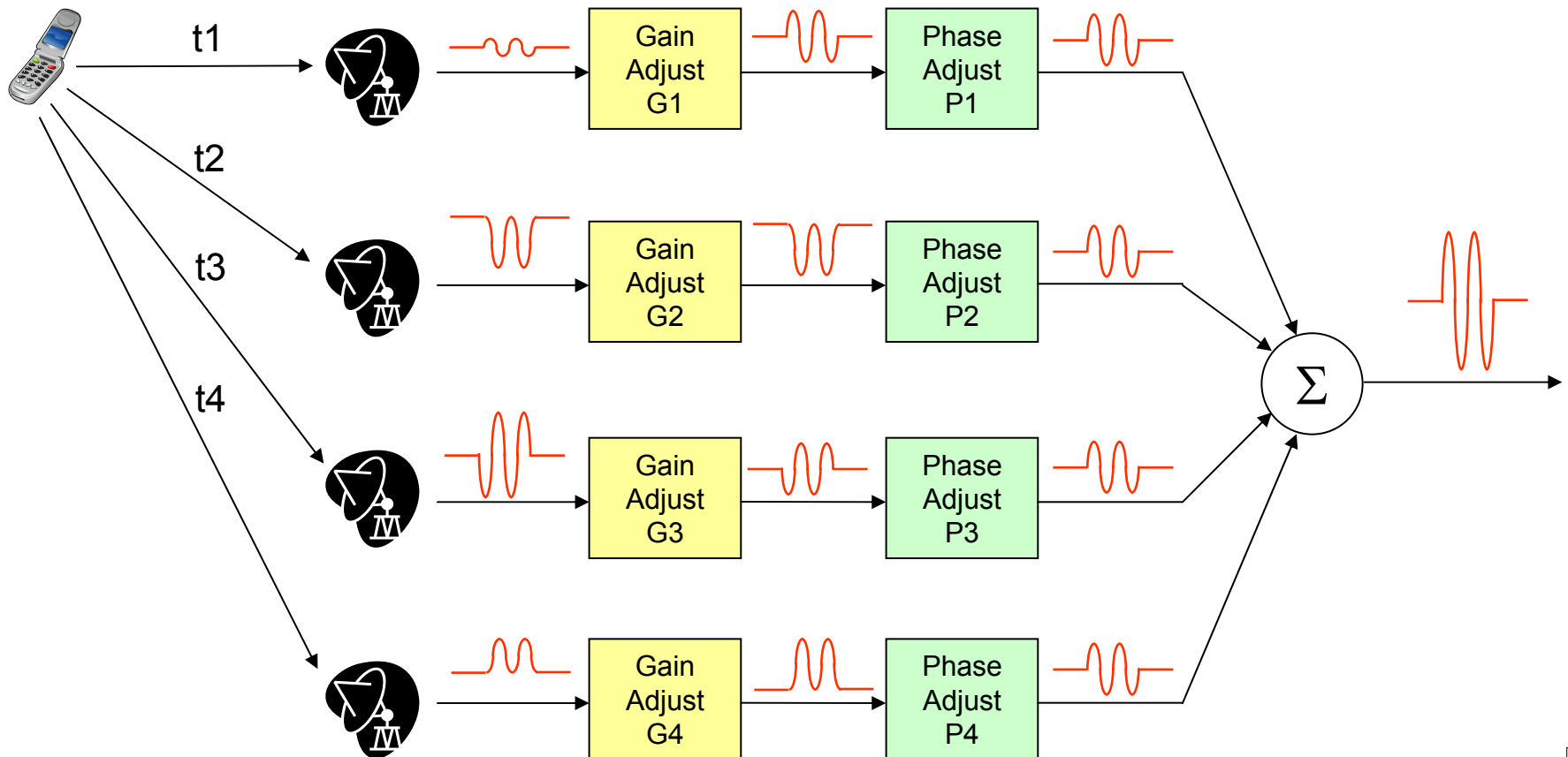
Pentek, Inc.

- Beamforming Basics
- System Requirements
- OpenVPX Beamforming Module
- OpenVPX Backplane and System Architecture
- Summary



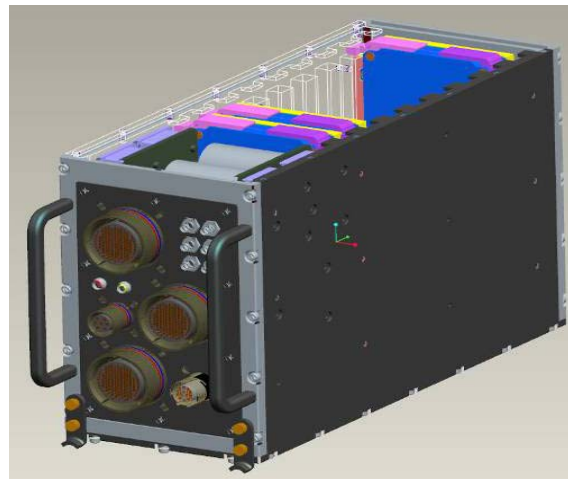
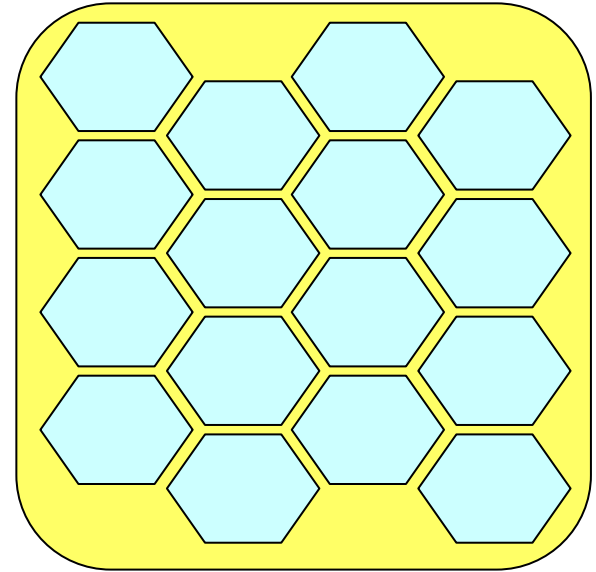
Principles of Beamforming

- Signal arrival delay at each antenna is based on path distance
- Beamforming adjusts gain and phase to align delays from one direction
- Aligned signals are summed to “steer” the directionality of the array
- Combined contributions from each antenna improve signal-to-noise



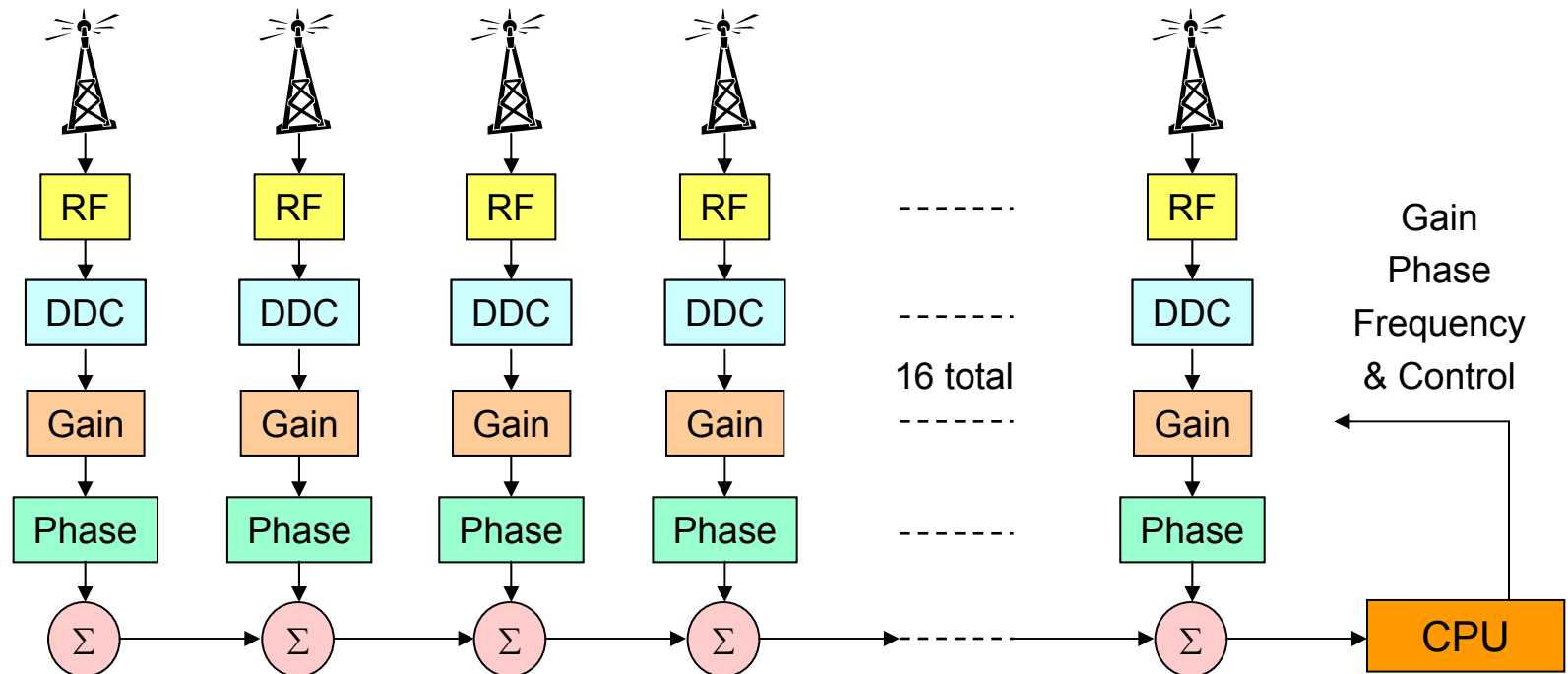
- Direction Finding
 - Beamformed antenna can be steered to locate arrival angle of signal source
- Diversity Receiver
 - Multiple elements beamformed towards a particular source improves reception
- Frequency Sharing
 - Cell phone systems share the same frequency by steering antennas by sector
- Radar Receiver
 - Phased array and synthetic aperture array (SAR) system use multiple antennas
 - Airborne arrays take full advantage of electronic steering – no moving mechanisms
- Fire control and Countermeasures
 - Missile detection and threat detection systems use beamformed arrays
 - Improved tracking allows earlier detection of object for more effective response
- Medical Diagnostics
 - MRI, CAT, PET and ultrasound imaging all use beamforming technology
- Hostile Fire Location
 - Triangulation of gunfire for defense, law enforcement and homeland security

- Airborne 16 Antenna Array
- IF Frequency: 70 MHz
- IF Bandwidth: 40 MHz
- Beamforming Signal Processing:
 - Downconvert 16 IF signals to baseband
 - Apply phase shift to each baseband signal
 - Apply gain adjustment to each baseband signal
 - Sum 16 phase+gain adjusted baseband signals
- Deliver final sum to CPU
- Ruggedized, conduction-cooled 3U chassis



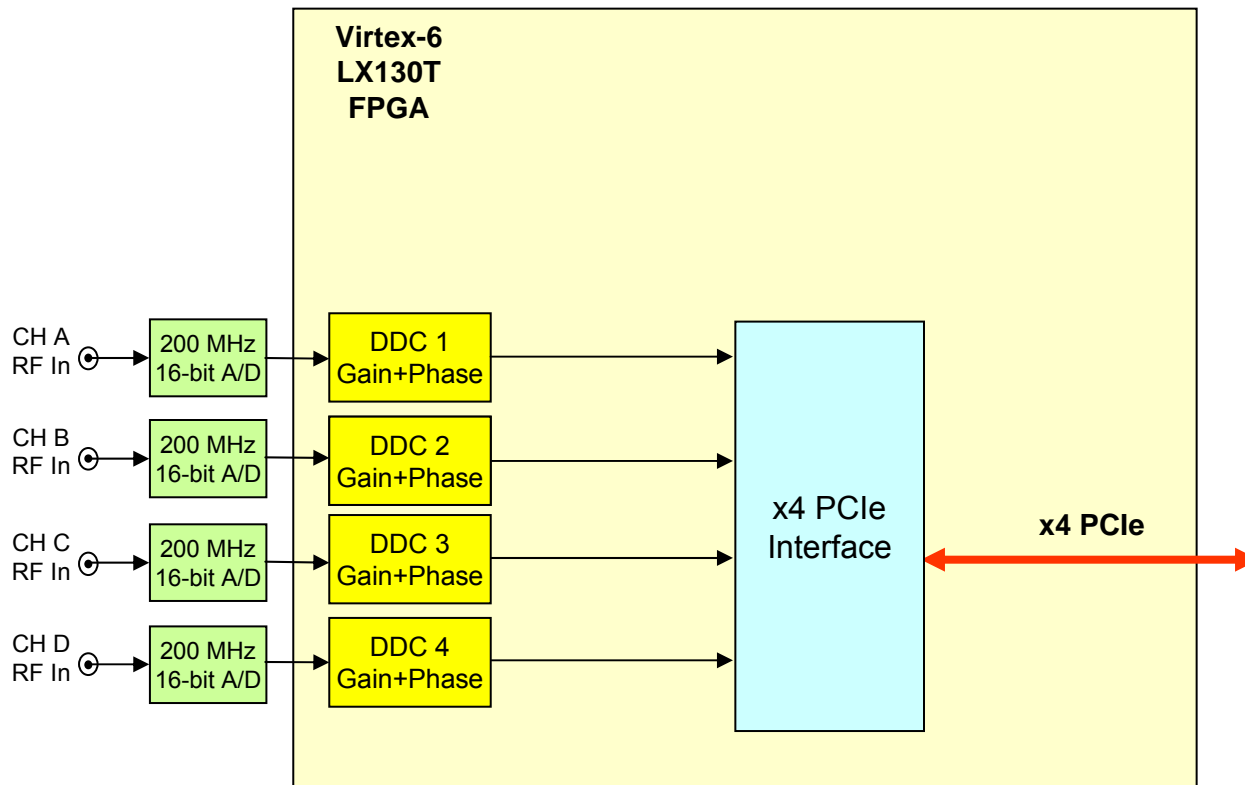
Functional System Block Diagram

- RF stage converts the antenna frequency down to IF
- DDC downconverts IF to baseband with gain and phase adjustments
- Summation chain adds all 16 signals
- CPU receives the beamformed sum
- CPU adaptively controls frequency, gain, and phase shifts for each antenna



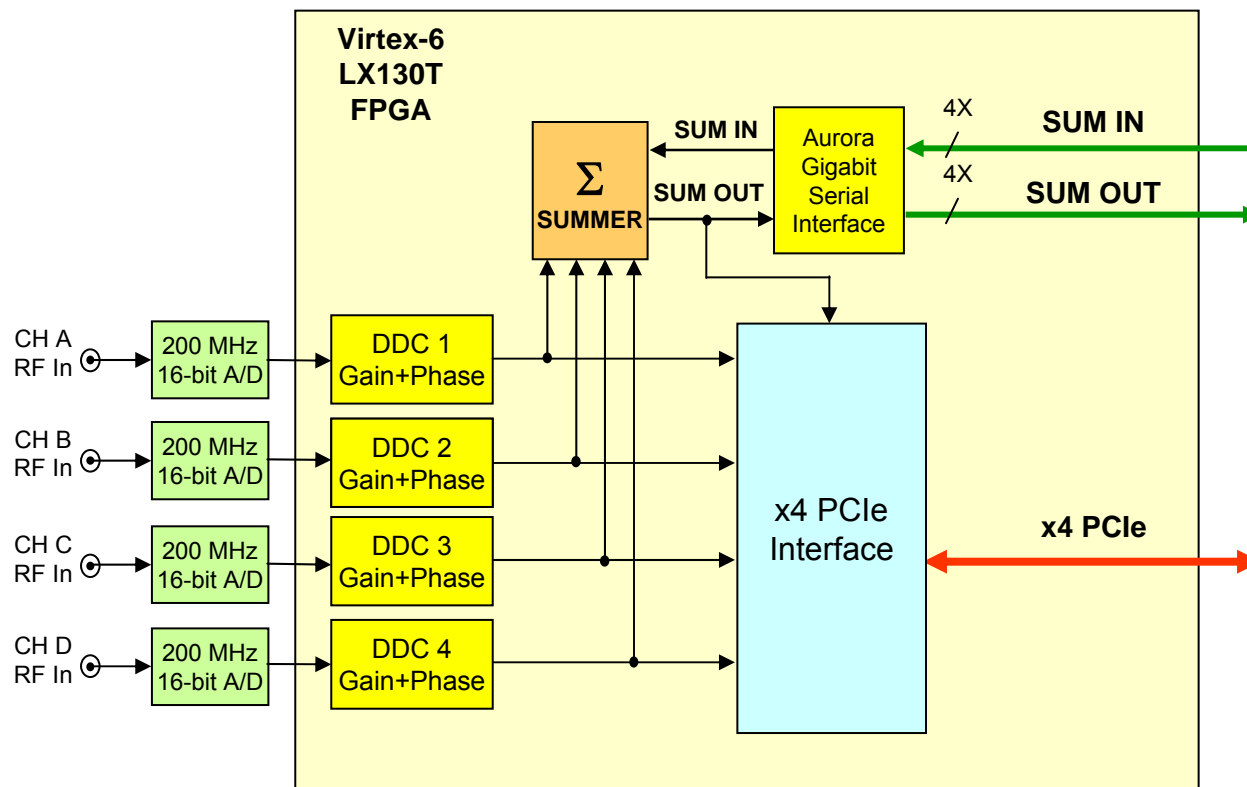
Model 53661 XMC Beamformer

- Xilinx Virtex-6 FPGA
- Four 200 MHz 16-bit A/Ds
- Four Digital Downconverters (DDCs)
- Each DDC has independent Phase and Gain Adjustments
- PCIe x4 Interface
- Controls module operating modes
- Delivers phase and gain coefficients to the DDCs



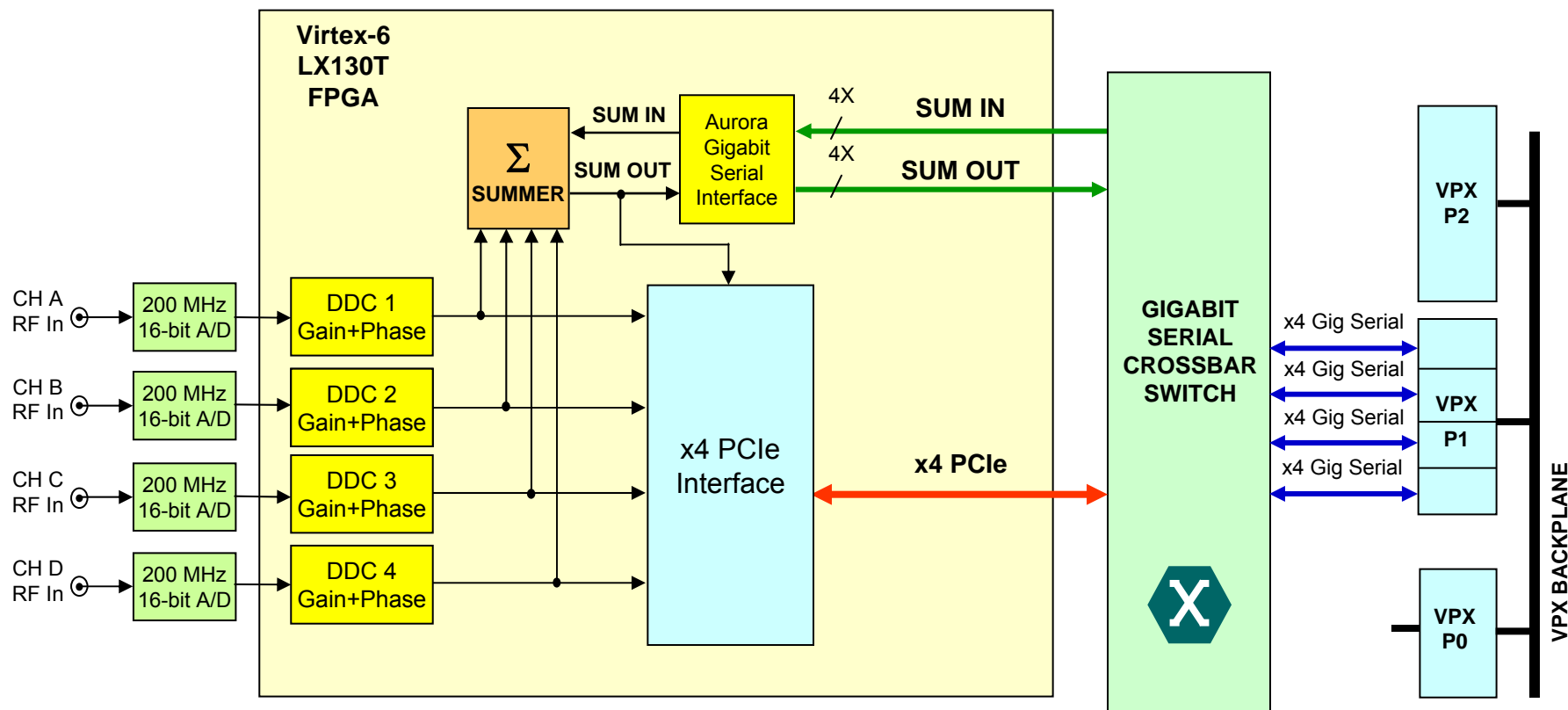
Model 53661 XMC Beamformer

- Summer block sums 4 DDC outputs
- Summer accepts Sum In from previous module
- Summer delivers Sum Out to PCIe interface and next module
- Xilinx Aurora Gigabit Serial Engine
 - Accepts 4X Sum In from previous module (1.25 GB/sec)
 - Propagates 4X Sum Out to next module (1.25 GB/sec)



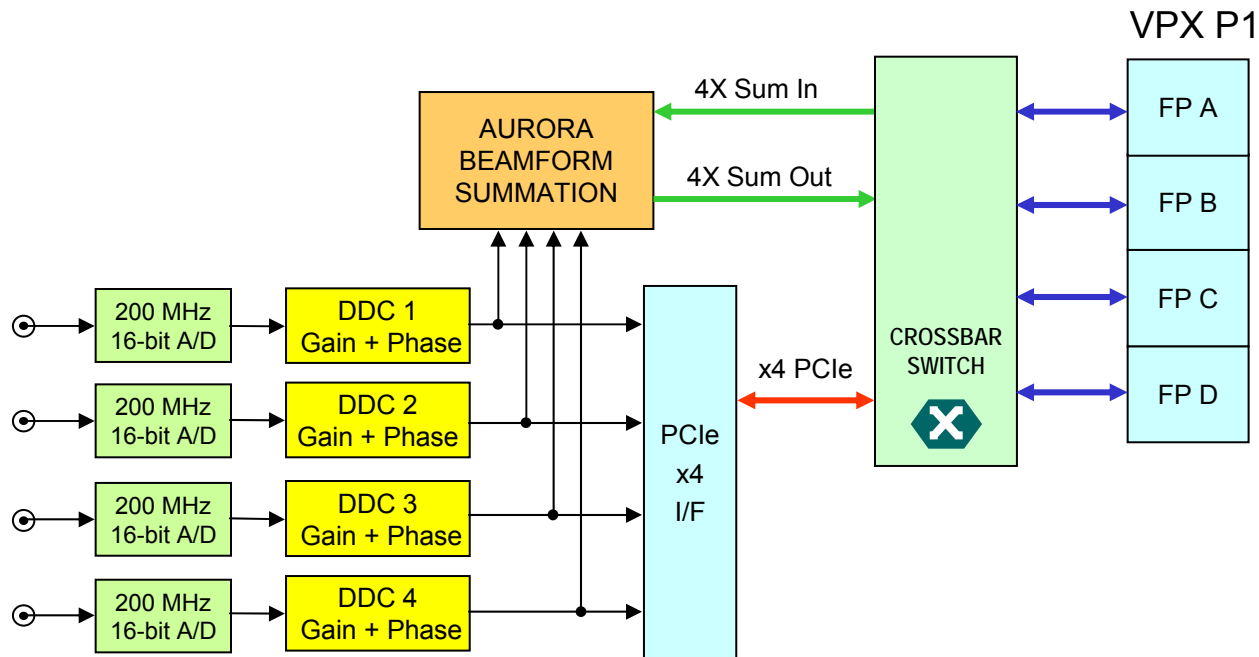
Model 53661 3U VPX Beamformer

- Programmable Fabric Transparent Crossbar Switch
- User programmable crossbar switch path routing
- Allows flexible routing of Aurora sum and PCIe gigabit serial links to VPX P1 connector



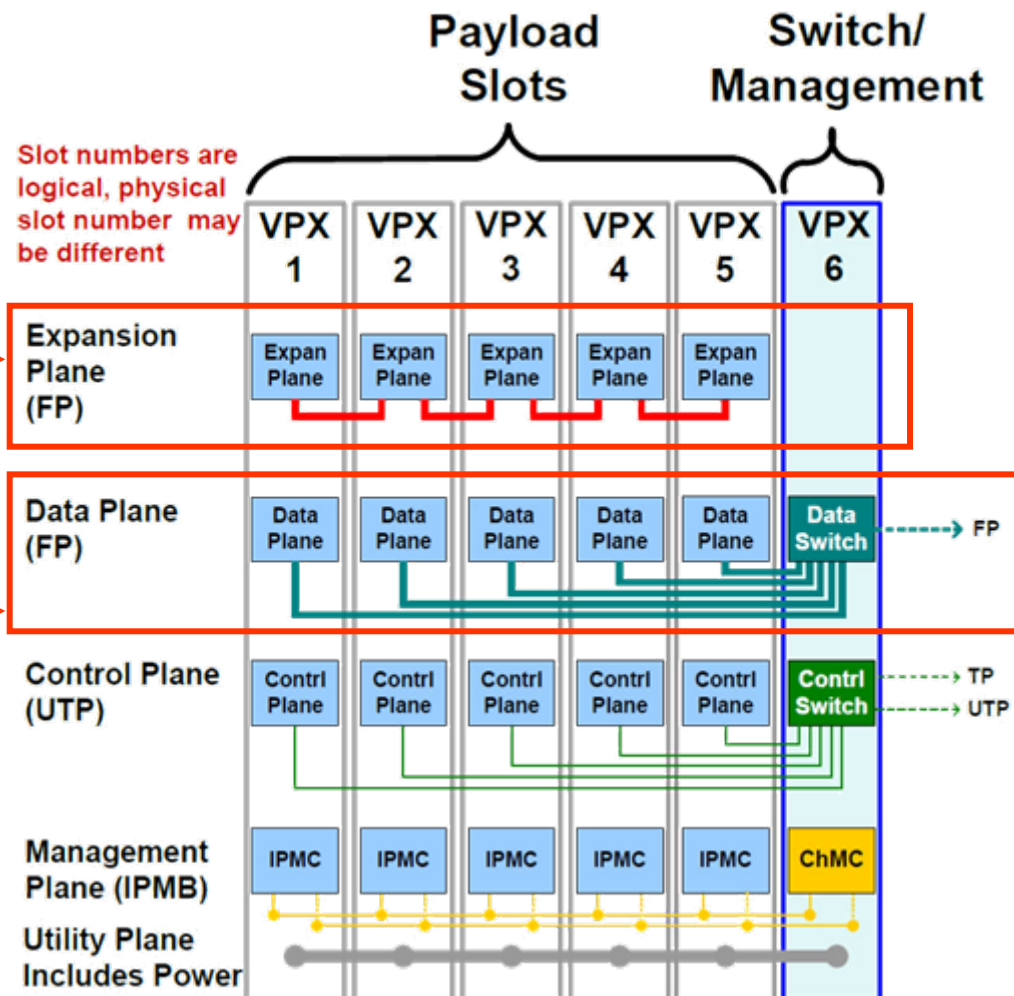
Model 53661 3U VPX Beamformer

- Simplified block diagram
- Available in both commercial and conduction-cooled versions
- Four FP (“Fat Pipe”) connections to VPX P1
- Crossbar switch supports many different backplanes



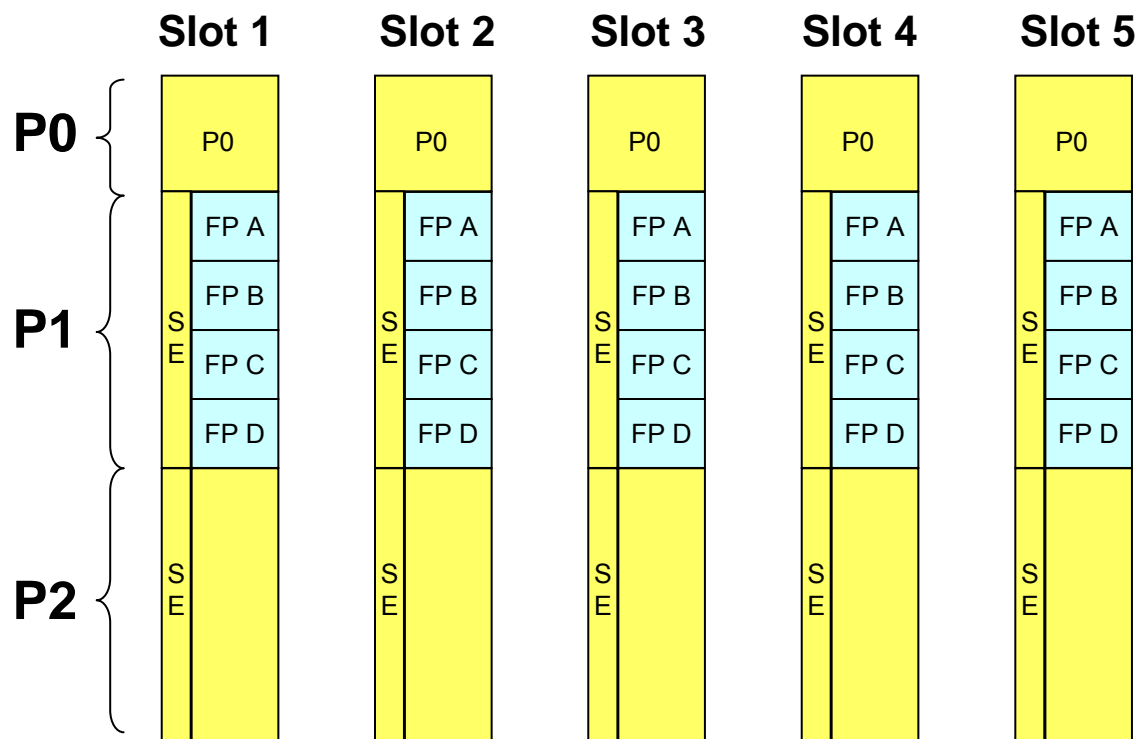
Choosing a 3U OpenVPX Backplane

- VITA 65 specifies a wide range of backplanes
- Many different backplane topologies are described
- **FP** (fat pipe) means four bi-directional gigabit lanes
- **Expansion Plane** defines links to support raw data transfers
 - Often Aurora, sFPDP, etc.
- **Data Plane** defines links for data packet transfers
 - Often PCIe, SRIO, etc.
- System Strategy
 - Use Data Plane for gain, phase and frequency control
 - Use Expansion Plane for beamforming summation path



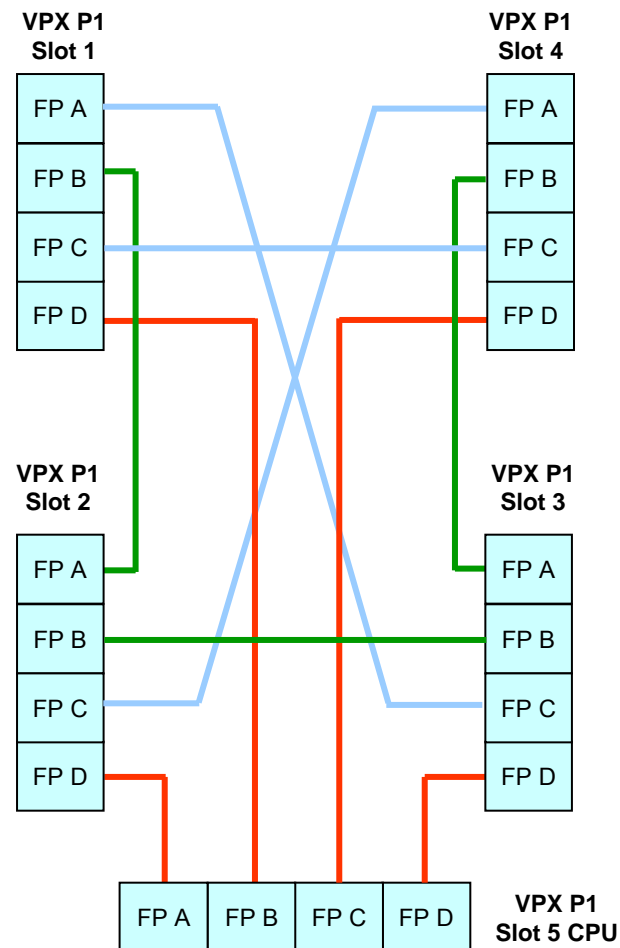
3U VPX 5-Slot Full-Mesh Backplane

- Jointly specified by Pentek and DRS
- 5 Payload Slots connected as full mesh
- Each P1 connector has four X4 fat pipe ports (FP)
- Each slot has one FP connection to the other four slots



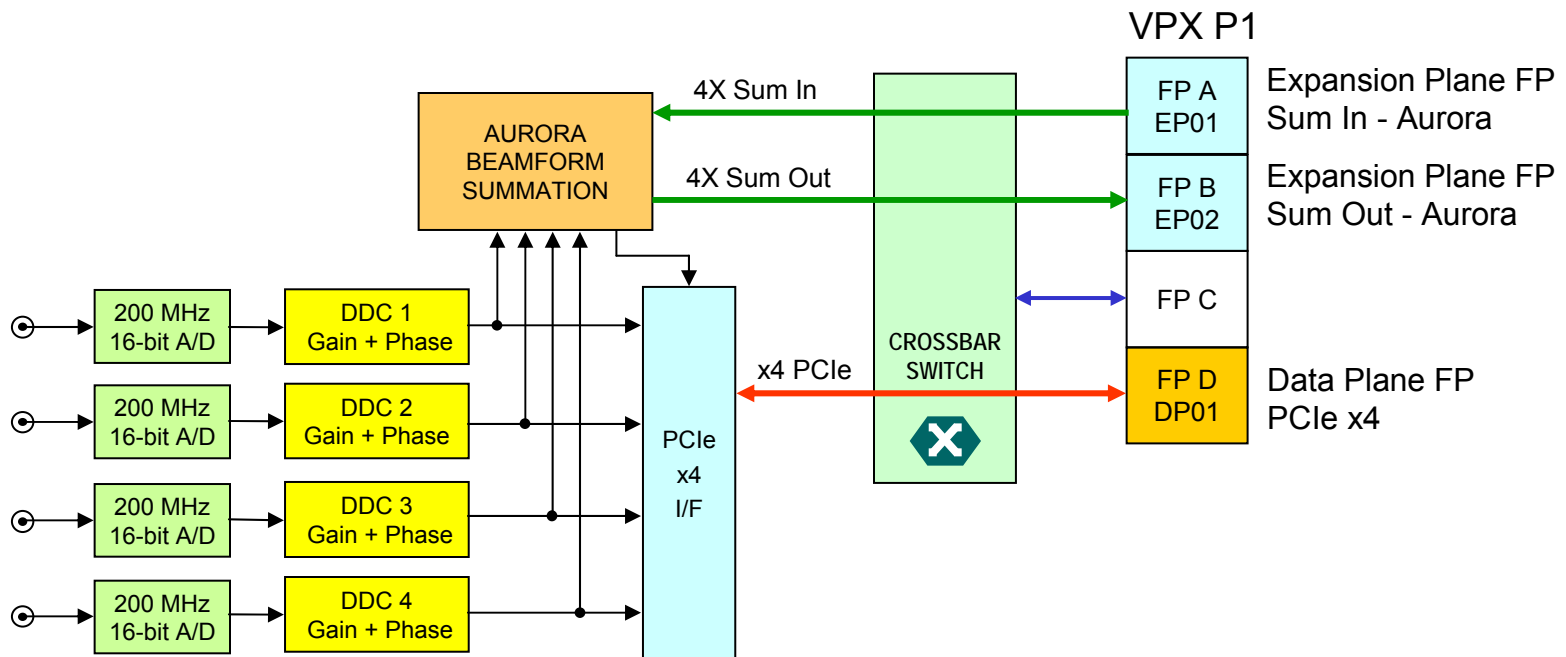
VPX P1 Fat Pipe Connections

- VPX P1 connectors are rearranged for clarity
- X4 fat pipe (FP) mesh interconnects are shown
- Each VPX slot is joined to each of the other slots with one FP
- Expansion plane requirement is met: sum data propagates between slots 1 thru 4
 - FP A and FP B can be used for sum in and out (green links)
- Data plane requirement is met: slots 1 thru 4 connect to the CPU in slot 5
 - FP D of slots 1 – 4 connect to all four FPs on slot 5 (red links)



Mapping OpenVPX to the Model 53661

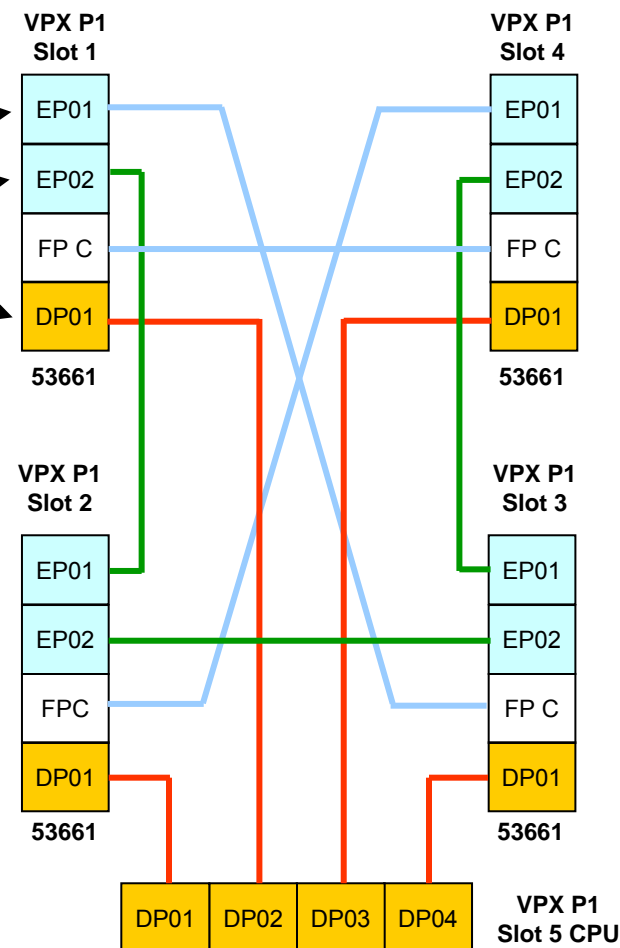
- Crossbar switch is configured the Aurora and PCIe FPs to VPX P1 connector
- FP A: 4X Aurora Sum In maps to Expansion Plane EP01
- FP B: 4X Aurora Sum Out maps to Expansion Plane EP02
- FP D: x4 PCIe control interface maps to Data Plane DP01



Mapping OpenVPX onto the Backplane

- Slot 1 through Slot 4 – Model 53661

- FP A maps to Exp Plane EP01 (Sum In)
- FP B maps to Exp Plane EP02 (Sum Out)
- FP D maps to Exp Plane DP01 (PCIe x4)



Mapping OpenVPX onto the Backplane

- Slot 1 through Slot 4 – Model 53661

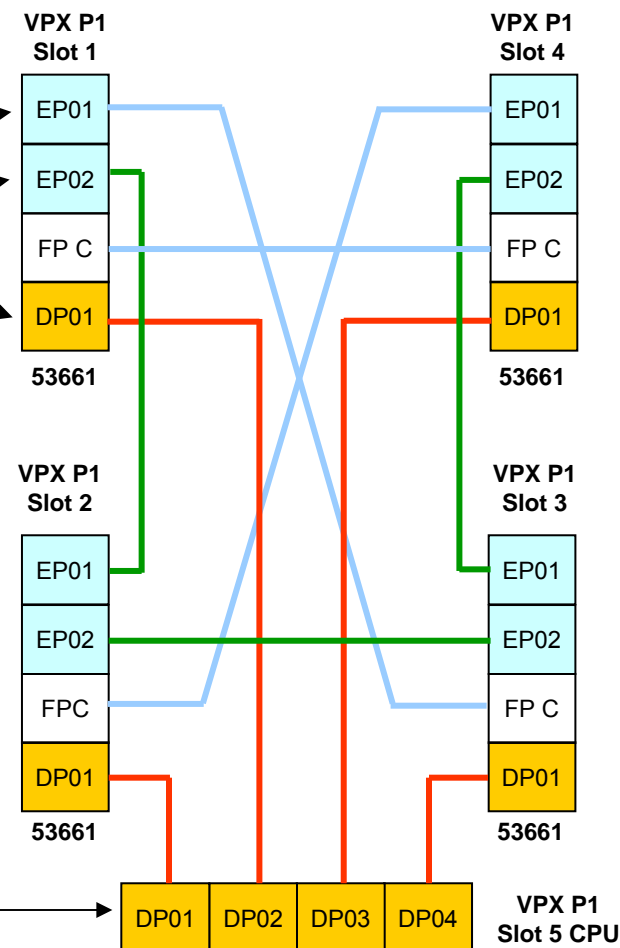
- FP A maps to Exp Plane EP01 (Sum In)
- FP B maps to Exp Plane EP02 (Sum Out)
- FP D maps to Exp Plane DP01 (PCIe x4)

- Slot 5 – CPU

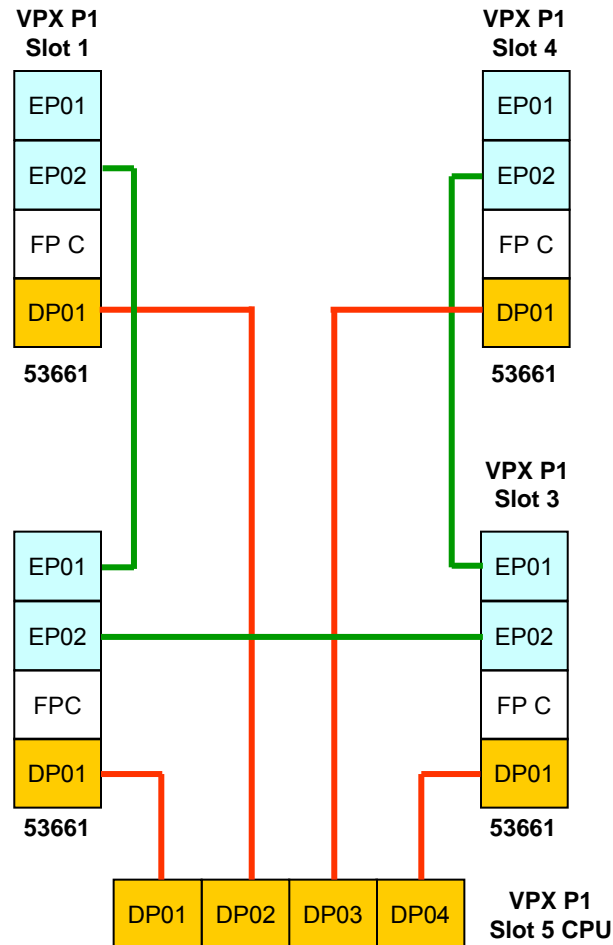
- FP A maps to Data Plane DP01
- FP B maps to Data Plane DP02
- FP C maps to Data Plane DP03
- FP D maps to Data Plane DP04

- Not all links are required

- Links in blue can be removed from drawing for clarity

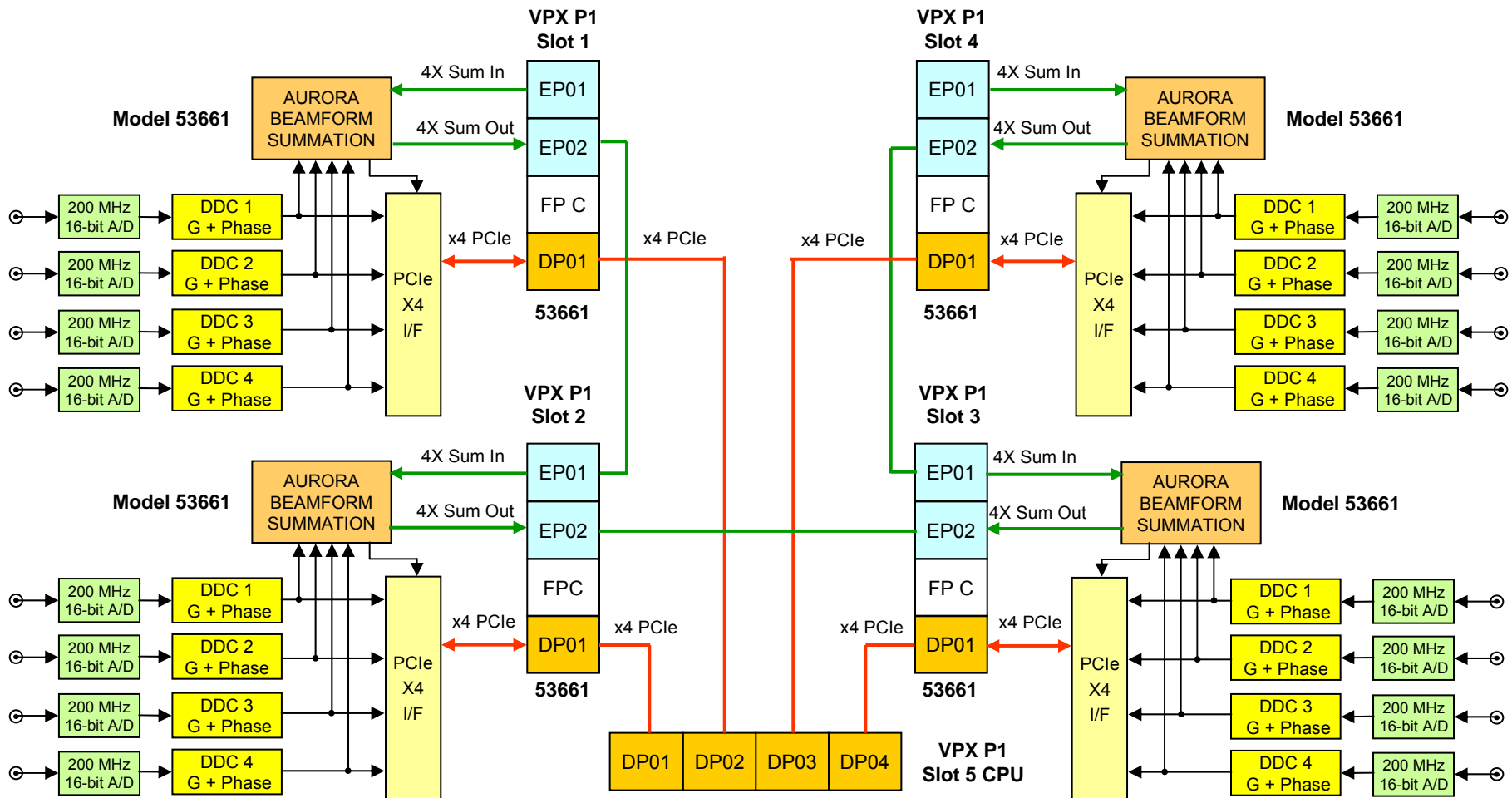


Simplified Backplane Interconnections

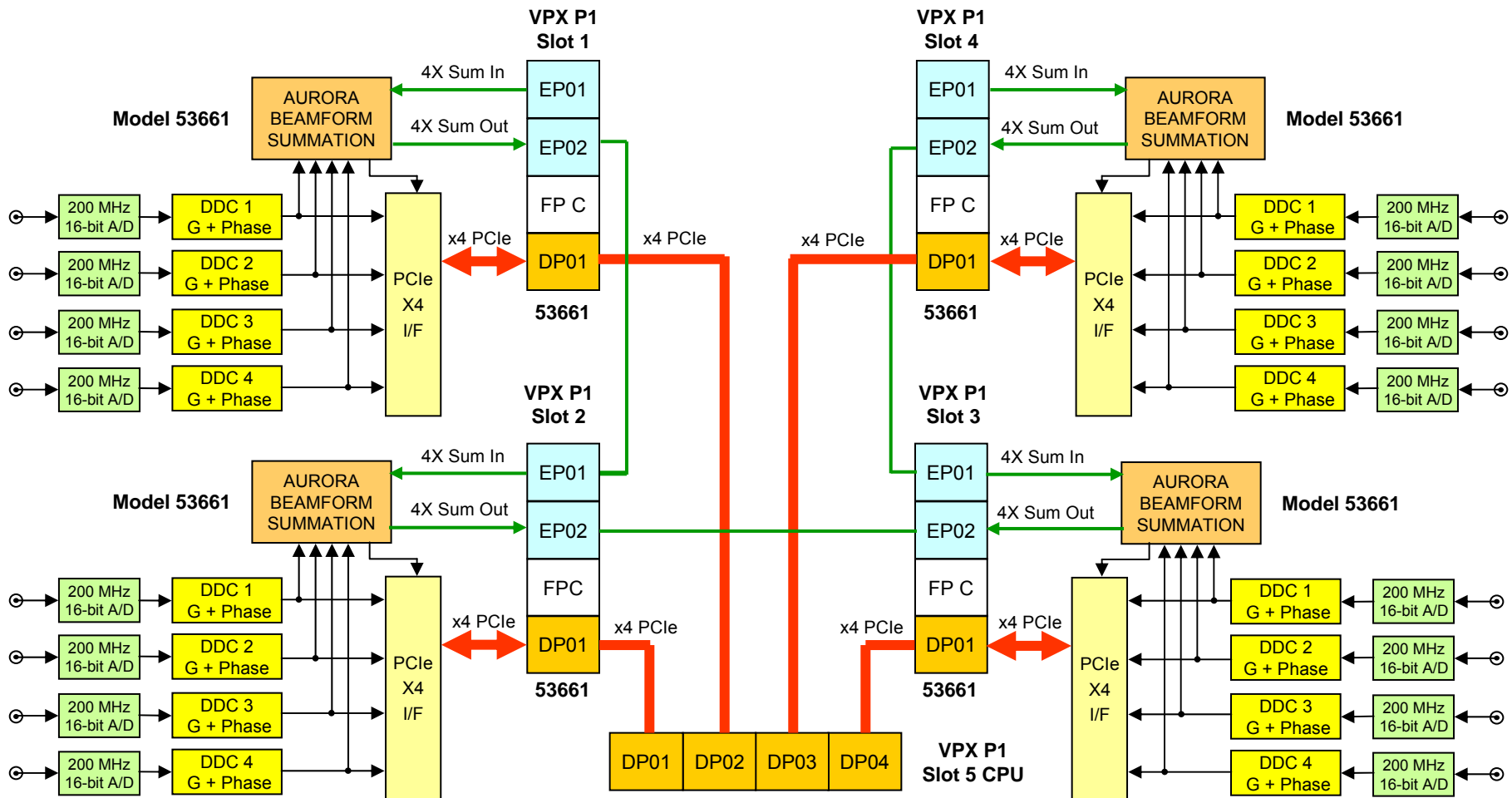


Modules installed in the backplane

- Install four 3U VPX 53661 beamformer modules in payload slots 1 through 4
- Install a 3U VPX PCIe CPU in payload slot 5 (bottom)

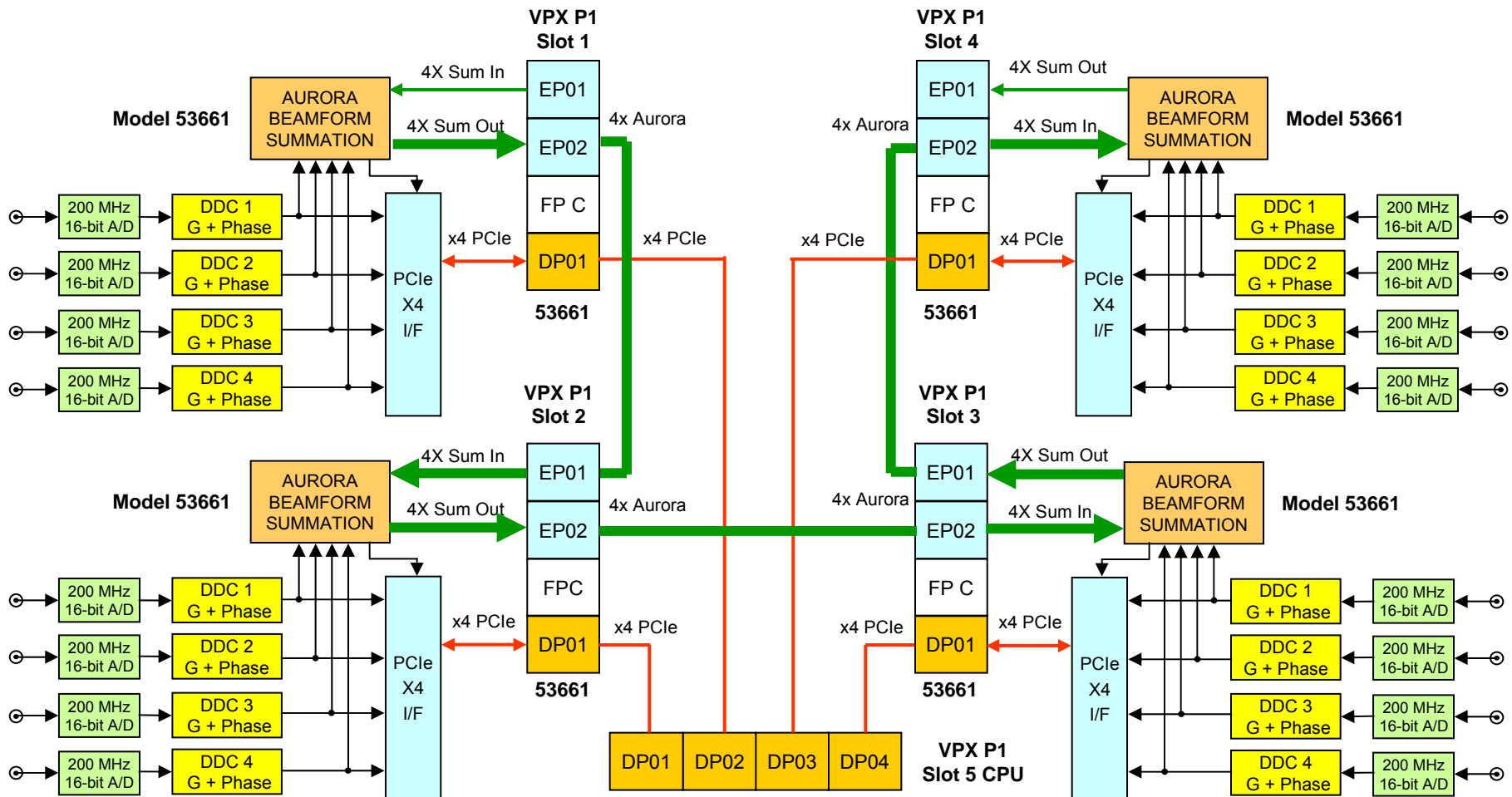


- Provides four x4 PCIe data plane fat pipes between CPU and each 53661
- Delivers 16 sets of beamforming coefficients to 16 DDCs



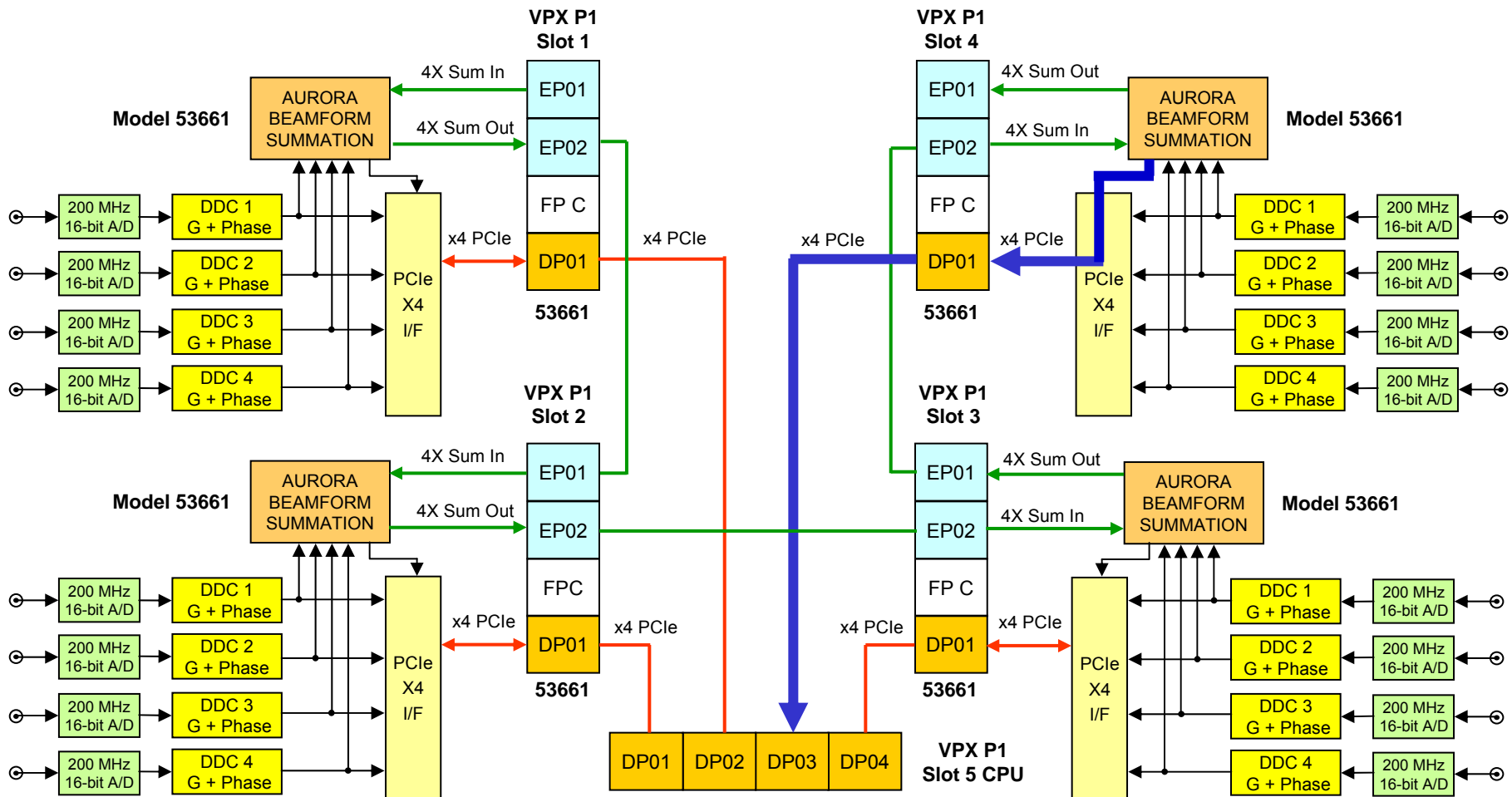
Beamformed sum propagation paths

- Expansion Plane fat pipes join the four 53661s to propagate the 4X Aurora beamformed summation data in a daisy chain through the boards



Final sum delivered via PCIe to CPU

- Final summation flows across x4 PCIe link from last 53661 module in slot 4 to CPU card in slot 5



- FPGA-Based Model 53661 3U VPX Module

- Xilinx Virtex-6 FPGA: Scalable up to 2016 DSP Engines
- Includes all critical beamforming IP functions
- Four A/Ds, four DDCs with Phase & Gain Adjustments
- Summation Block with Aurora Summation over VPX P1
- VPX P1 PCIe interface to PCI-X bus on for control

- OpenVPX: An Excellent Embedded Architecture Solution

- Supports multiple protocols
- Eliminates backplane bottlenecks with fast, dedicated gigabit serial links
- Presents a well defined, standard nomenclature for system components
- Provides standard profiles for cards, slots, backplanes and chassis
- Improves MTBF and MTTR through modular design and backplane interconnects
- Defines forced-air, circulating liquid, and conduction cooled strategies
- Supports severe environmental requirements for rugged applications
- Offers a high degree of scalability



VPX Technology Central

- VPX Overview
- OpenVPX FAQ
- VPX Marketing Alliance

VPX Press Releases

- [Model 53661 VPX Release](#) (November 2010)
- [OpenVPX ANSI Ratification](#) (June 2010)
- [14 VPX Software Radio Products](#) (April 2010)

Recent Pipeline Newsletters

- [VPX & VXS System Development Strategies](#) (Spring 2010)
- [Switched Topologies for Extreme Performance](#) (Winter 2008)

Handbooks

- [Switched Serial Fabric Handbook](#)

Recent Pentek Articles

- [VME & Critical Systems: Migrating to VPX - Without Leaving VME Behind](#) (June 2010)
- [MIL COTS Journal: VPX and VXS: System-Level Switched Fabric Strategies](#) (Mar 2010)
- [Open Architecture Review: VXS & VPX](#)

Product Selector Tool

- Find products easily using key parameters

VITA Standards

- www.vita.com for VPX Specification

Pentek, Inc. - VPX - Mozilla Firefox

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http://www.pentek.com/vpx/vpx.cfm

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SITE MAP

VPX Technology

Pentek Model 5353

A high-speed software radio board designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds supported by a high-performance 4-channel installed DDC and a complete set of beamforming functions. With built-in multiboard synchronization, it is ideally matched to the requirements of real-time software radio and radar systems.

"The introduction of VPX and its state-of-the-art interconnect technology provides significant benefits for high-speed serial systems. VPX technology allows for higher data transaction bandwidth, increased scalability and improved reliability in both commercial and rugged systems."

Marc Ruocco
Product Manager

VPX 3U Products

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Serial Fabrics Handbook

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Data Acquisition and Software Radio Product Search Parameters

Form Factor	Auxiliary IO	Min DDC Chan	Min A/D Chan	Min A/D Bits	A/D Sample Freq.	Max Input Freq.	Min DUC Chan	Min D/A Chan	Min D/A Bits	D/A Sample Freq.
All	All	All	All	All	All	All	All	All	All	All
cPCI 3U	'C40 Comm Port	2	2	10	50 kHz	22.5 kHz	1	1	12	200 MHz
MIX	FPDP/FPDPII	4	3	12	216 kHz	100 kHz	2	2	16	500 MHz
PCI	PCle	8	4	14	234 kHz	2 MHz		4		800 MHz
PCle	PPI	16	8	16	250 kHz	8 MHz				

CERTIFIED QUALITY MANAGEMENT SYSTEM

ISO 9001:2008