FPGAS TACKLE SIGNAL PROCESSING TASKS FOR VPX BEAMFORMING SYSTEMS

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ABSTRACT

Beamforming is a signal processing technique that utilizes an array of sensors to achieve directionality, increase the strength of transmitted signals and improve the quality of received signals.

Beamforming applications span frequencies from sub-audio to light, and encompass a diverse range of critical applications for commerce, industry, government and defense. Systems developers are continuously exploiting new technology to boost performance for specific applications, with significant emphasis on communications and signals intelligence.

This paper outlines the general principles of beamforming as applied to the reception of radio frequency signals, followed by a basic discussion of the required signal processing algorithms. Then this paper presents the several important roles in beamforming played by the latest generation of FPGAs (Field Programmable Gate Arrays), including both the key DSP resources, and the fast links for data transmission.

Finally, a powerful new embedded system architecture called OpenVPX will be harnessed, showing how its features are extremely well suited for implementing deployable, highly-scalable beamforming systems.

1. PRINCIPLES OF BEAMFORMING

For software radio systems, the beamforming sensors are transmit and receive antennas. For receiver systems, the signal arrival delay at each antenna is directly proportional to the path distance from the source. The beamforming process adjusts the gain and phase of each antenna signal to cancel the delay path differences for signals arriving from a particular direction. Aligned signals are then summed together to produce high signal to noise reception in the chosen direction.

By adjusting gain and phase in each path, the antenna is electronically "steered" without the need for moving mechanical structures. Examples of software radio applications that use beamforming include direction finding, in which a beamformed antenna can be steered to locate the arrival angle of a signal source. Two or more the arrays can be used to triangulate the exact location of the source, which is essential for many signal intelligence and counter terrorism efforts.

In addition to directionality, beamforming also improves reception in so-called “diversity receivers”. The combined signal from multiple antennas boosts the signal-to-noise ratio compared to a single antenna, thus extending the operational range of the receiver system.

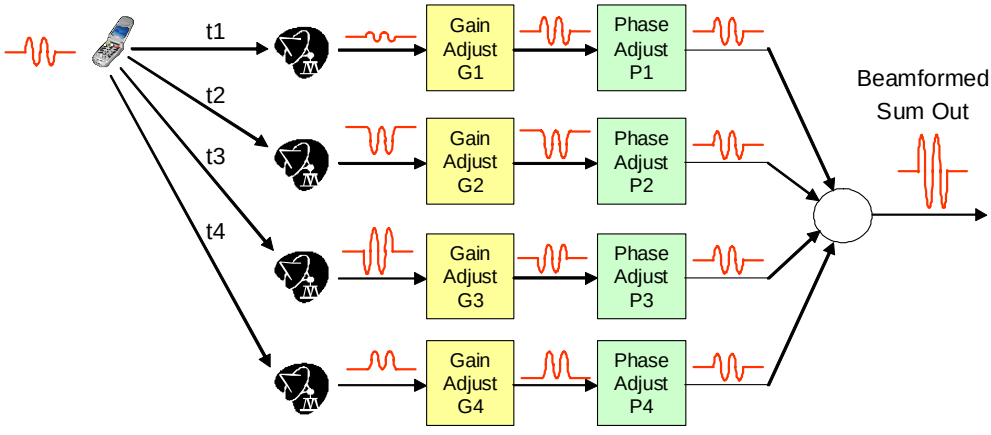

Figure 1. Beamforming adjusts phase and gain of signals from each antenna in an array to compensate for differential delays (tn) and attenuation, so that signals arriving from a particular angle relative to the array add constructively when combined in the summer.

Missile detection and countermeasure applications use beamforming to improve tracking of an object allowing for early detection and improved responsiveness. With no moving mechanisms, airborne arrays take full advantage of electronic steering to dramatically improve the range and target resolution. And lastly, beamforming allows spatial frequency sharing for commercial mobile phone carriers by dividing one cell into several beamformed pie-slice sectors that can share the same frequency.

2. FPGAs: IDEAL BEAMFORMING ENGINES

Each new generation of FPFA delivers new features, higher levels of performance, and reduced power consumption for a given function. The latest announcement from Xilinx is the new 7 Series featuring 28 nm technology, serial gigabit transceivers with rates up to 13 GHz, fast PCI Express end points, nearly 4,000 DSP engines, and over 900,000 logic cells. FPGAs have become extremely popular for embedded software radio functions, and they are especially appropriate for beamforming applications.

After amplification and analog downconversion to an IF frequency, each antenna signal must be digitized with an A/D converter. To handle this task, FPGAs offer high speed LVDS interfaces supporting data converter peripherals operating at sample rates to 500 MHz and higher.

The next task is digital downconversion of the IF signal to complex baseband, which is performed by mixing the input signal with the signal from a numerically controlled local oscillator (NCO). The mixer employs one of the multipliers in an FPGA DSP block and the NCO is a phase accumulator (also part of the DSP block) followed by a sine look-up table. This is followed by a low pass filter (using multipliers, registers and adders) set equal to the signal channel bandwidth. Together, the mixer, NCO and filter all comprise the DDC, or digital downconverter. Special circuitry incorporated in the DDC allows the user to adjust the phase and gain of the downconverted signals to support the special requirements of beamforming. The adjusted outputs of each DDC are summed together, again taking advantage of the adder in the DSP block.

A/D conversion plus all beamforming DSP operations for up to four channels can be handled in a contemporary FPGA-based software radio module. However, for larger systems with many antennas, the summation must accommodate multiple modules which must operate with synchronous sampling and must preserve strict alignment of DDC samples forming the final sum.

3. VPX BEAMFORMING MODULE

OpenVPX, based on the recently adopted VITA 65 standard, provides an effective taxonomy for describing VPX components, and also defines numerous “profiles” for boards, slots and gigabit serial backplanes that detail specific configurations of channels, interconnections, and fabrics. Instead of starting from scratch each time, designers can browse through these standardized profiles to find one that satisfies the objectives of each new system. By narrowing the field of configurations, these profiles boost reusability and interoperability between vendors.

Pentek’s Model 5353 Software Radio Beamformer is a 3U OpenVPX module, featuring four 200 MHz 16-bit A/D converters and two Virtex-5 FPGAs. Inside the first FPGA are four digital downconverters (DDCs) with programmable phase shift and gain, four power meters at each DDC output and interfaces to the four A/D converters. A simplified block diagram of the 5353 is shown in Figure 2.

The Model 5353 also includes a summation block that adds the DDC outputs to form a four-channel beamforming sum. This block also accepts a propagated “sum in” signal from another module and generates a propagated “sum out” signal to the next module. The sum in and sum out signals use two X4 Aurora gigabit serial links connected to the VPX P1 backplane connector, each capable of moving data at 1.25 GB/sec peak.

To support a 20 MHz IF channel bandwidth with a 25% filter margin, the DDC outputs deliver complex 16-bit I+Q samples at 25 MHz, or 100 MB/sec. The propagated sum in/sum out signals also operate at 100 MB/sec and are thus easily handled by the 1.25 GB/sec X4 Aurora links.

The 5353 system interface for control and data is an X4 PCIe port, also connected to P1. Bandwidth requirements for the control and data port are dominated by delivery of the final beamformed sum out to the control processor. This 100 MB/sec stream falls well within the 2 GB/sec peak rate of the X4 PCIe port when operating in Gen 2 mode.

A programmable, fabric-transparent crossbar switch allows free assignment of the two X4 Aurora ports and the X4 PCIe port, in any combination, to the four X4 links on P1. This flexibility allows the 5353 to accommodate various VPX slot profiles and backplanes.

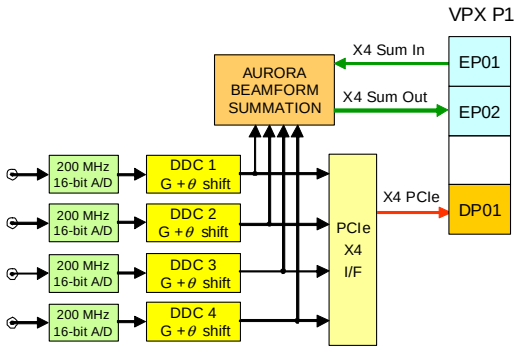

Figure 2. Model 5353 3U VPX Beamformer Module with four A/Ds, four DDCs, X4 PCIe interface, gain adjusts, phase shifters and summation engine for beamforming.

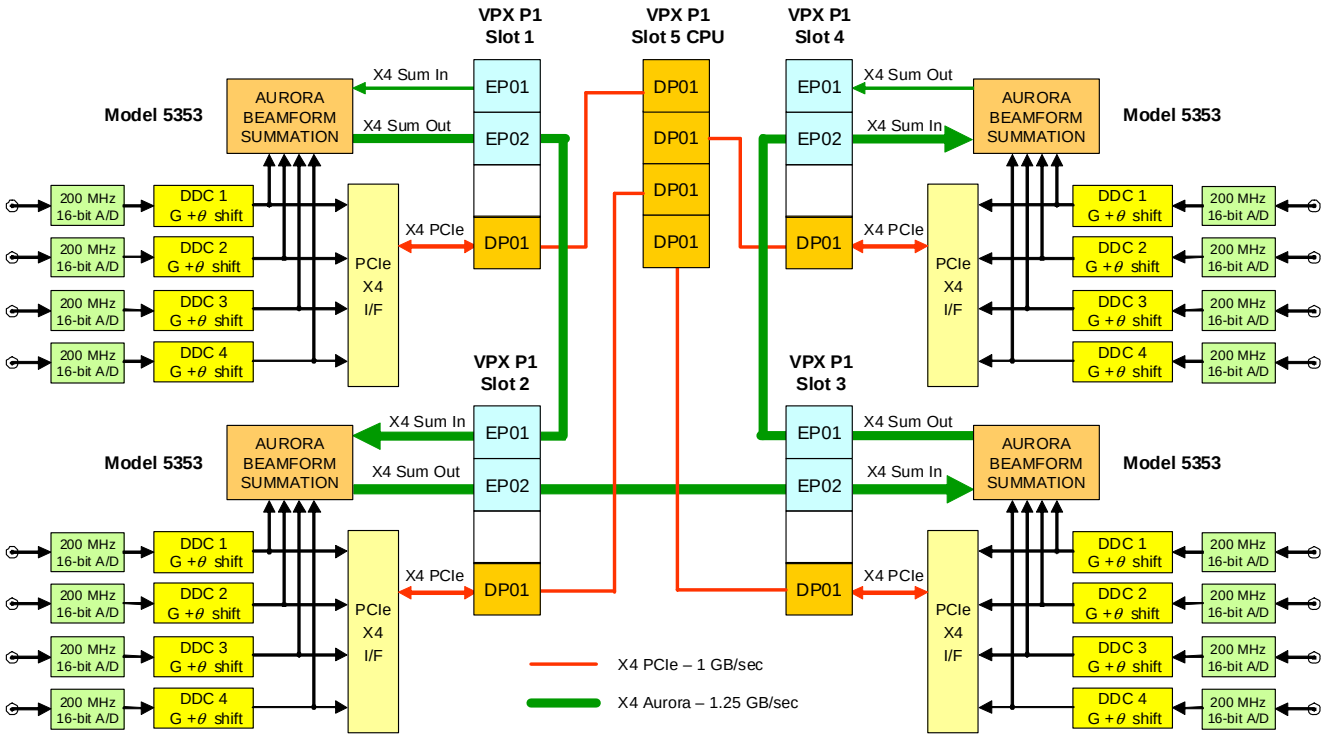

Figure 3. 16-Channel VPX Beamforming System. Each Model 5353 creates four beamformed signals which contribute to a summation signal propagated through X4 Aurora gigabit serial backplane links on the expansion plane. A CPU module connects to all four 5353's using X4 PCIe using data plane gigabit serial backplane links on the data plane.

For a larger system with 16 antennas, a total of four 4-channel 5353 modules are required. Since the summation chain requires the same data rate as each DDC, the two sum ports must simultaneously handle 100 MB/sec each. This class of signals falls under the definition of "expansion plane" in the OpenVPX specification.

The X4 PCIe interface to handle the data initialization, and delivery of beamforming parameters is described as the "control plane" under OpenVPX. Final delivery of the beamformed result to the system control processor is best classified as the "data plane" in OpenVPX definitions.

4. 16-CHANNEL VPX BEAMFORMING SYSTEM

A 16-channel VPX-based FPGA-based beamformer system using four Model 5353 3U VPX modules is shown in Figure 3. Using the dedicated X4 PCIe links, each module connects to a CPU card located in slot 5, serving as the control and status processor for the system.

Each 5353 module digitizes four IF signals from four antennas in the array. Four digital down converters translate the antenna IF signals to baseband as complex digital samples and then perform beamforming signal processing, including phase shifts and gain adjustments.

The OpenVPX backplane most appropriate for this system is a five-slot "full mesh" topology design which provides one X4 link from each slot to every other slot.

Each summation engine accepts the propagated sum from the previous module, adds the four channels from the local module and then generates a new sum signal for delivery to the sum input of the next module in the chain. The summation paths use Aurora 4X gigabit serial links for the expansion plane connections across the backplane. The final 16-channel sum is delivered from the 5353 in slot 4 to the CPU card in slot 5 across the X4 PCIe interface.

5. SUMMARY

There are several major benefits to this system architecture. First, FPGAs implement the data acquisition, digital down conversion, beamforming DSP tasks, and gigabit serial system interfaces. Secondly, all interboard summation paths are supported with existing links on the OpenVPX backplane. Third, the system is highly modular and scalable: additional 5353 modules can be added as required to increase the number of antenna channels. Finally, OpenVPX provides a ruggedized solution capable of operating in a wide range of deployed environments.

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