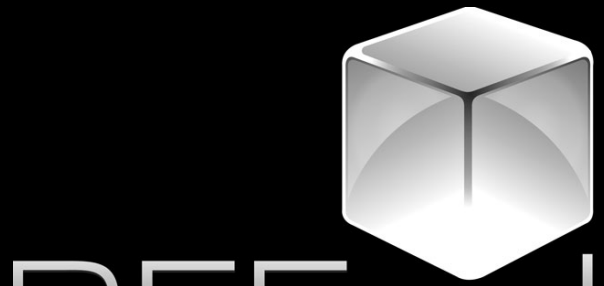
Multi-GHz Software and Hardware Platform for Software Defined Radio



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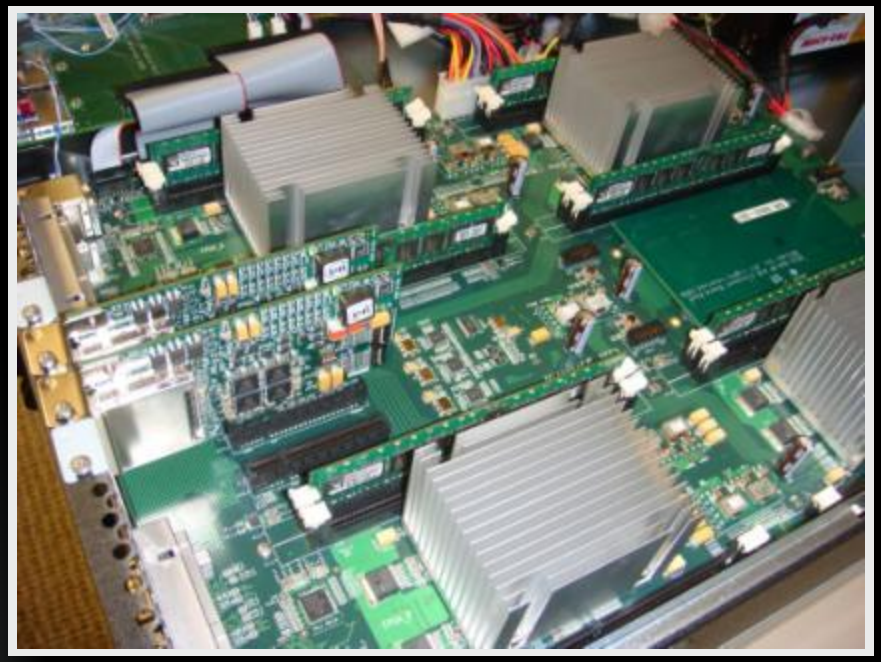
SDR and Cognitive Radio Strategies Challenges

- Meeting “Dynamic” Mission-Critical Communication Needs
- Prototyping New Radio Algorithms in Real Time
- Mixed Signal (Analog and Digital) Designs

BEE3-W —Digital Communication Design Platform



- Signal Intelligence
- Software Defined Radio
- Radar Signal Processing
- Cognitive Radio
- MIMO Communication
- Signal Warfare

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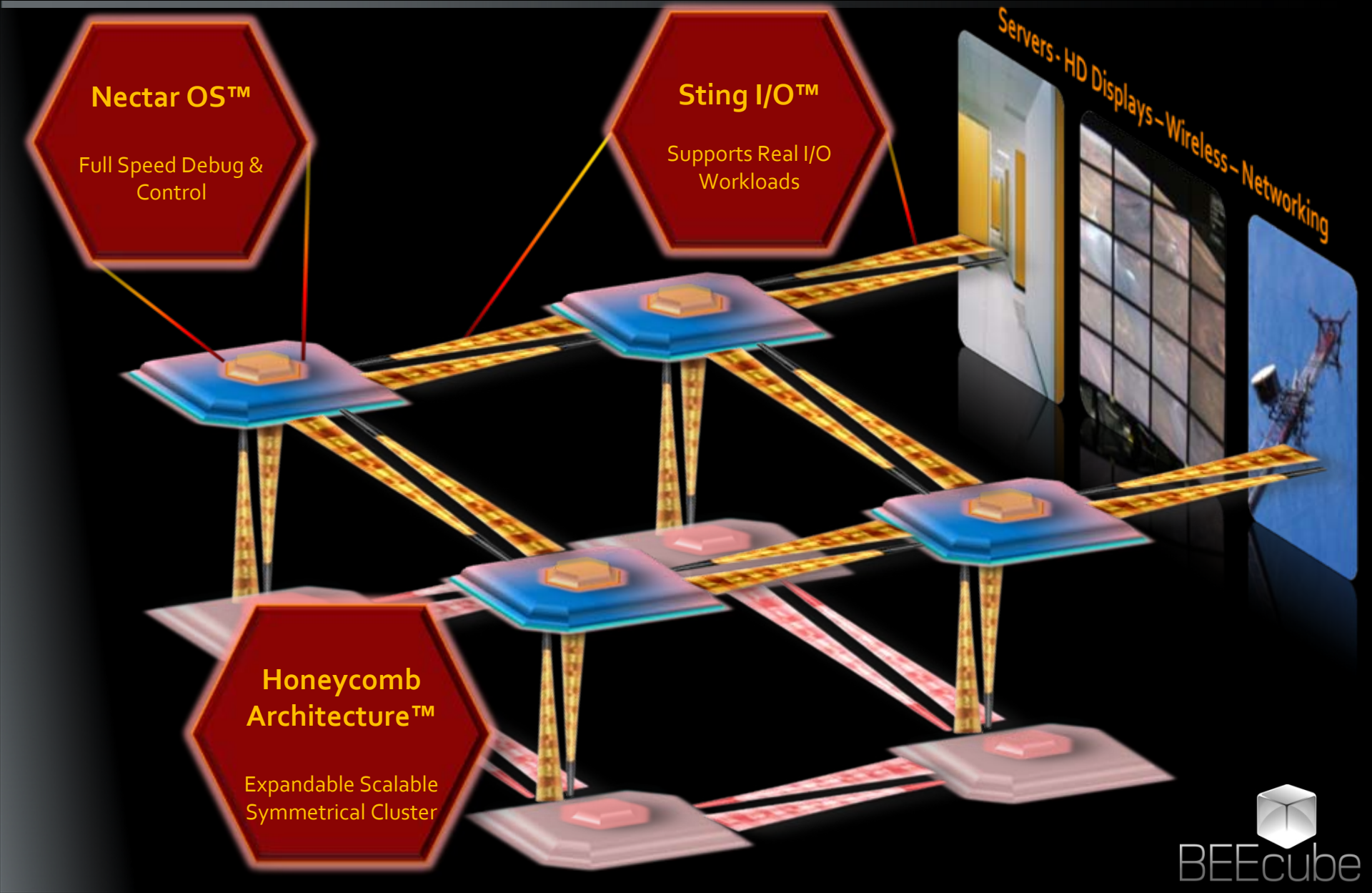
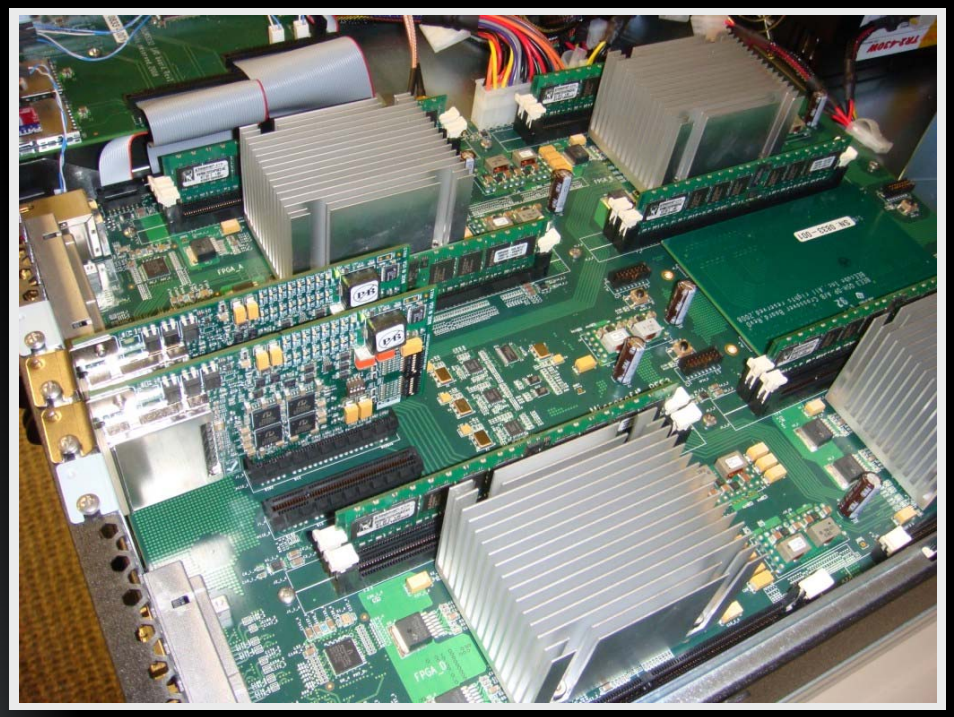
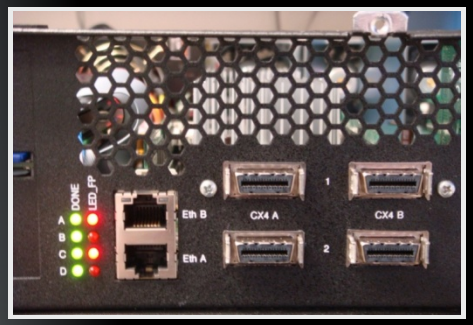
BEEcube Architecture



BEE3 Hardware Platform





- Quad Xilinx Virtex-5 FPGA signal processing
  - 5M gate capacity
  - Integrated DDR800 inter-FPGA ring bus
- 64GB DDR2 ECC DRAM
- Multiple high-speed data interfaces
  - 160 Gbps SERDES I/O
  - Quad x8 PCI Express
  - Quad 1000BASE-T Ethernet
  - Quad 40-pair LVDS QSH expansion slots

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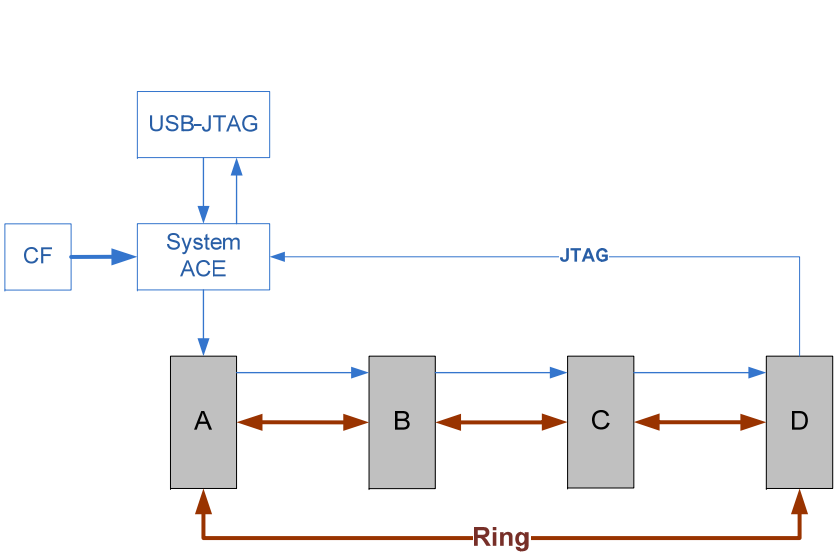
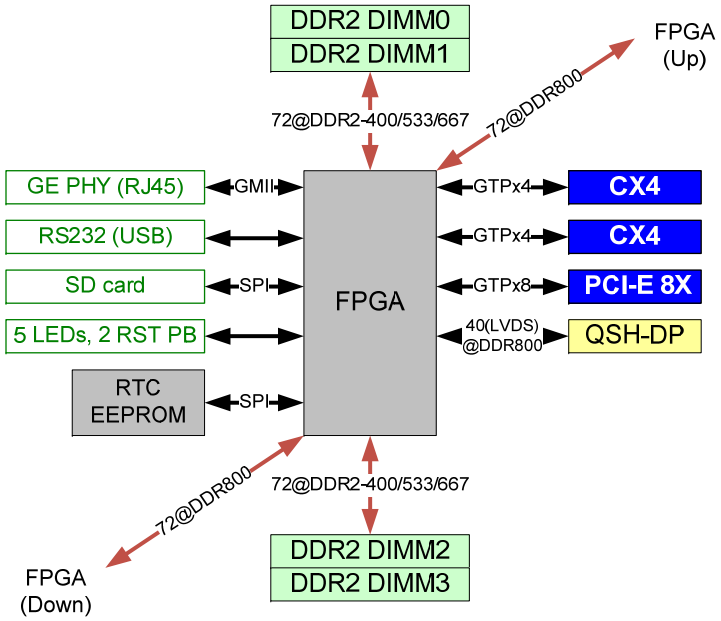
BEE3 Hardware Platform





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ADC Expansion Boards for BEE3

- Dual-channel 3 GSps model
  - Two National Semiconductor ADC083000 ADCs
  - Independent clock, data, reset, and trigger SMA inputs for each ADC
- Quad-channel 1.5 GSps model
  - Two National Semiconductor ADC08D1500 ADCs
  - Independent clock, I-data, Q-data, and trigger SMA inputs for each ADC

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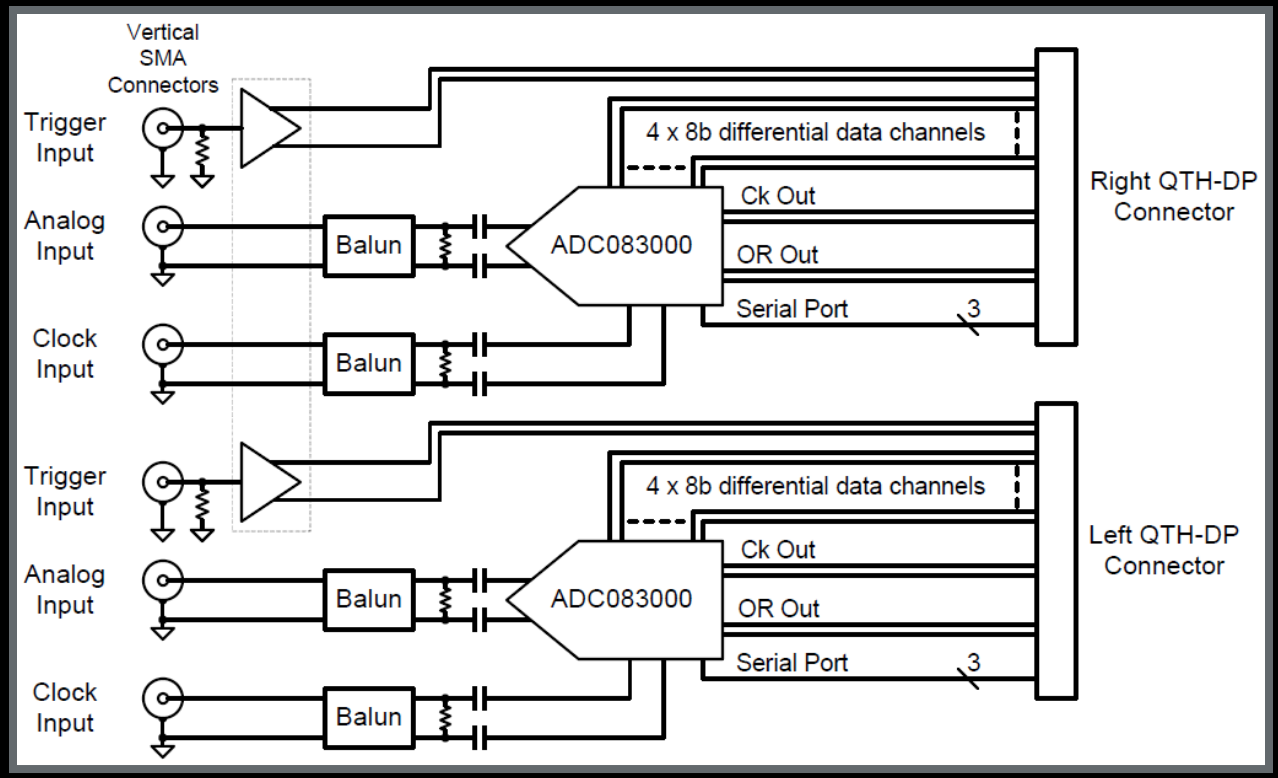
Dual 3 GSps ADC Board



- 8-bit resolution, one channel per ADC/FPGA
- Analog sample rate 1000-3000 MHz
- Balun input bandwidth 30-1800 MHz

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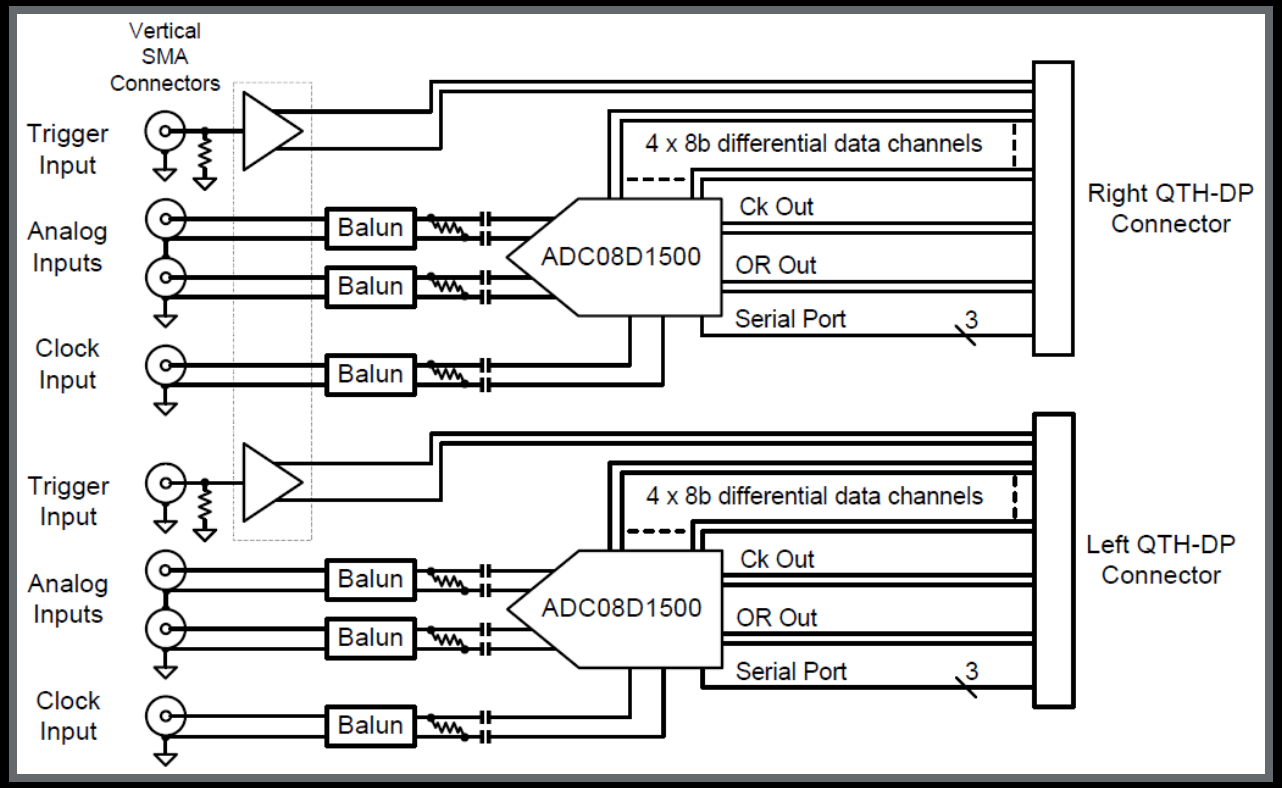
Quad 1.5 GSps ADC Board



- 8-bit resolution, two channels per ADC/FPGA
- Analog sample rate 200-1500 MHz
- Balun input bandwidth 30-1800 MHz

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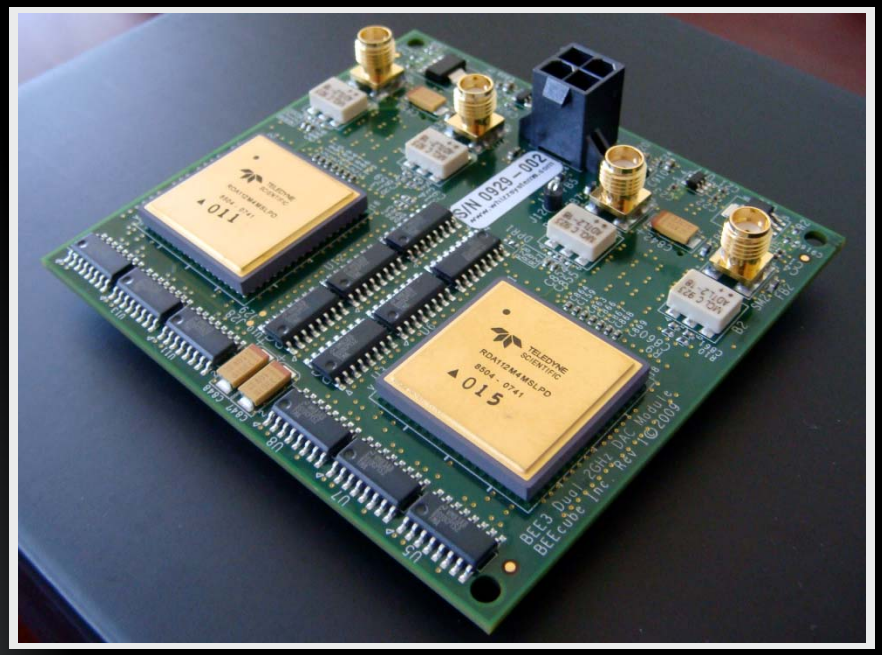
DAC Expansion Boards for BEE3



- Dual 2 GSps model
  - Teledyne RDA112M4MSLPD
  - Independent clock inputs and data outputs
- Factory configured in master-slave mode
- User-selectable resolution
  - 9-bit resolution up to 2 GSps (4:1 mux)
  - 12-bit resolution up to 1.5 GSps (2:1 mux)

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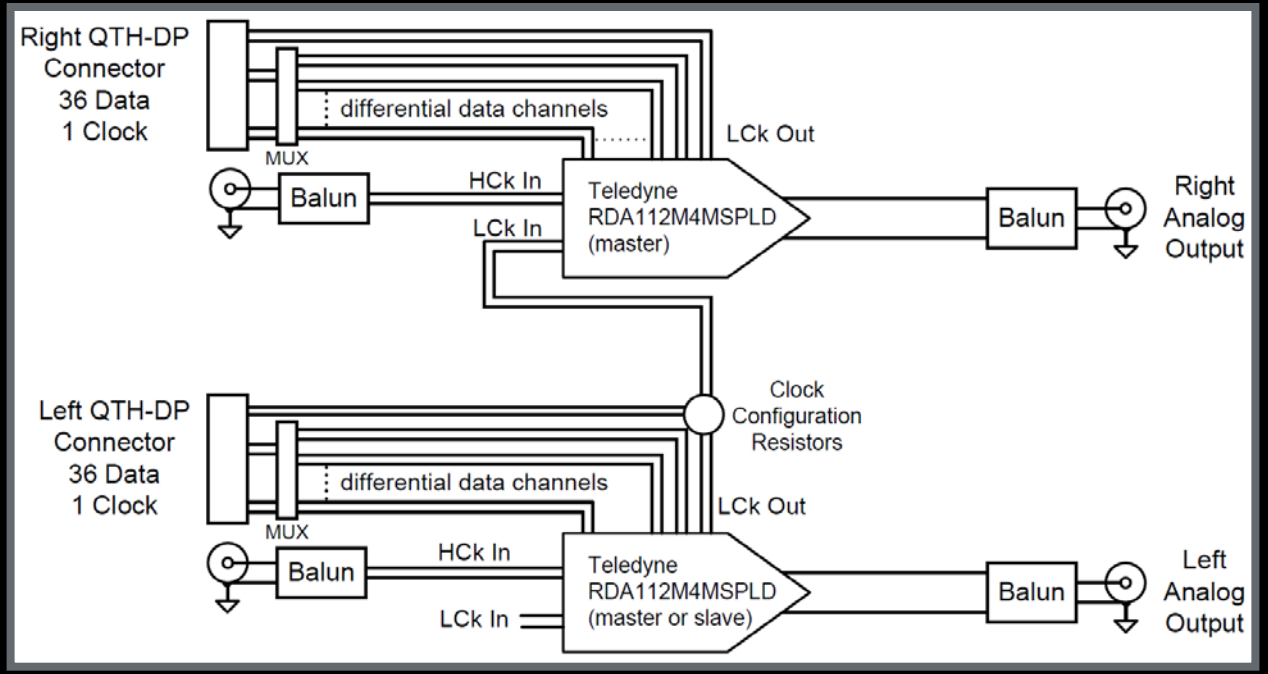
Dual 2 GSps DAC Board



- On-board muxes switch between 9-bit (4:1) and 12-bit (2:1) modes
- Nominal output level of 600 mV
- Configured for master-slave mode from factory

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SDR Reference Design

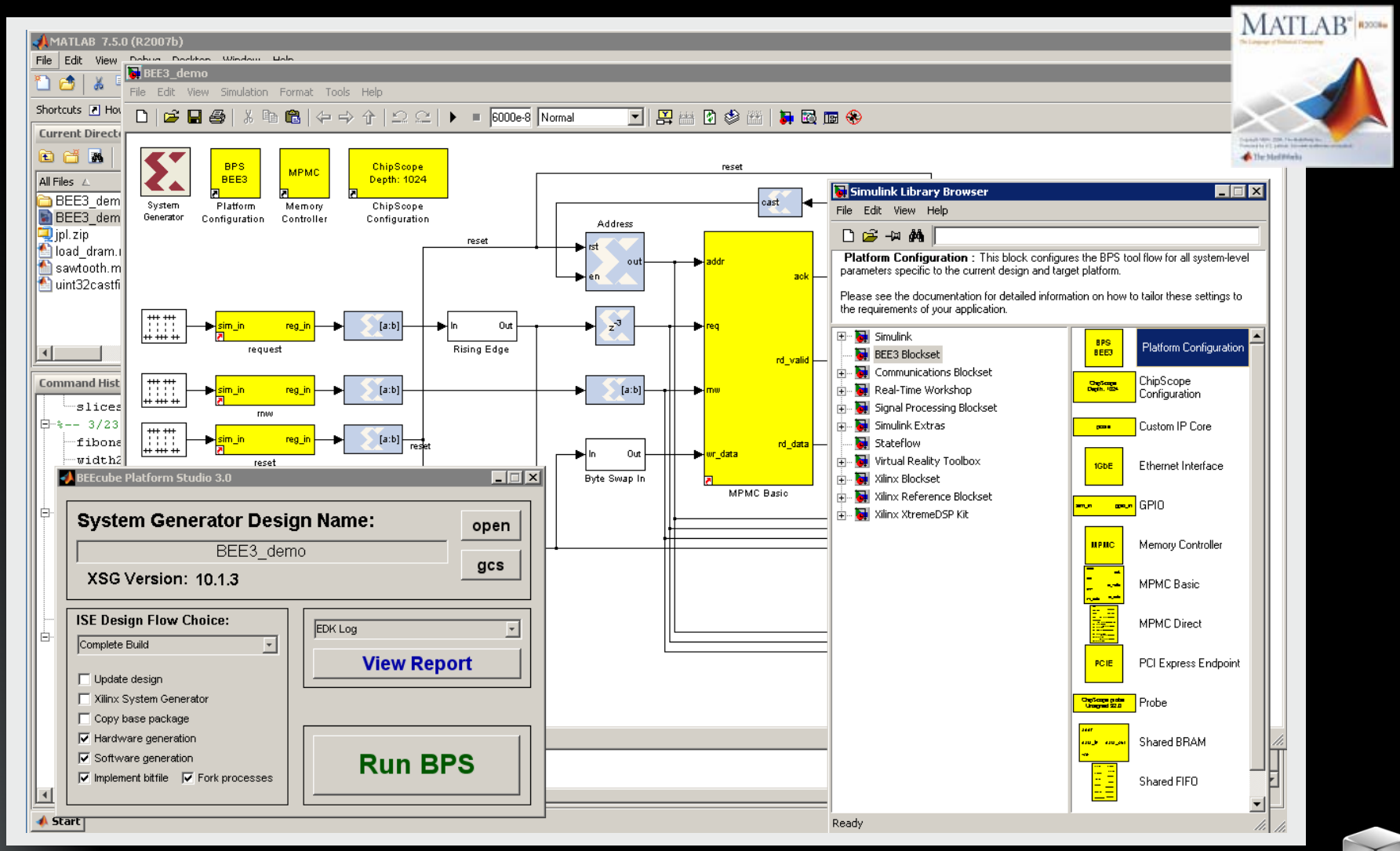
FPGA A

- 2 GSps DAC signal source
  - Carrier tone generated by FPGA-based numerically-controlled oscillator (NCO)
  - Arbitrary modulation pattern up to 16,384 samples contained in FPGA Block RAM (BRAM)

FPGA B

- 3 GSps ADC virtual oscilloscope
  - Data captured into FPGA BRAM in 16,384-sample windows
  - Captured data read via Ethernet or serial port into Matlab for direct analysis

BEEcube Platform Studio



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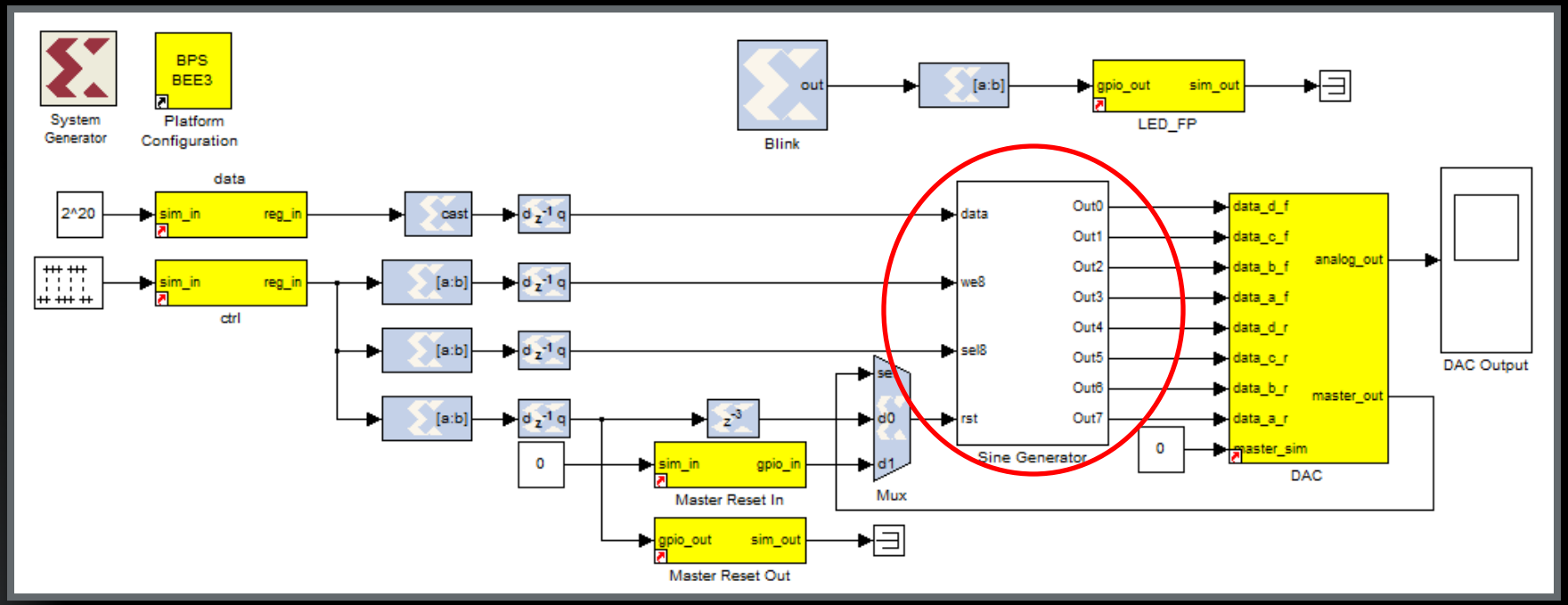
DAC Signal Source Model



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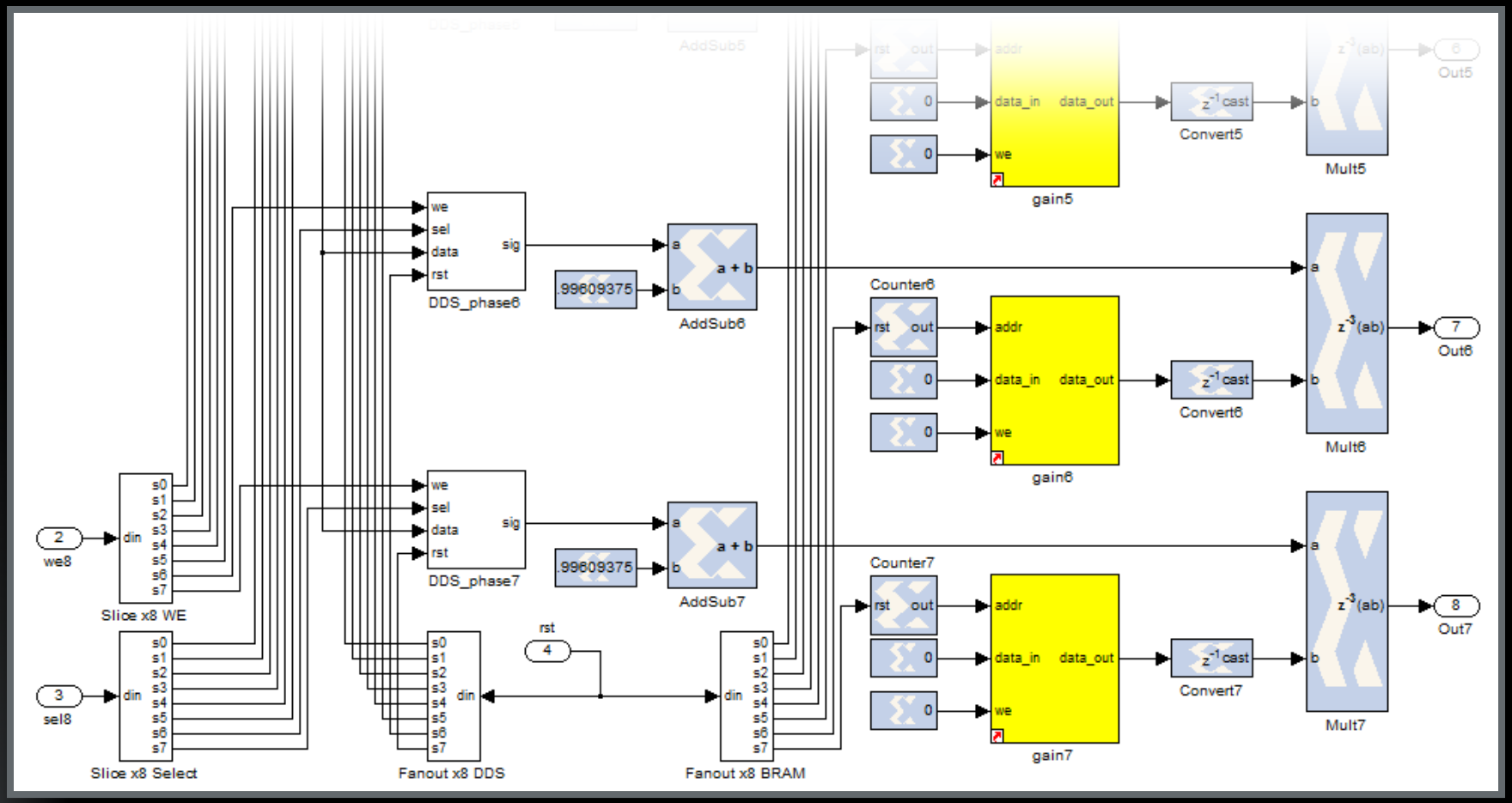
DAC Signal Source Model



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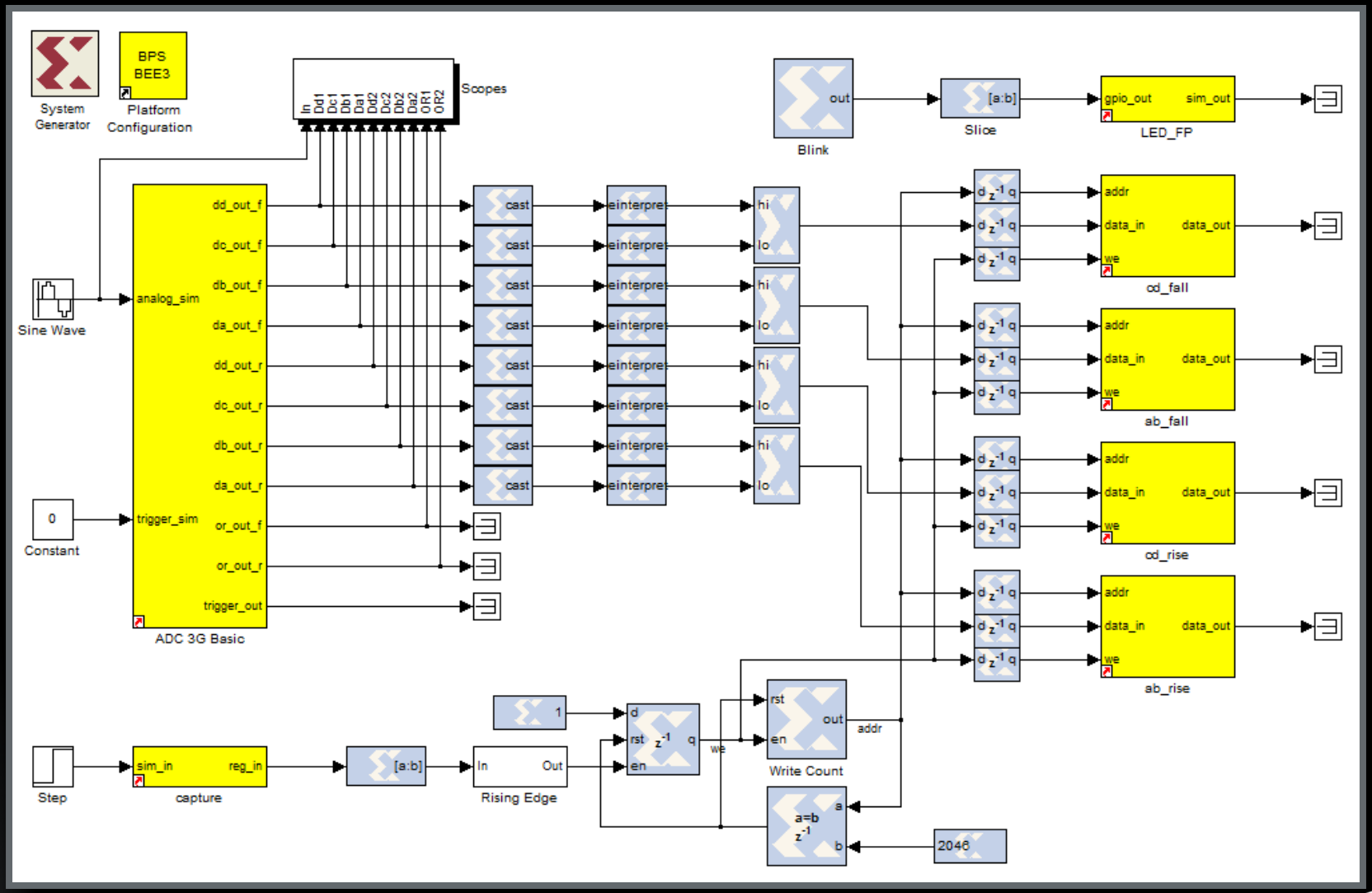
ADC Virtual Scope Model



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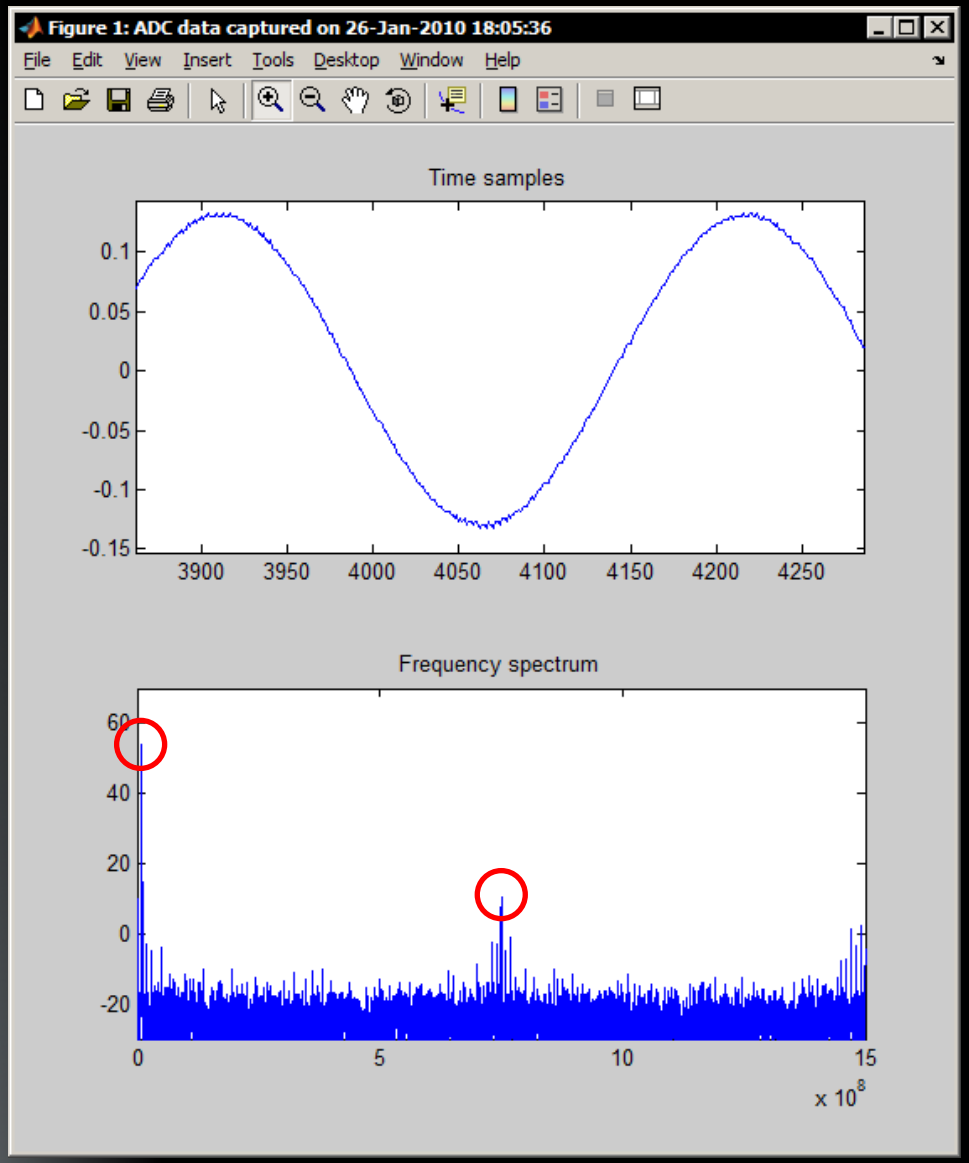
DAC Signal Source Performance

- FPGA system clock runs at 250 MHz
  - Enforced by DAC sample rate of 2 GSps, DDR signaling, and 4:1 mux ratio
- NCO implemented using Xilinx DDS cores
  - CoreGen “DDS Compiler v2.1” specification
  - Up to 20 bits signal output precision, SFDR up to 120 dB, Δf down to 0.02 Hz
- Total device utilization on SX95T:
  - NCO: 9bit output, 1Hz resolution, 54dB SFDR
  - 4% DSP48s, 21% BRAM, 21% Slices

ADC Virtual Scope Performance

- FPGA system clock runs at 375 MHz
  - Enforced by ADC sample rate of 3 GSps, DDR signaling, and 4:1 demux ratio
- Total device utilization on SX95T:
  - 1% DSP48s, 16% BRAM, 15% Slices

Overall System Performance



- Results for 10 MHz tone:
  - Carrier peak @ 53.90 dB
  - Largest spur @ 10.64 dB
  - SFDR = 43.26 dB

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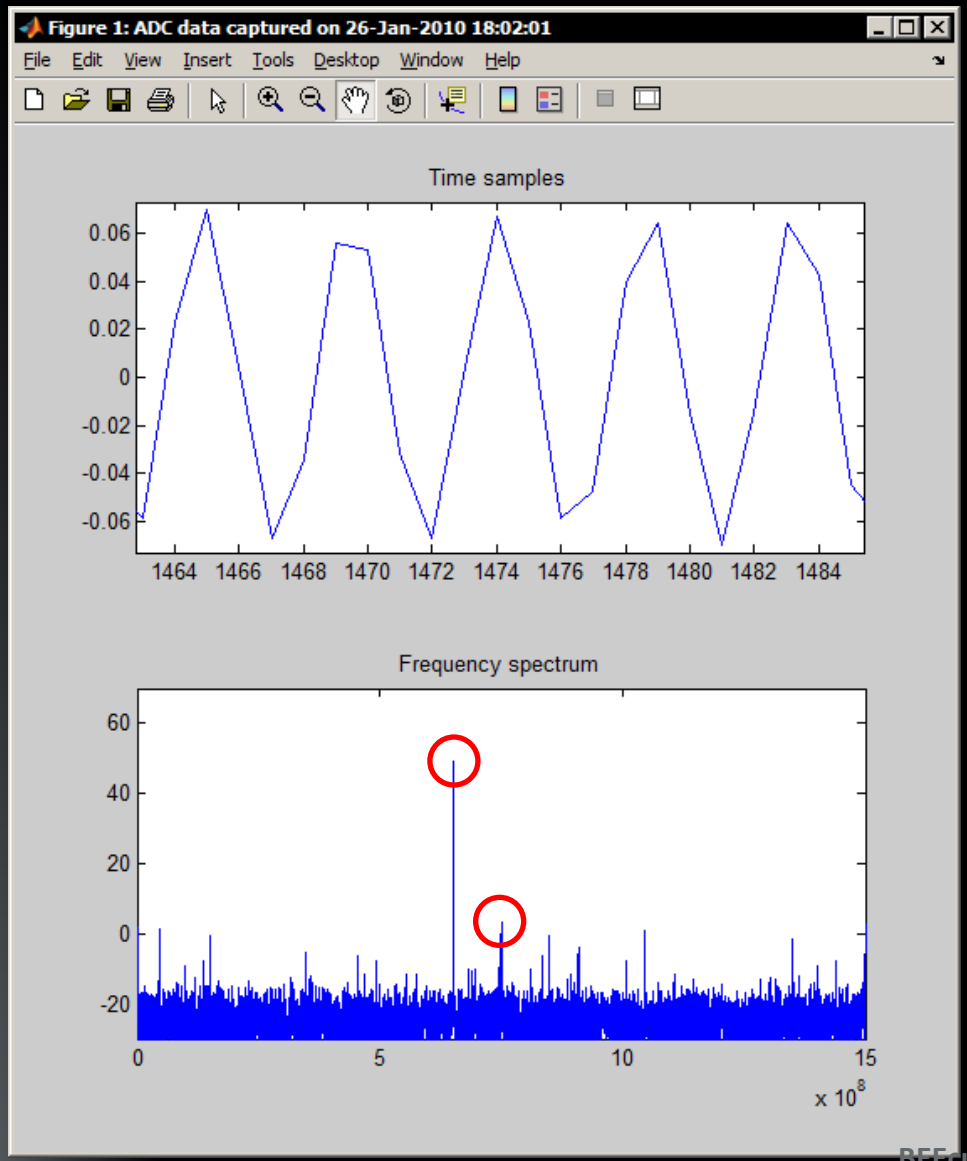
Overall System Performance



- Results for 667 MHz tone:
  - Carrier peak @ 49.1 dB
  - Largest spur @ 3.1 dB
  - SFDR = 46.0 dB

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Conclusion

- Using a Flexible Platform allows Adding “Intelligence” to Signal Handling and Information
- And Can be Applied to:
  - MIMO communication,
  - Radar Applications,
  - Signal Intelligence and Warfare