Full reconfigurable interleaver architecture for High-Performance SDR applications

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Interleaver in SDR applications

This paper presents several interleaver / deinterleaver architectures for SDR applications.

Full reconfigurable interleaver / deinterleaver characteristics.

- Allows to run several interleaving methods concurrently.
- Hard-bit and Soft-bit modes.
- Rate-Matching mode.
- Frame-Equalization mode.
- Very large permutation functions.

We propose Optimized interleaver cores for

- LTE turbo encoder interleaver.
- UMTS turbo encoder interleaver.

Reconfigurable IP Core, Basic Operation

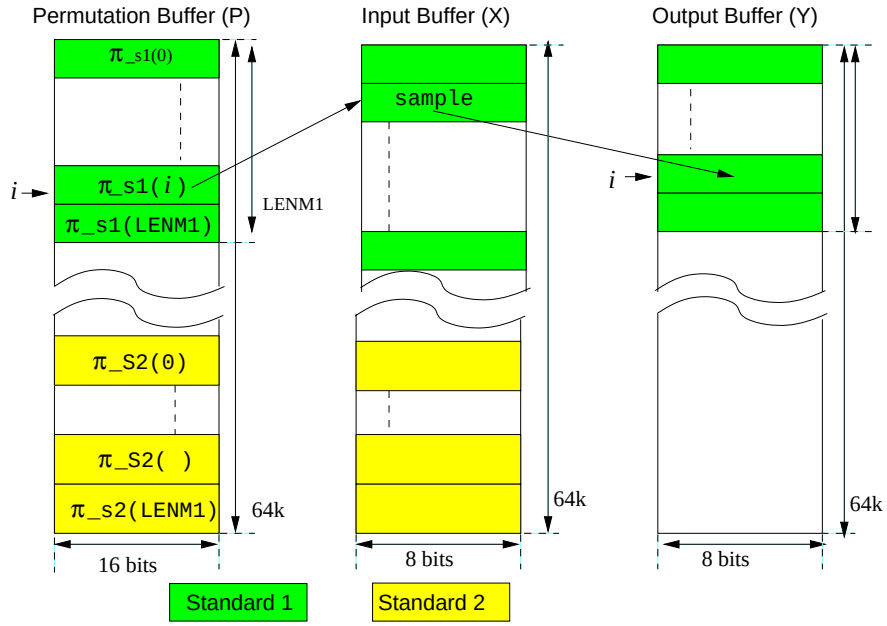
The memory is arranged in four distinct blocks, allowing access to two blocks simultaneously. This memory arrangement allows for implementation of any interleaving method to our knowledge.

Input buffer X 8bits wide.
$2^{16} = 65536$ entries.

Output buffer Y 8bits wide.
$2^{16} = 65536$ entries.

Permutation buffer $P = \pi(i)$.
16 bits wide.$2^{16} = 65536$

$$Y[i] = X[P[i]]$$



Advanced operation modes

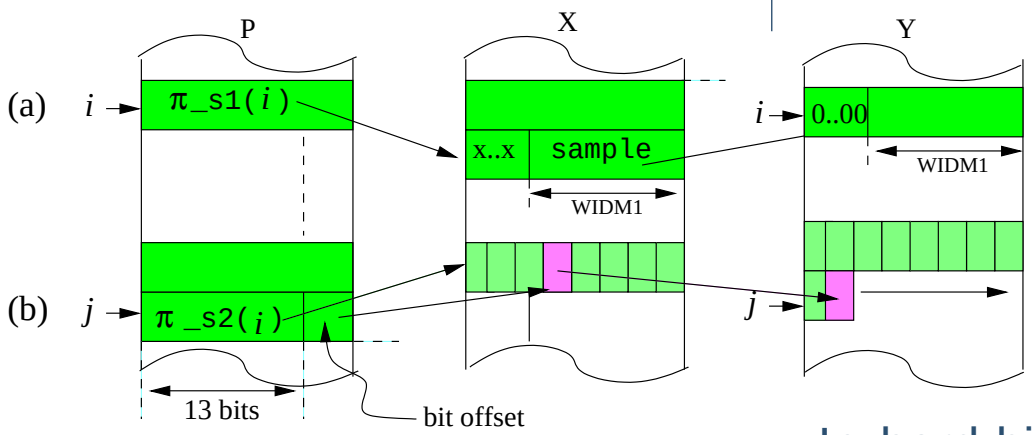
In order to mitigate the memory overhead we take benefit of flexibility and implement extra features like:

- Concurrent operation of several interleaving methods
- Soft bits and Hard bits
- Rate matching
- Frame equalization
- Large permutation functions
- Symbol mapping

Hard/Soft bits mode

Hard-bits and Soft-Bits

In soft-bits mode, the entries in IB are samples of 1 to 8 bits.

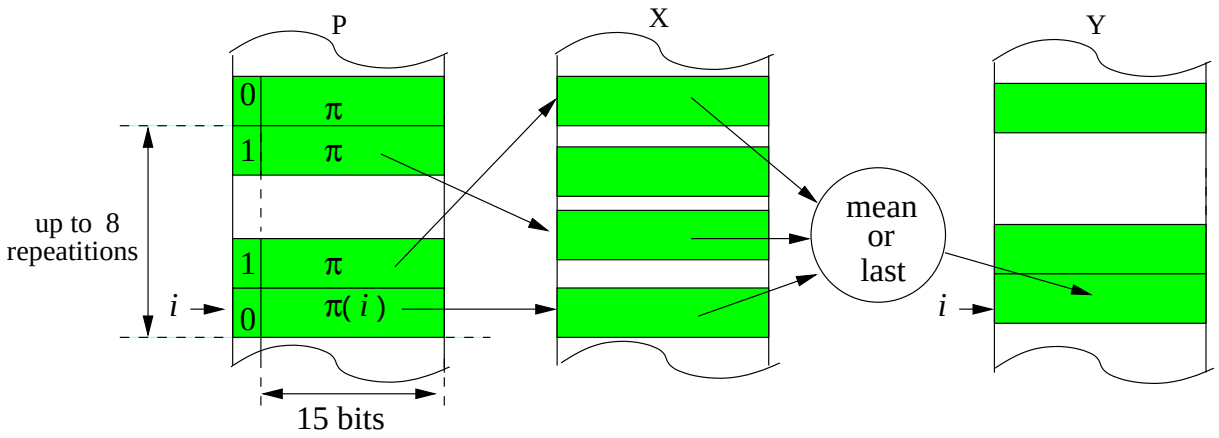


In hard-bits mode, each byte of the input or output buffer holds 8 different one-bit samples.

Entries in P in HBM is: the 13 MSBs are the byte offset in IB and the 3 LSBs the bit offset.

Rate-matching mode (optional)

The rate matching process is carried out so that the size of a block of samples matches the size of radio frames. It will either repeat bits to increase the rate or puncture bits to decrease the rate.



At transmission, omit or repeat entries in PB.

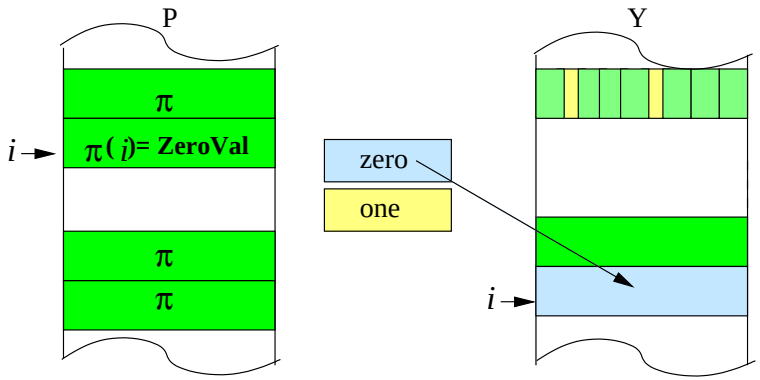
At reception, the first MSB of PB is considered as a repeat flag, and its 15 LSB are the offset of IB. There are two modes in reception: **average mode**, where it handles up to 8 repetitions at reception, and **Last-one mode** with no repetition limitations.

Frame-equalization mode(optional)

Frame equalization consists in adding stuffing bits to the data stream, either zeros or ones, with the purpose of ensuring that the output can be segmented into equal size segments to be transmitted in a TTI.

Special values of permutation entry are defined: **ForceZero** and **ForceOne**.

When encountered in the PB, then $Y[i] = 0, 1$



Other Advanced modes (optional)

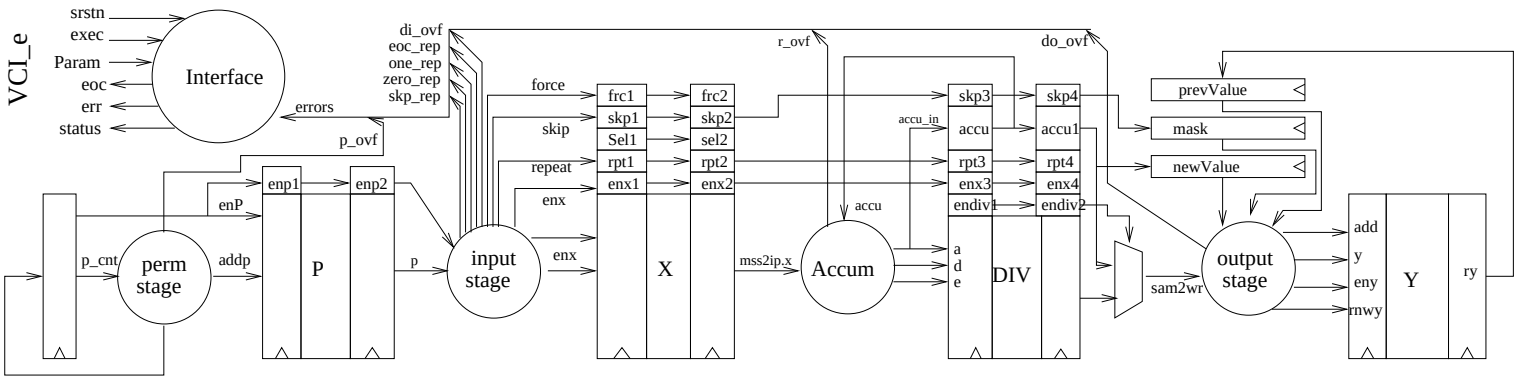
Very Large permutation table

Use of a third special value **SkipValue**. It allows skipping entries of the OB when encountered in the PB.

Symbol mapping in OFDM based standards

This interleaver has the flexibility to execute symbol mapping and demapping to/from OFDM carriers. Although the width of the input samples is not optimal for this purposes.

Architecture and System results



The address generation logic of this module was synthesized for a 130 nm CMOS standard cells library, its maximum speed is 350Mhz, but we require only 200Mhz. At 200Mhz the area consumption is of 0.02mm^2.
The 256 k-Bytes memory (about 0.85 mm^2 in 40 nm or 9 mm^2 in 130 nm) is a worst case. Most SDR platforms would require far less.

Optimized Interleaver cores

A generic, table-based, interleaver such as the one described in the previous section is not always the best solution, even in the SDR context.This is especially true in the channel decoder because the interleaver is used several times per iteration , frequently 5 to 10 per code word.

A dedicated, compact and energy efficient address generator, embedded directly inside the channel coder / decoder seams a much better solution.

This paper presents two optimized interleaver for:

- 3GPP UMTS turbo interleaver.
- 3GPP LTE turbo interleaver.

LTE turbo encoder interleaver

This module implements an address generator for the LTE turbo encoder and decoder as defined in 3GPP Multiplexing and channel coding document(36-212)[2]. is defined as:

$$\pi(i) = P(i) = (f_1 \times i + f_2 \times i^2) \bmod k \quad (1)$$

The parameters used by the module (α, β) are calculated in advance:

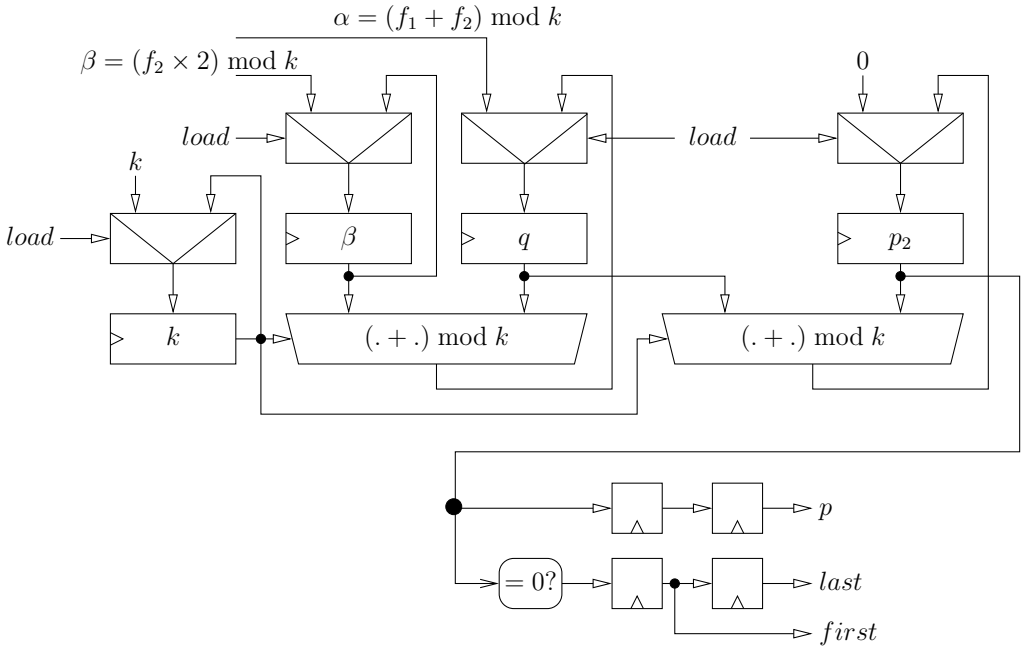
$$\begin{aligned} \alpha &= (f_1 + f_2) \bmod k \\ \beta &= (2 \times f_2) \bmod k \end{aligned}$$

The module computes the polynomial (1) incrementally:

$$\begin{aligned} P(i+1) &= f_1 \times (i+1) + f_2 \times (i+1)^2 \\ &= P(i) + f_1 + 2 \times i \times f_2 + f_2 = P(i) + Q(i) \\ Q(i+1) &= Q(i) + 2 \times f_2 = Q(i) + \beta \\ P(0) &= 0 \\ Q(0) &= f_1 + f_2 = \alpha \end{aligned}$$

Implementation

The sequence wraps around k naturally. $P(k) = P(0) = 0$ and $Q(k) = Q(0) = \alpha$.
Because $P(i), Q(i), \alpha, \beta$ are naturals less than k. The modulus k reduction is a comparison with k, or at most a subtraction by k.



UMTS turbo encoder interleaver

This module implements UMTS turbo encoder interleaver as defined in 3GPP 25-212 document, Multiplexing and channel coding(FDD)[1].
U sequences of elements constructed incrementally and stored in a shift register ($u^{(i)}$.
The j-th value of the $T(i)$-th U sequence is:

$$U_{T(i)}(j) = s((j \times r_{T(i)}) \bmod (p-1)) = (v^{(j \times r_{T(i)}) \bmod (p-1)}) \bmod p$$

Fermat's little theorem allows to rewrite this expression as:

$$U_{T(i)}(j) = (v^{j \times r_{T(i)}}) \bmod p = (v^{j \times q_i}) \bmod p = \left(\frac{x_i}{256}\right)^j \bmod p$$

From which it comes:

$$U_{T(i)}(0) = 1$$

$$U_{T(i)}(j \neq 0) = \left(U_{T(i)}(j-1) \times \frac{x_i}{256}\right) \bmod p = \overline{\times}(U_{T(i)}(j-1), x_i, p)$$

where $\overline{\times}(a, b, p)$ is an 8 bits modular Montgomery multiplication:

$$\overline{\times}(a, b, p) = \left(\frac{a \times b}{256}\right) \bmod p$$

Architecture and Synthesis results

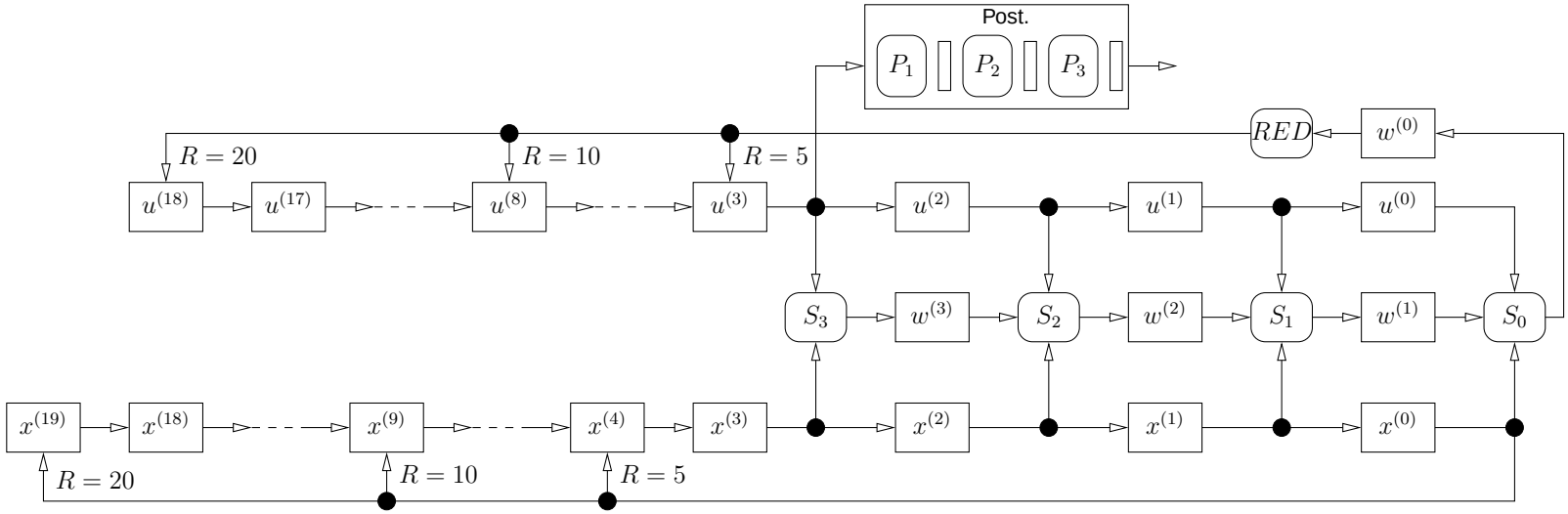


Table 1: Design Results comparison

Design	Process	Standards	Area (mm^2)	Freq (MHz)
Design[4]	180 nm	UMTS	0.24	130
Design[3]	90 nm	UMTS, LTE	ND	ND
This work	130 nm	UMTS, LTE	0.044	350

Questions??

questions

Bibliography

[1] 3GPP. Multiplexing and channel coding (fdd), 25-212 rel 920.

[2] 3GPP. Evolved universal terrestrial radio access (e-utra); multiplexing and channel coding, 36-212 rel 920.

[3] ASGHAR, R., AND LIU, D. Dual standard re-configurable hardware interleaver for turbo decoding. In *Wireless Pervasive Computing, 2008. ISWPC 2008. 3rd International Symposium on* (7-9 2008), pp. 768 –772.

[4] WANG, Z., AND LI, Q. Very low-complexity hardware interleaver for turbo decoding. *Circuits and Systems II: Express Briefs, IEEE Transactions on 54*, 7 (july 2007), 636 –640.