Digital Data Innovations

DDI

Data Packet Processor (DPP) Core

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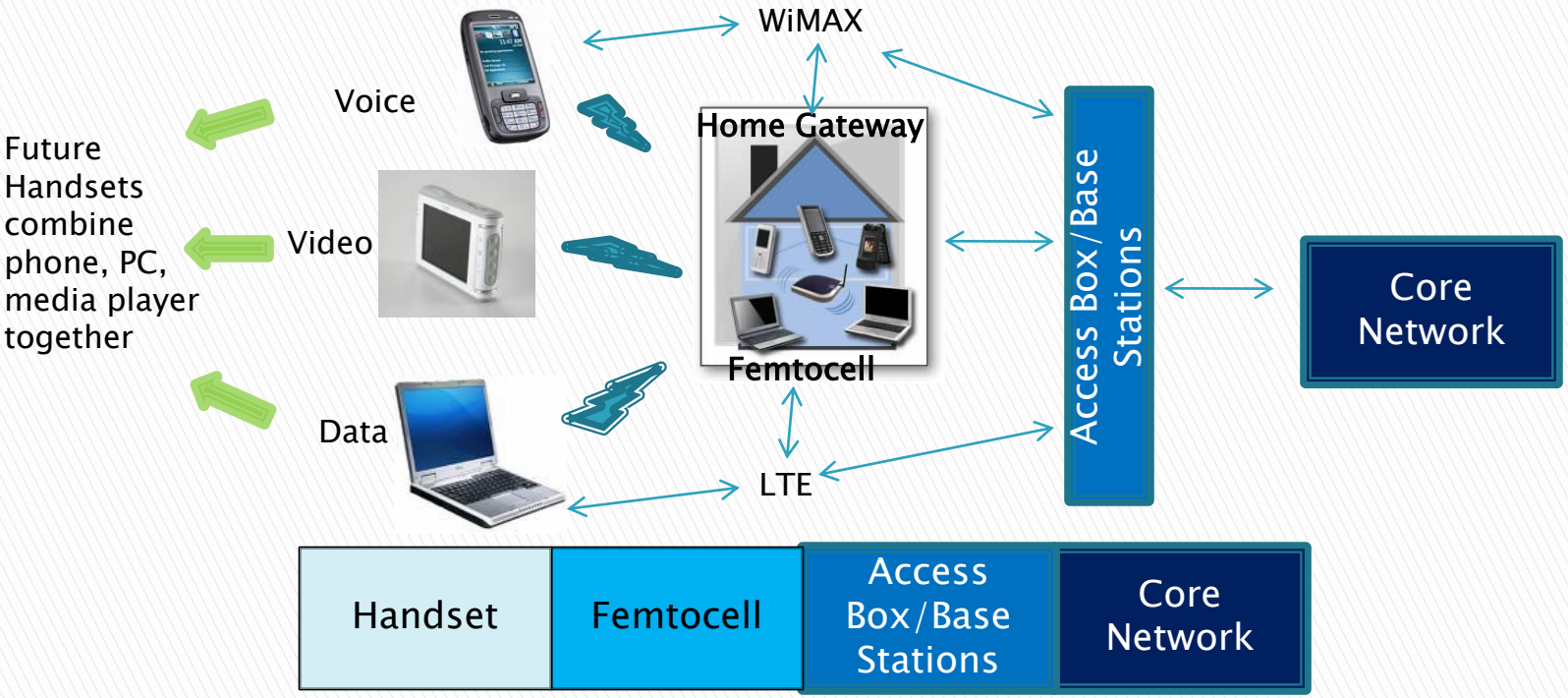
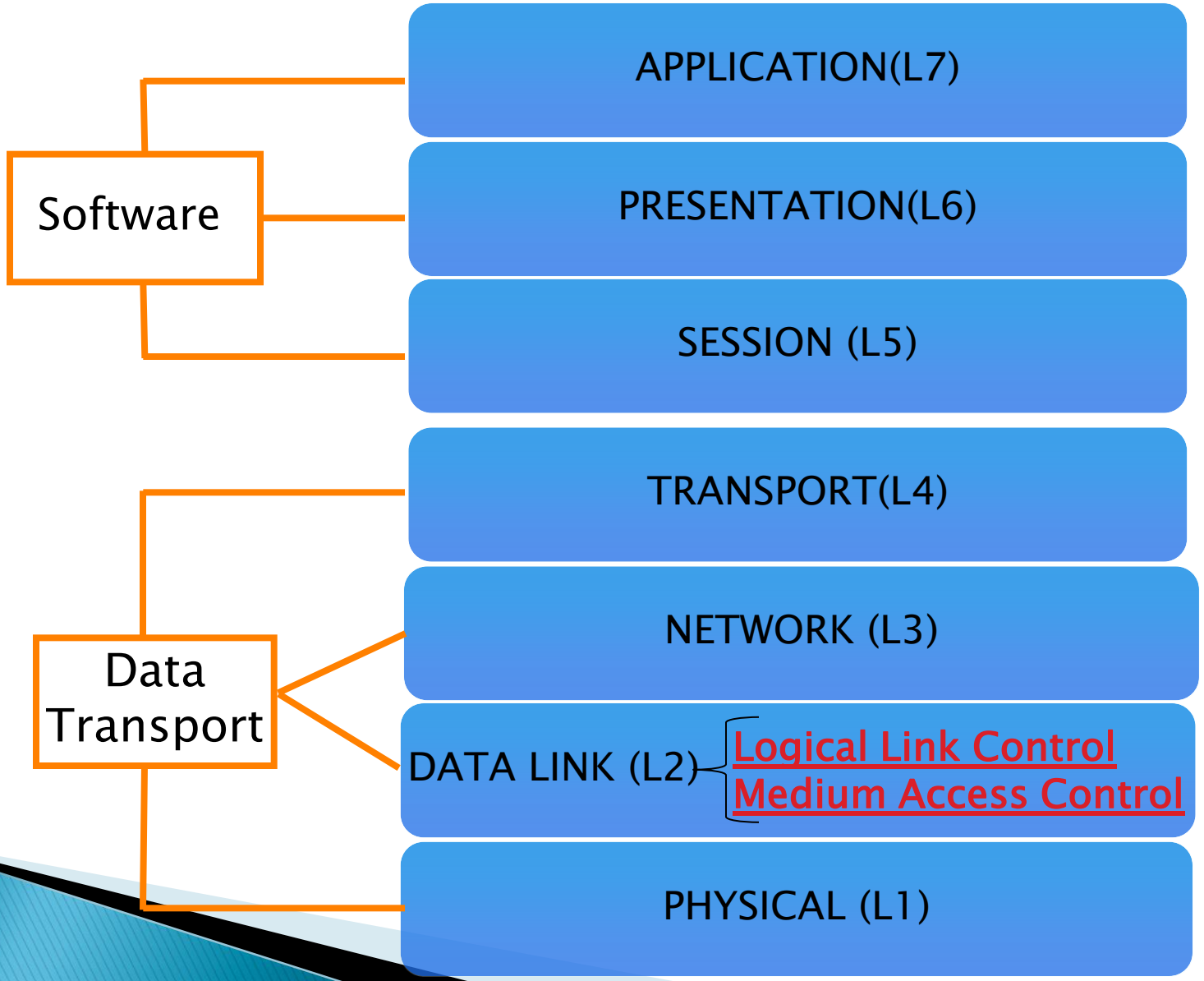
Digital Communications Challenges

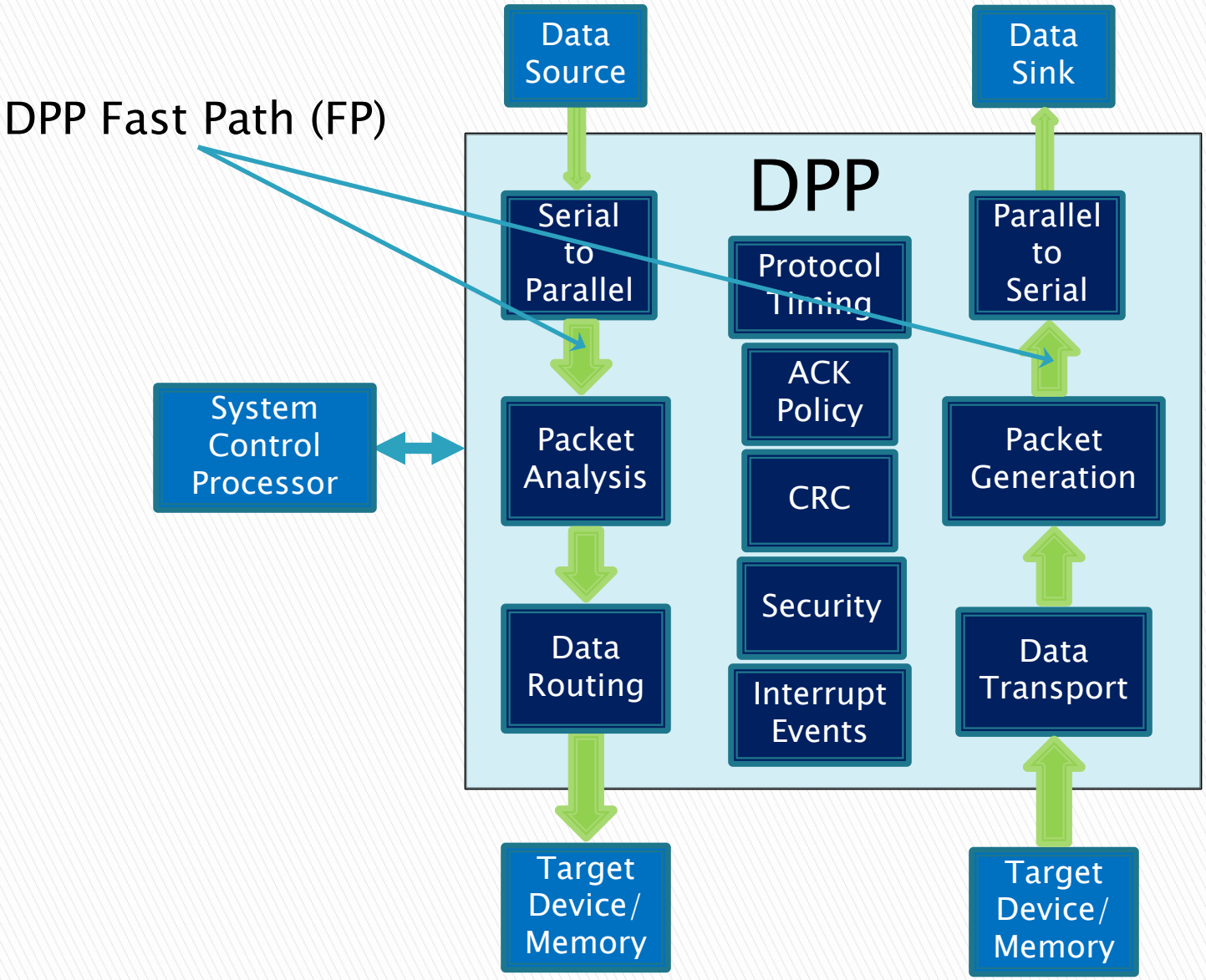
- Converging world (voice, data/text, media/video)
- Multi-standards (all in one)
- Support for changing emerging standards
- Proprietary protocol
- Efficiency: Power, Area, Speed, Throughput, Cost
- Differentiation
- Agility



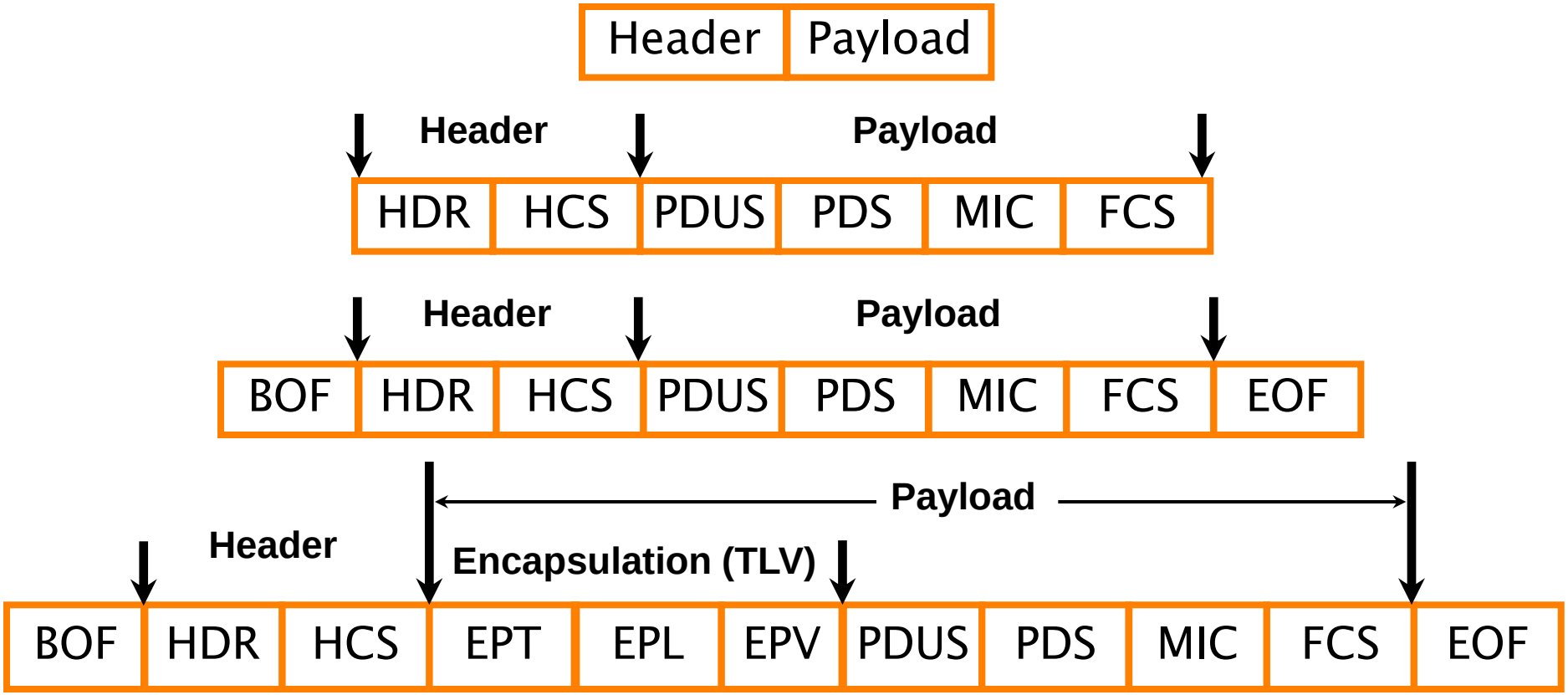
DPP Solution in the OSI Model



DDI's Data Packet Processor (DPP) System Diagram



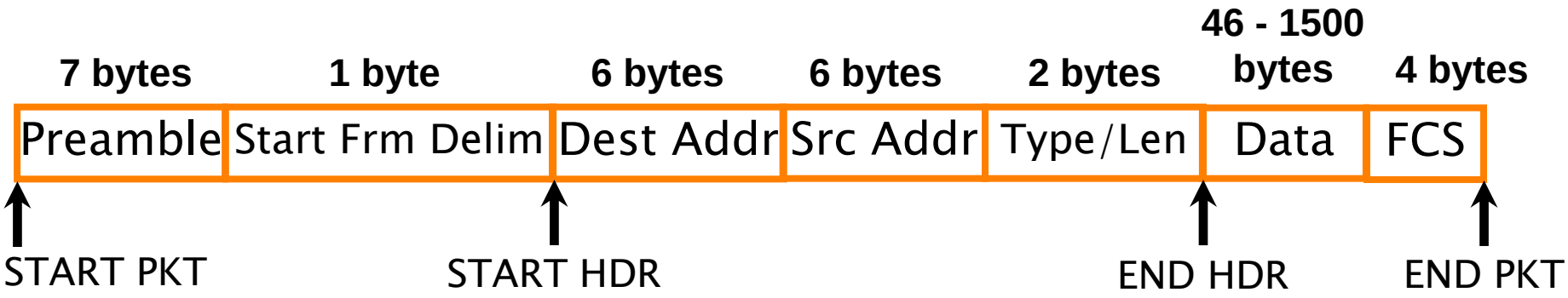
Breakdown Of A Data Packet



!!! THE DATA PACKET HAS BEEN ABSRACTED !!!

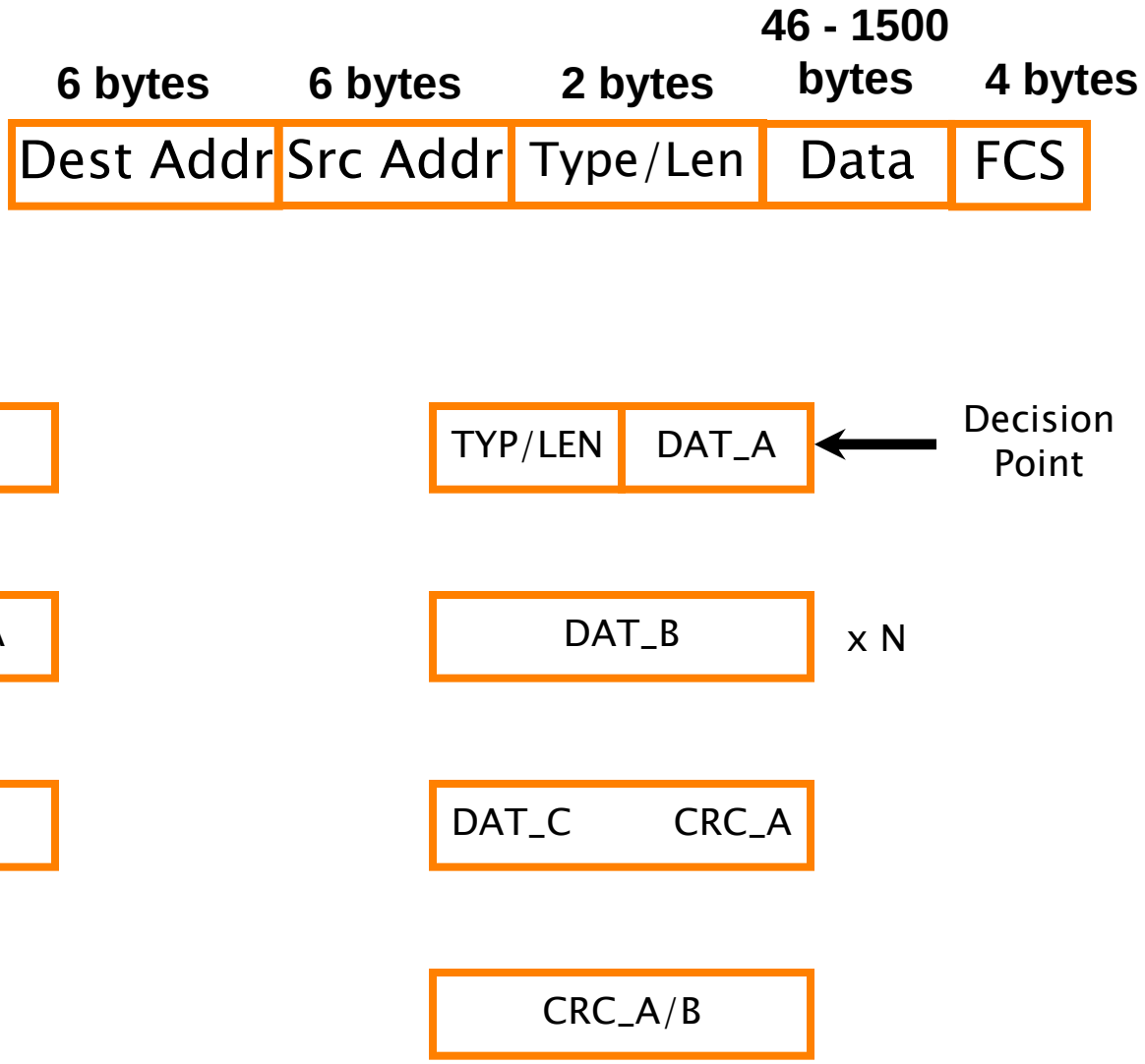
Example Packet Format (Ethernet)

Ethernet Packets:



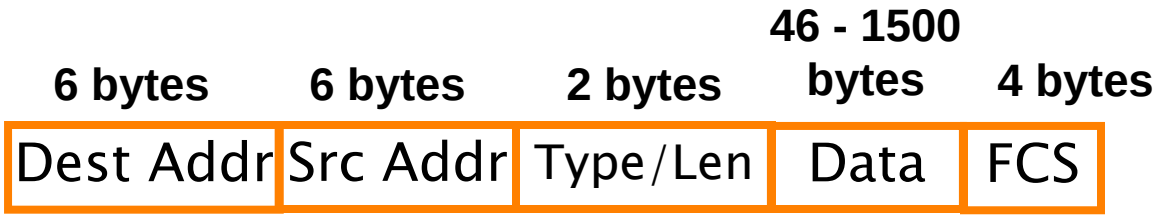
Example Packet Format (Ethernet)

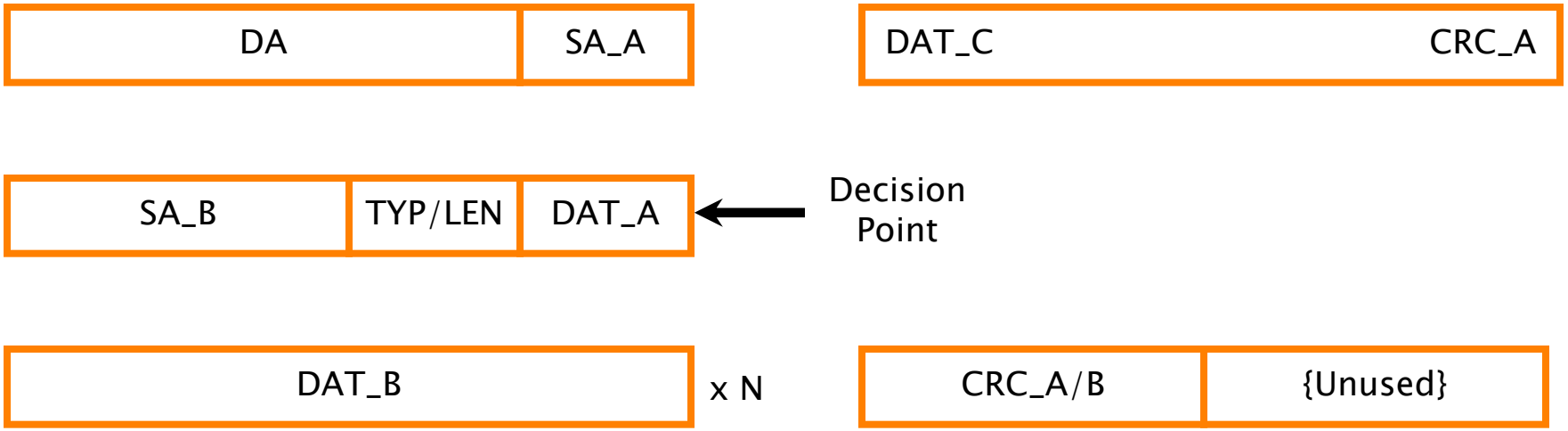
Fast Path @ 32-Bits:



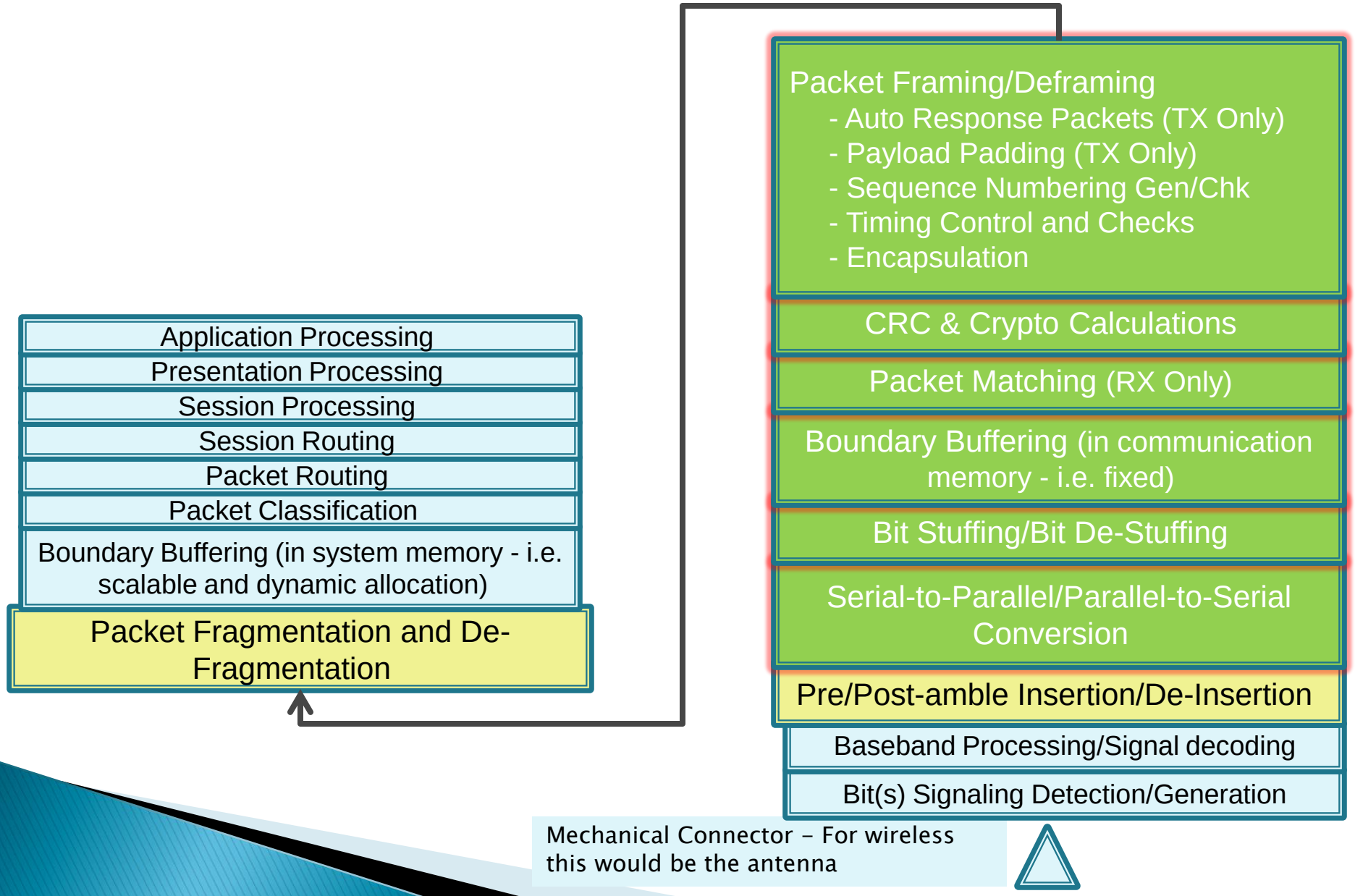
Example Packet Format (Ethernet)

Fast Path @ 64-Bits:





DPP and MAC Data Sequencing



DPP High Level Requirements

Control Path	▸ Support for Full/Half Duplex ▸ Provides bit level granularity ▸ Enhanced Interrupt Support ▸ Configurable CRC module
Data Path	▸ Isolated data transaction bus from control & status register accesses ▸ Supports a MAC-PHY interface that uses from 1 to N bits
Timing Path	▸ Abstracted and independent (Rx + Tx) packet timing control

DPP Flexible Features

- Protocol-Agnostic:
  - Supports standard protocols (e.g. WiFi, WiMax, LTE, Ethernet, PCIe, USB, Zigbee) and **custom** protocols
- Highly Programmable:
  - Packet structure specific microcode, MAC-PHY I/O Interface, CRC size, and other parameters are under program control
- Scalable Architecture:
  - Supports dynamic allocation of work registers, execution paths, and dynamic microcode decoding.
- Configurable:
  - # of Encryption bits, levels of CRC programmability, full/half duplex operation
- Bit-level granularity throughout architecture

Any Questions?