EXPERIMENTAL RESULTS ON ALL-DIGITAL IMPLEMENTATION OF THE PHASE LOCKED-LOOP FOR SOFTWARE-DEFINED RADIO

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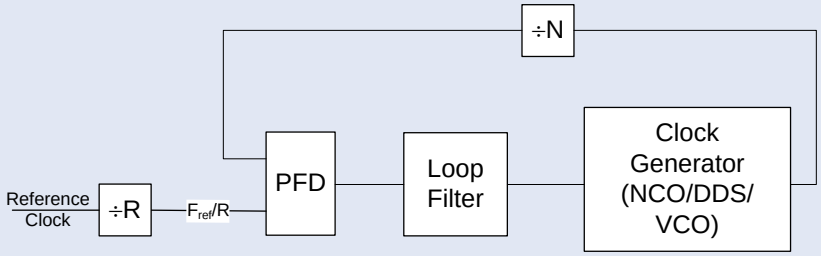
Agenda

- Introduction
- Proposed Design
- HW performance results
- Conclusion

Introduction

- Software-Defined Radio require a system with high flexibility.
- Many ways to design a good SDR system. All-digital approach with fixed sampling clock is the most preferred choice.
- The work presents an approach to generate purely digitally a clock that is synchronous with a reference clock.
- It is a combination of a PLL and DDS, thus it contains the merits from both techniques.

Overview



	Analog	Digital
Phase noise and Jitter	Excellent	Relative good
Size and Cost	More	Less
Sensitivity to environmental variations	Yes	No
Parameter control	Slow	Very fast

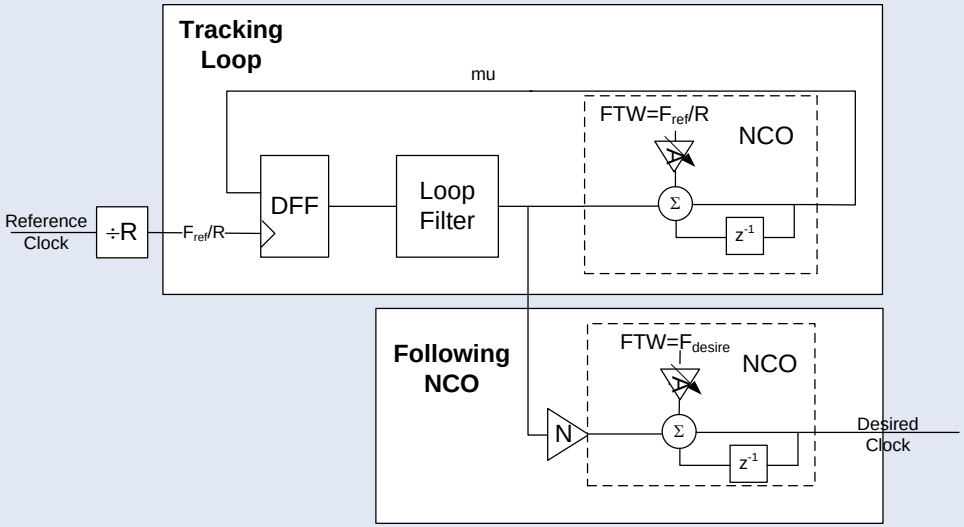
Overview (cont)

Source	Technology	Jitter Performance
VCO	Analog	<1ps
Xilinx embedded PLL	Analog	~ 100 ps
Altera embedded PLL	Digital	190 to 250 ps
ADI PLL-DDS	Hybrid	<1ps

- Any common ground between two approaches?

Proposed Scheme

Overview



- The PFD process is now imbedded in the NCO
  - So no extra circuitry is needed.
- D Flip Flop:
  - Since the NCO count value “mu”, represent the current phase of the NCO and the D Flip-Flop (DFF) will latch the phase error w.r.t the reference phase on the rising edge of the reference clock.
- New Approach:
  - Instead of converting the phase error into a pulse and then integrating with the loop filter and averaging; we obtain the exact phase error from the NCO “mu”.

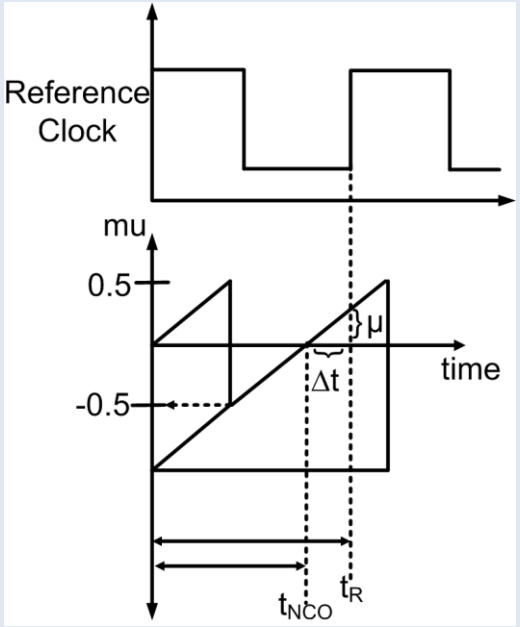
Concept of Operation

EQUATION DERIVATION

- Rule of rectangle triangles help in understanding the process
- The ratio of sides being equal give rise to some interesting formula

$$\frac{t_{NCO}}{1} = \frac{\Delta t}{\mu} = \frac{t_R - t_{NCO}}{\mu}$$

$$t_R = t_{NCO}(1+\mu)$$



Concept of Operation

Fast Frequency Estimation

$$\Delta R_{adjust} = \frac{\Delta R}{1+\mu} = A.\Delta R$$

- Increase the capture range
- Frequency estimation can include a method to re-calculate the nominal FTW,
- Reference frequency error can be corrected such that the frequency error can be set to be in the capture range

Concept of Operation

Frequency Tracking

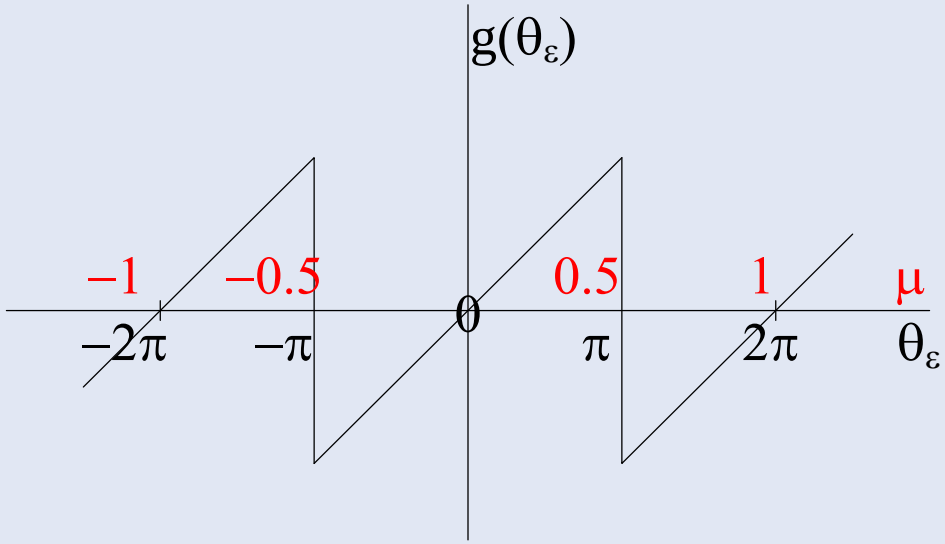
$$\Delta R_{n+1} \cong \Delta R_n (1-\mu), \mu \ll 1$$

- Increase the capture range
- Frequency estimation can include a method to re-calculate the nominal FTW,
- Reference frequency error can be corrected such that the frequency error can be set to be in the capture range

Properties of tracking loop

Basic

- Un-biased estimation
- S-curve for the PD predicts a large tracking range



Properties of tracking loop

Taylor Series Approximation

- Taylor Series Expansion
- Figure shows that the approximation is valid only for small values of "μ"<< 0.1
- The approximation does not crossover, i.e. should not impede the DPLL behavior

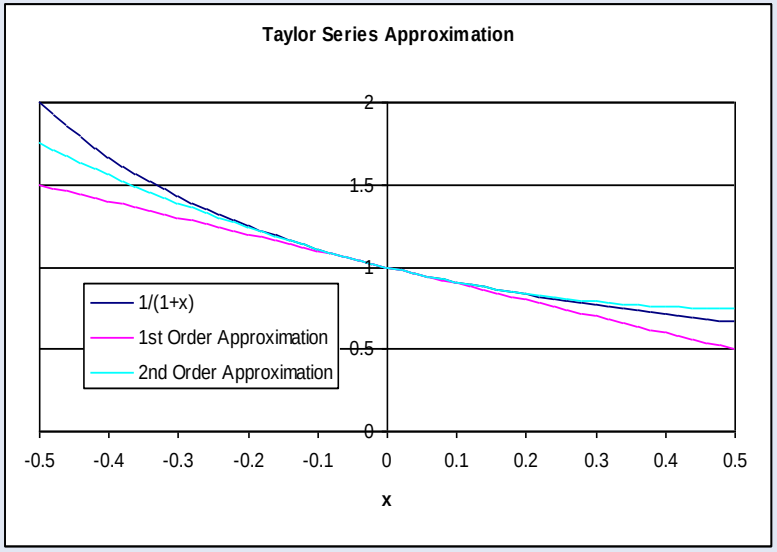
$$\frac{1}{1-x} = 1 + x + x^2 + x^3 \ldots = \sum_{n=0}^{\infty} x^n \; for \left|x\right| < 1$$

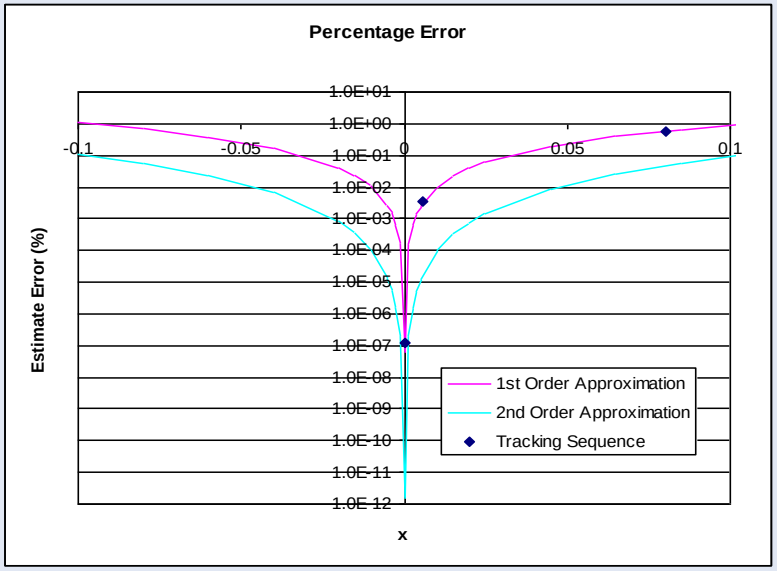
$$x = -\mu$$

$$\frac{1}{1+\mu} \xrightarrow{Taylor\_series\_expansion} 1 - \mu + \mu^2 - \mu^3 \ldots$$

$$Approximation:$$

$$\frac{1}{1+\mu} \approx 1 - \mu$$





Properties of tracking loop

Loop Behavior

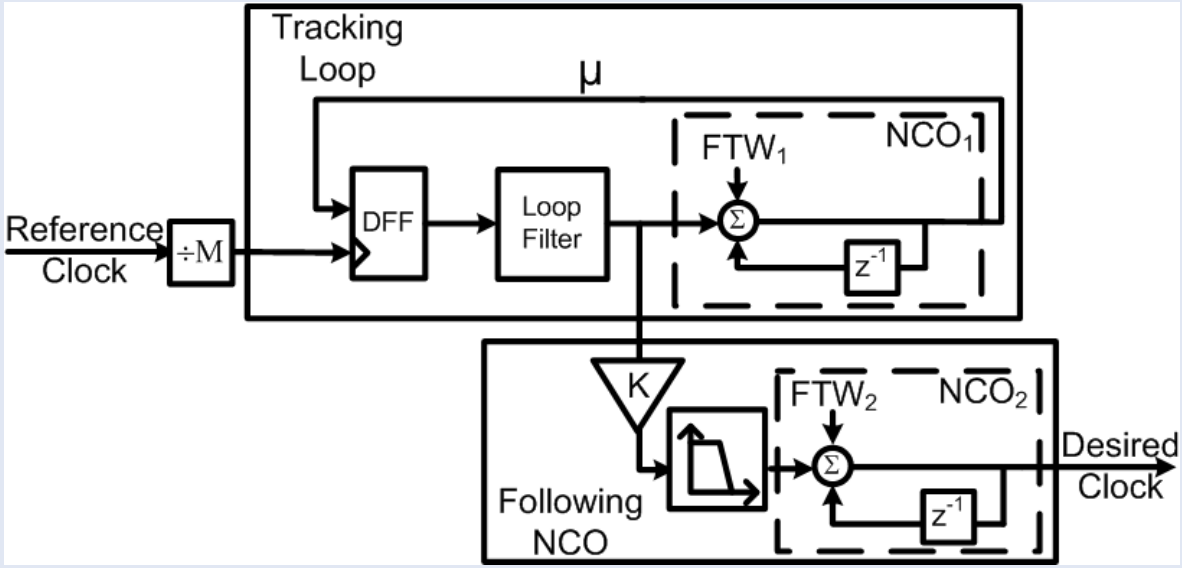
- Can use the standard feedback loop

- First Order Loop
  - Simple to implement
  - Not recommend for designs required low jitter

- Second Order Loop
  - Improve the reference jitter transfer function

Novel Phase Noise Shaping Technique

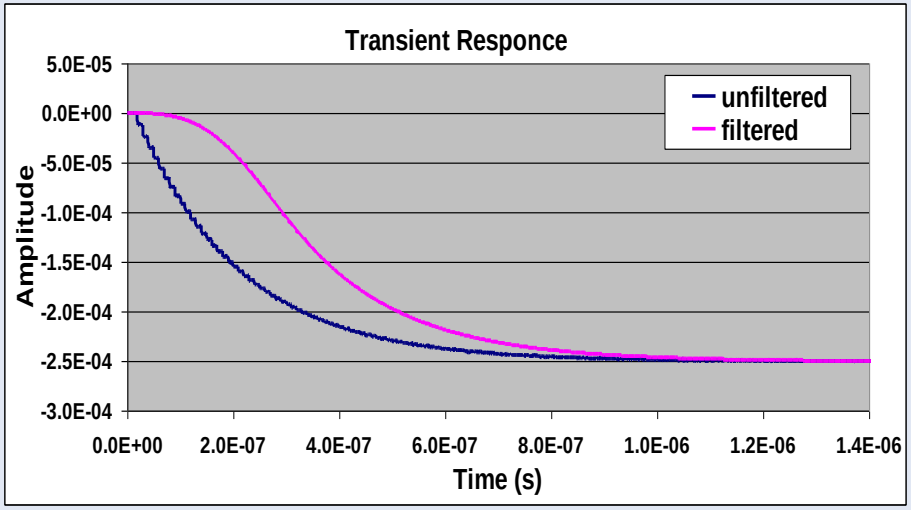
- Addition of an FIR filter
  - Design condition: Sum of all coefficient shall be unity
    - Permits DC signal to remain un affected
- Deterministic nature of the system
  - The transient behavior is decoupled from the Noise shaping
  - Novel: No longer need to trade-off Reference Noise vs. Settling time

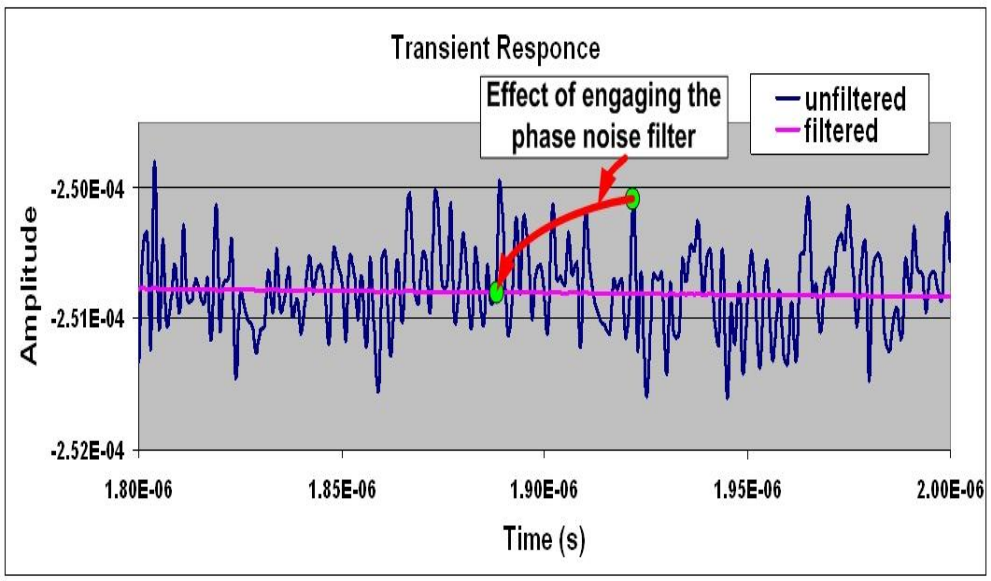


Simulation Results: Matlab Simulink

Loop Behavior

- FIR Introduced Delays
  - Dependent on the number of coefficients
- Effect of Added filtering

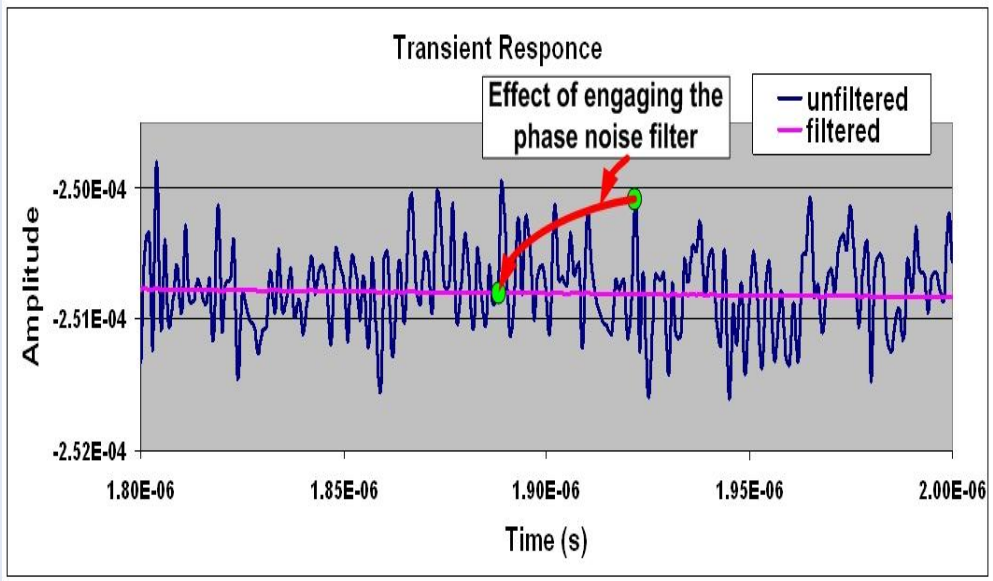


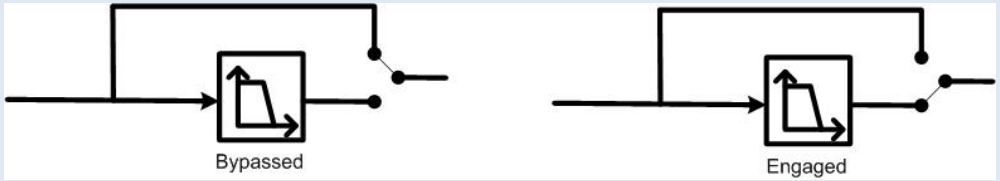


Optimized: Loop Response

Algorithm

- We are able to minimize the FIR impact on the loop response
  - Once lock is detected we can switch to the filter output

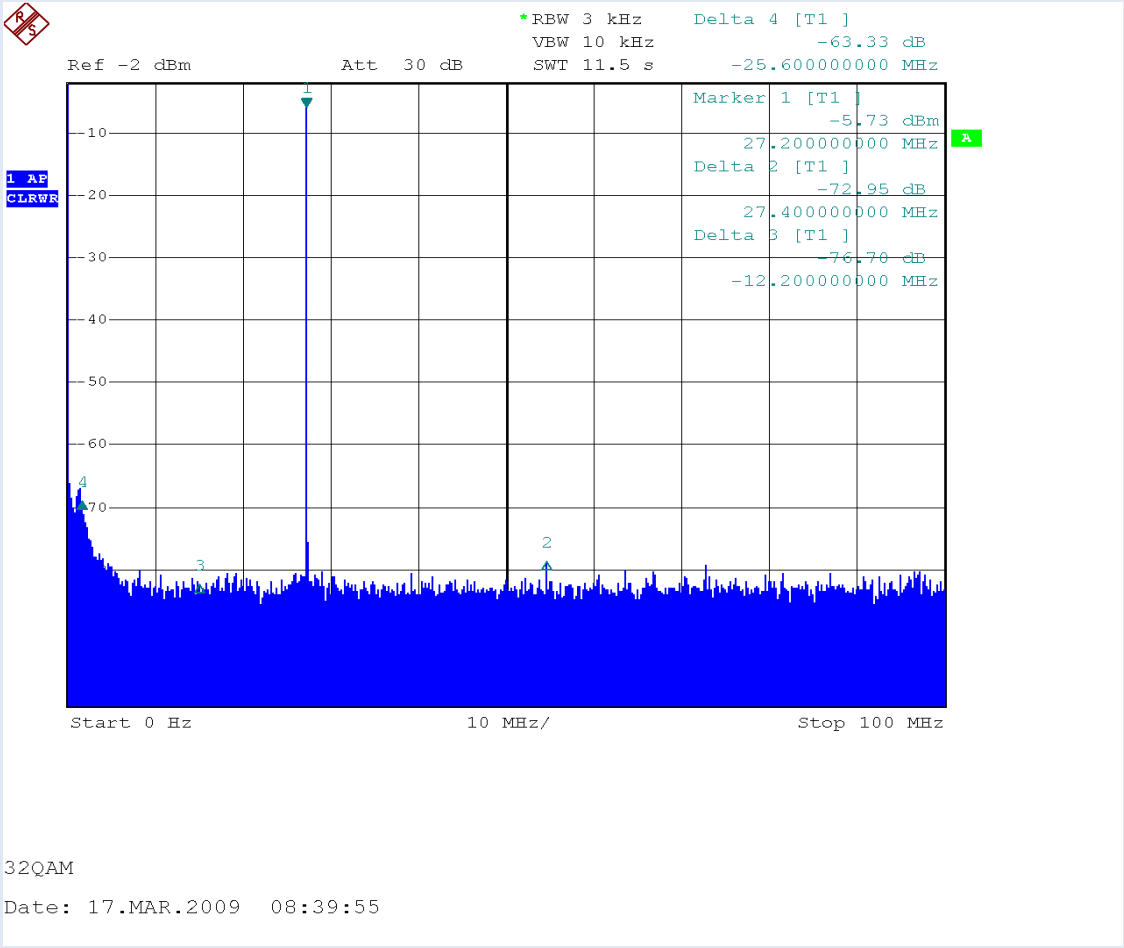




Lab Measurements

Spurs

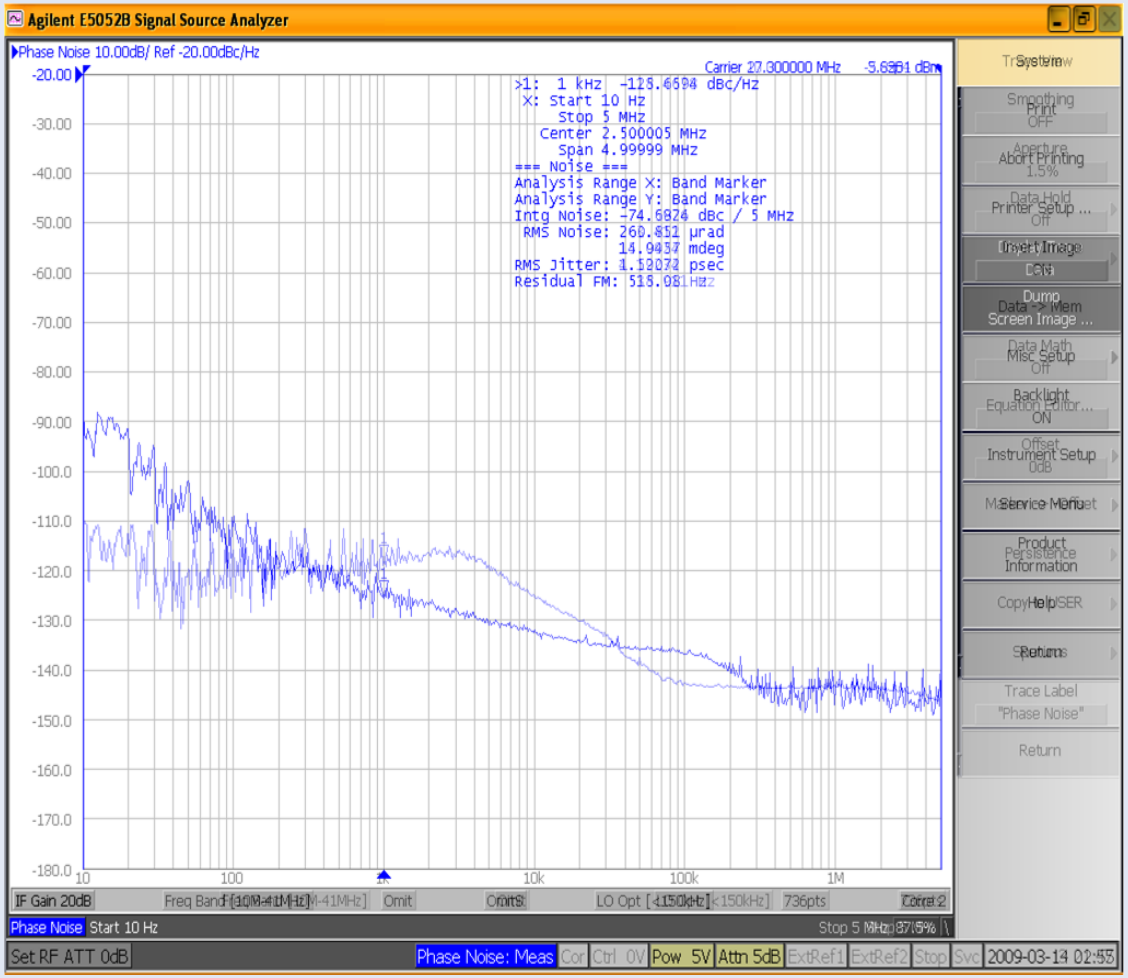
- -73dBc from the highest spur



Lab Measurements

Phase Noise

- Low phase noise
- RMS Jitter < 1.2 ps



Conclusion

- This novel circuit is the combination of a DDS and a PLL.
- A novel technique for optimal performance is presented
- Interesting note: transporting the “analog” value of the phase may introduce less jitter than going through clock buffers if the bit resolution is large enough. i.e. sending the “mu” instead of carrying a clock across a board may introduce less jitter under the right conditions.
- Excellent jitter and phase noise performance could be obtained.
- Simple, flexible, programmable.
- Suitable for many SDR applications.