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HARDWARE-IN-THE-LOOP DESIGN VERIFICATION TESTING FOR SOFTWARE-DEFINED RADIO WAVEFORMS

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Digital Test and Integration
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Overview

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- Hardware-in-the-loop (HWIL) test environment
  - Executes radio waveform on COTS board
  - Compares implemented waveform performance (BER, PER, packet synchronization, etc) vs. theoretical results
  - GUI allows user to swap firmware and software implementation of functions
  - Advantages:
    - expedites waveform design verification testing
    - provides platform for functional testing outside the target hardware
    - enables design verification testing for waveforms over complete range of waveform modes

Platform to expedite waveform design verification

Intro

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- SDRs offer greater flexibility and adaptability as they replace standard analog radio components with digital processing hardware and software.

- BUT… to implement waveforms in SDR requires
  - computationally intense algorithms error correction, digital filters and adaptive equalizers.
  - Parallel development of hardware and software
  - Fast detection and correction of waveform vulnerabilities through software updates

- We introduce the hardware-in-the-loop (HWIL) waveform test environment

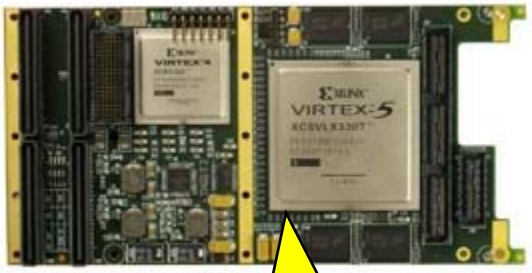
Purpose

Hardware-in-the-loop (HWIL) waveform test environment achieves…

- End-to-end testing
- Thorough test and validation of waveform processing
- Meeting waveform design requirements and establishing performance baselines
  - at FPGA level prior to hardware and software integration
  - Changes feed back to the waveform development process

Setup

- Test environment executes the radio waveform on a COTS board that fits in a PCI slot in a PC backplane
- COTS board was used to reduce hardware development and maintenance time
- GUI interface (using AlphaData APIs) from the COTS card
  - users can select the waveform processing in the test environment for transmit or receive path tests
  - user can also swap firmware and software implementations of the tests



AlphaData Xilinx COTS development hardware with an embedded Virtex 5-LX220 FPGA

Modulator and Demodulator Testing

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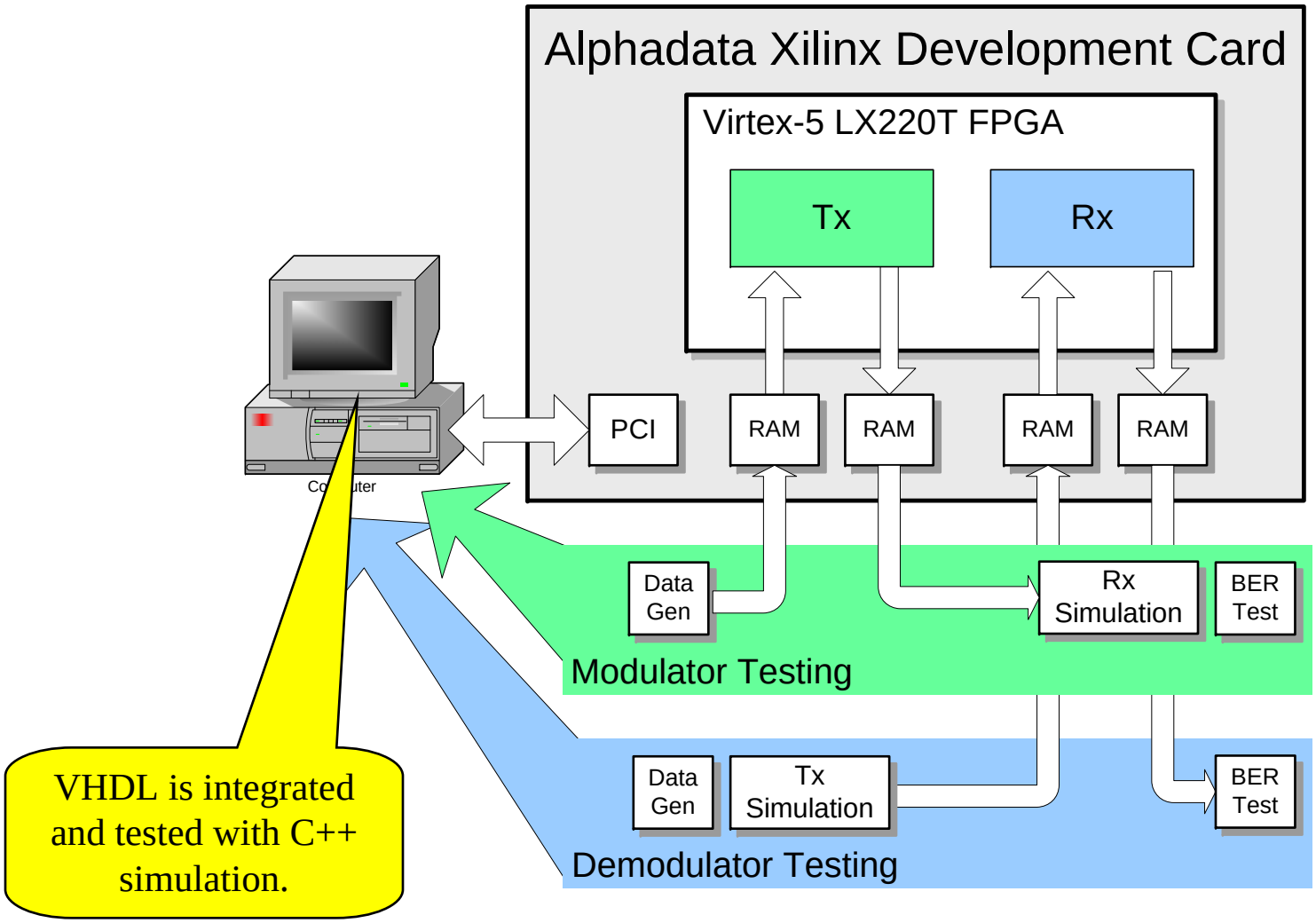

Modular Testing

- User executes a packet by writing to a specified register of the FPGA at the WTE GUI interface.
- user data, user status and packet configuration information are stored into four pages of memory in the RAM of the development card.
- FPGA processes the transmit path test for the wideband waveform and writes baseband or IF sample results back to the RAM off-chip memory bank
- Results processed by the FPGA are the data that would be sent to the DAC interface
- baseband or IF samples processed by the FPGA are inputs to the C++ simulation of waveform processing for receive path testing.

Demodulator Testing

- Start with C++ simulation of the transmit path of the wideband waveform.
- Baseband or IF sample results from the simulation are placed into the memory bank of the RAM in the COTS card
- Samples emulate the data that would be received by the FPGA at the ADC interface
- FPGA processes the receive path test for wideband waveform through de-interleaving, down conversion, synchronization, and demodulation algorithms before data is decoded and stored back to the RAM memory bank
- Results are extracted from the RAM for further analysis.

Loopback End-to-End Testing

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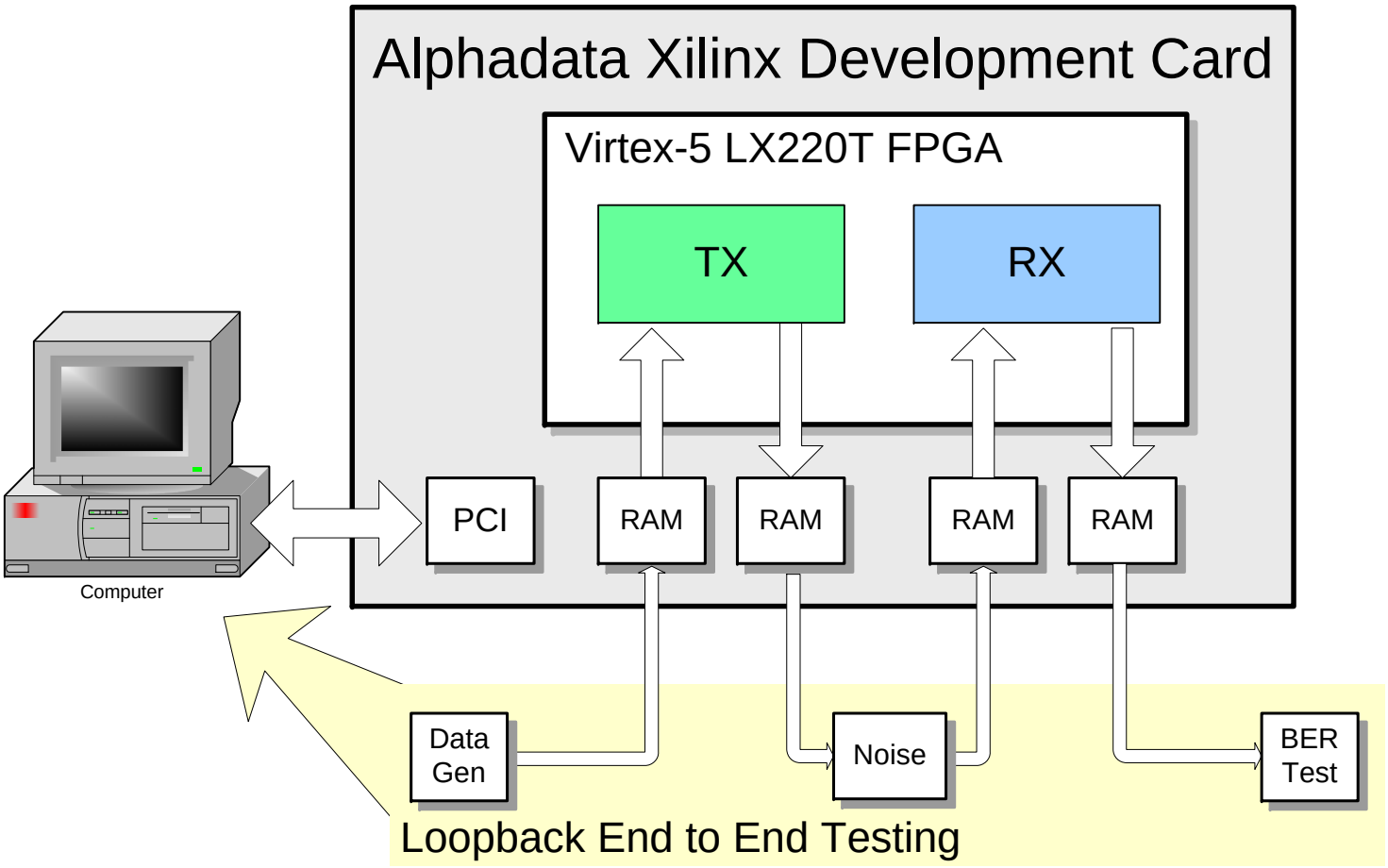

Loopback End-to-End Testing

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- End to end testing is accomplished at FPGA level prior to integration with target H/W and S/W
- Loopback end-to-end testing begins by storing the user data, status, and configuration information passed from the DSP to the RAM memory banks.
- FPGA executes waveform processing for transmit path test and writes baseband or IF samples to the memory bank
- Calibrated noise input is added to the baseband samples at the memory bank
- Finally, FPGA runs the waveform processing for receive path test and writes the results back to the RAM for further bit error rate (BER) and systems analyses

Data Calibrations

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- Different noise calibration of digital baseband samples or digital modem IF samples are introduced for various communication environments
- Data calibrations include attenuation, Doppler, propagation range delay, fading, and phase rotations
- We analyze the results of end-to-end testing for the different types of noise calibration inputs to rigorously test waveform implementation and ensure the waveform meets specified design requirements

GUI: Waveform Discovery and Sync Performance

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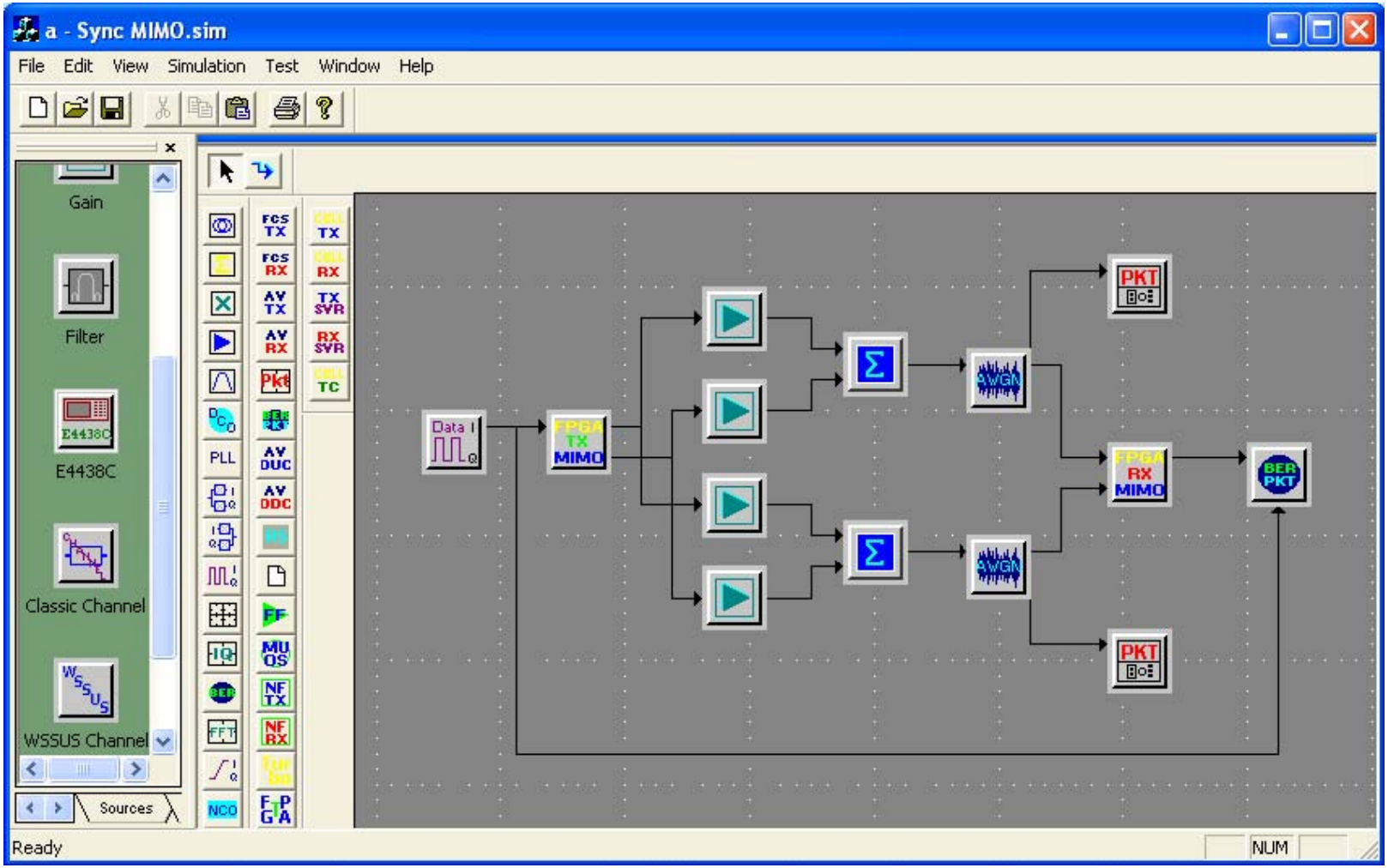

Results: Waveform Discovery and Sync Performance

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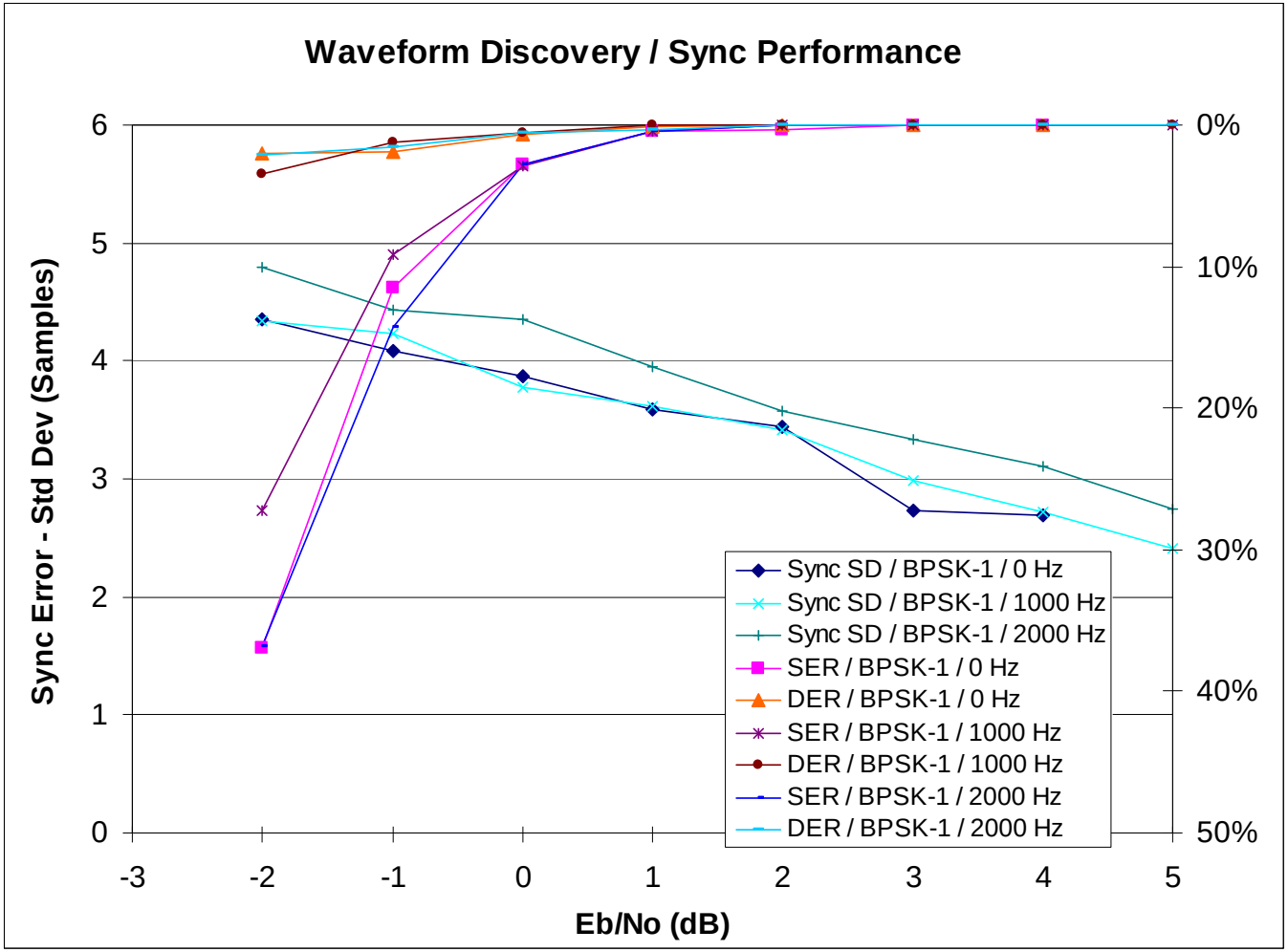

GUI: Multipath Fading

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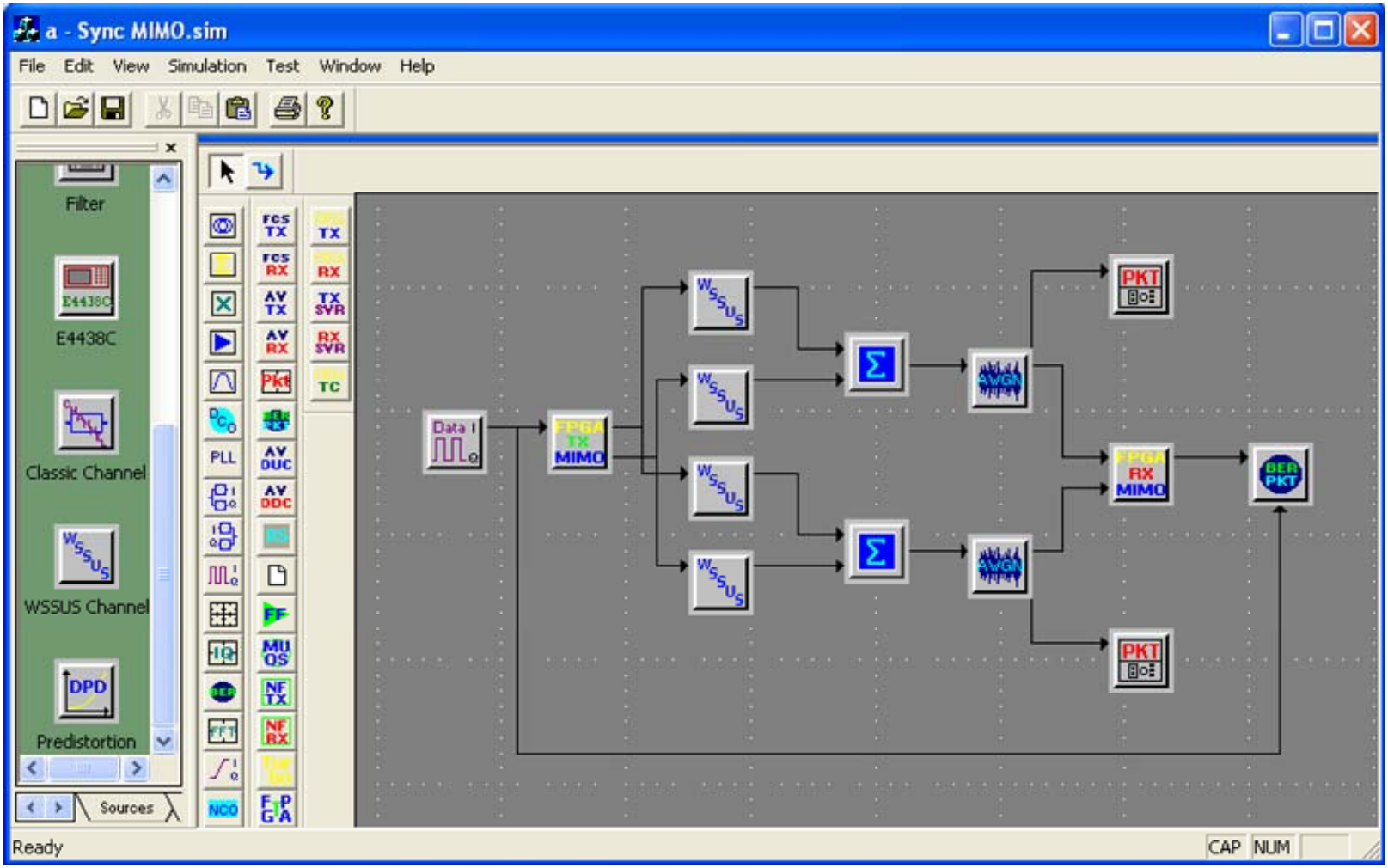

Results: Multipath Fading

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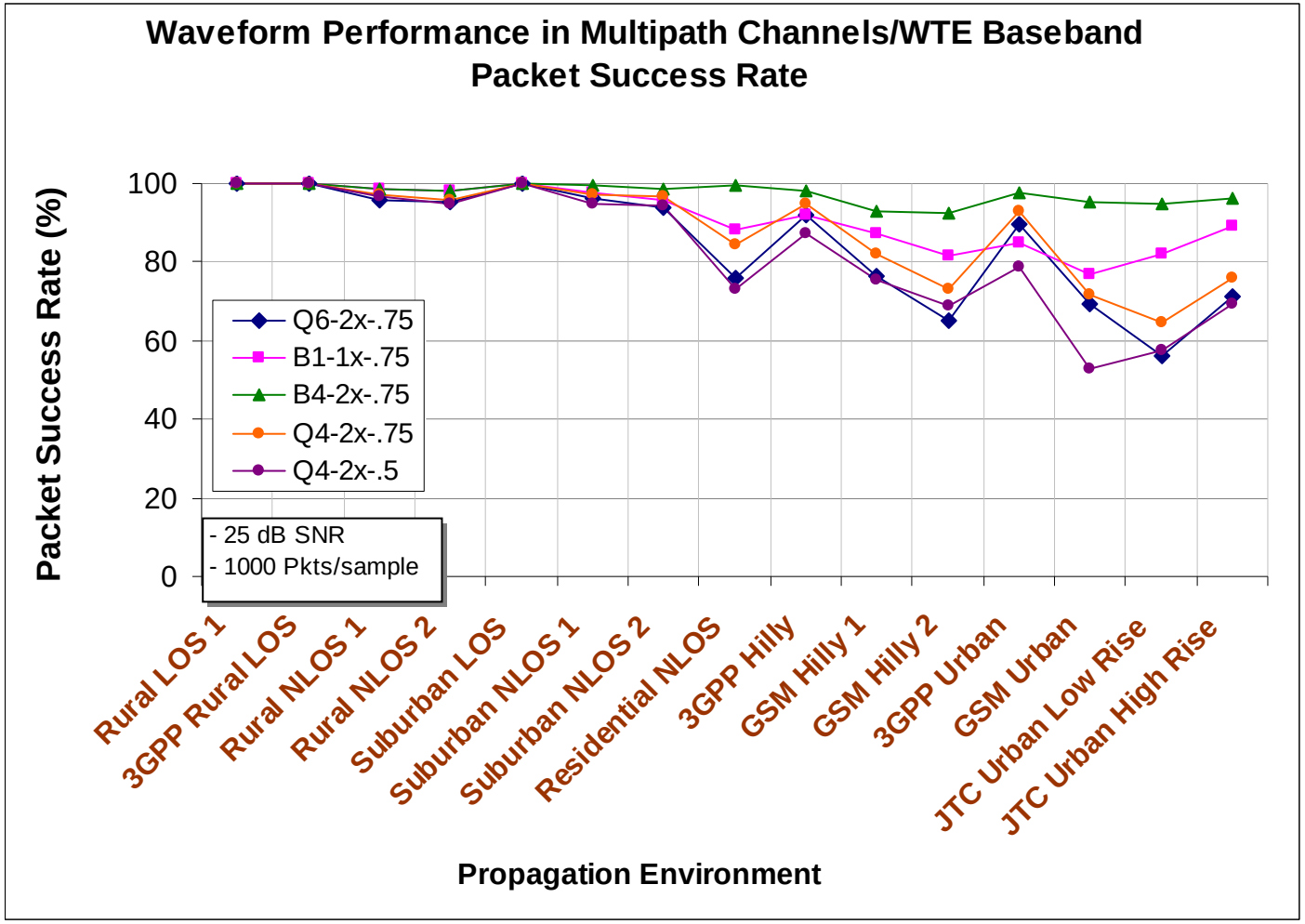

GUI: BER and Spectrum

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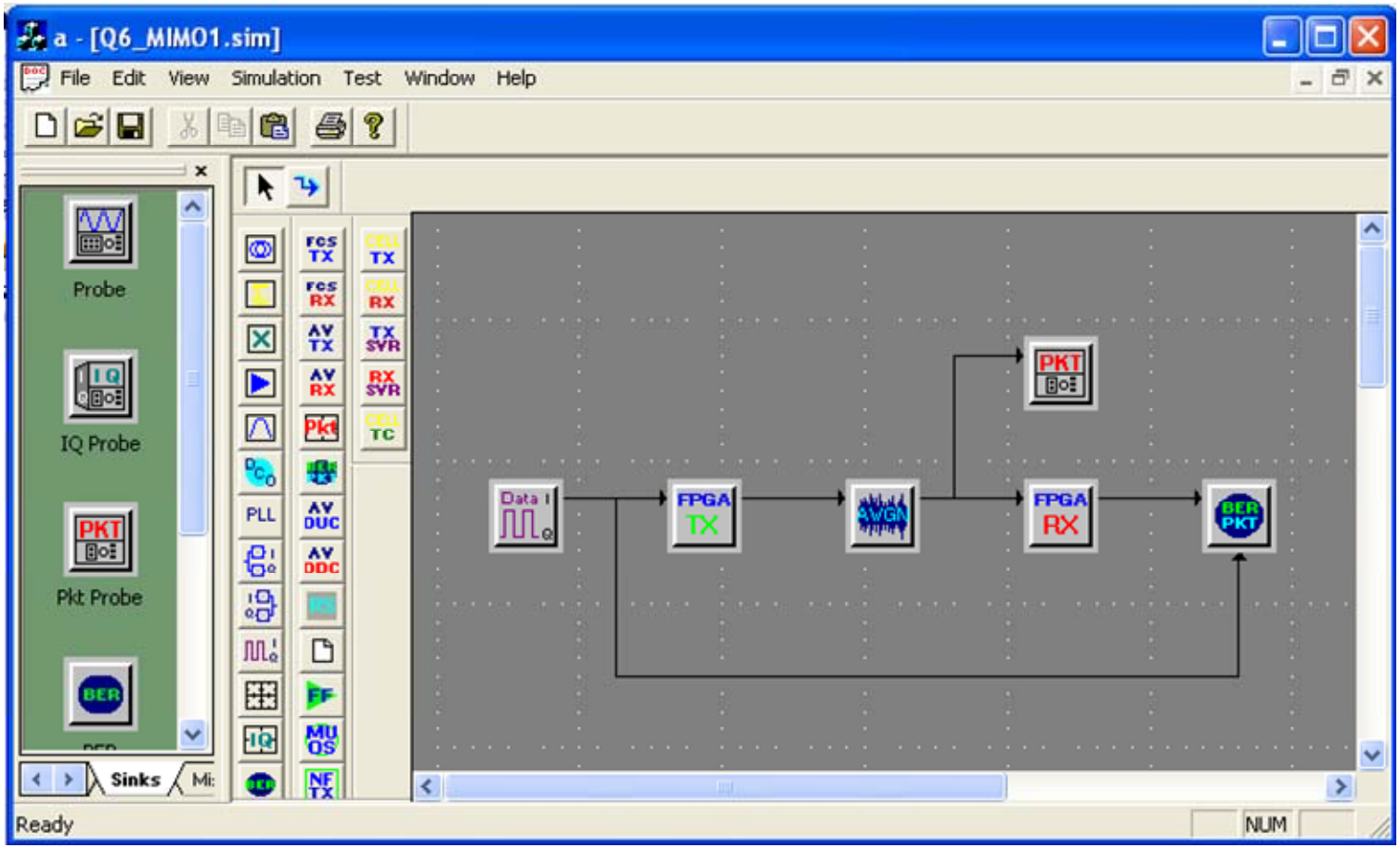

Results: BER vs. SNR

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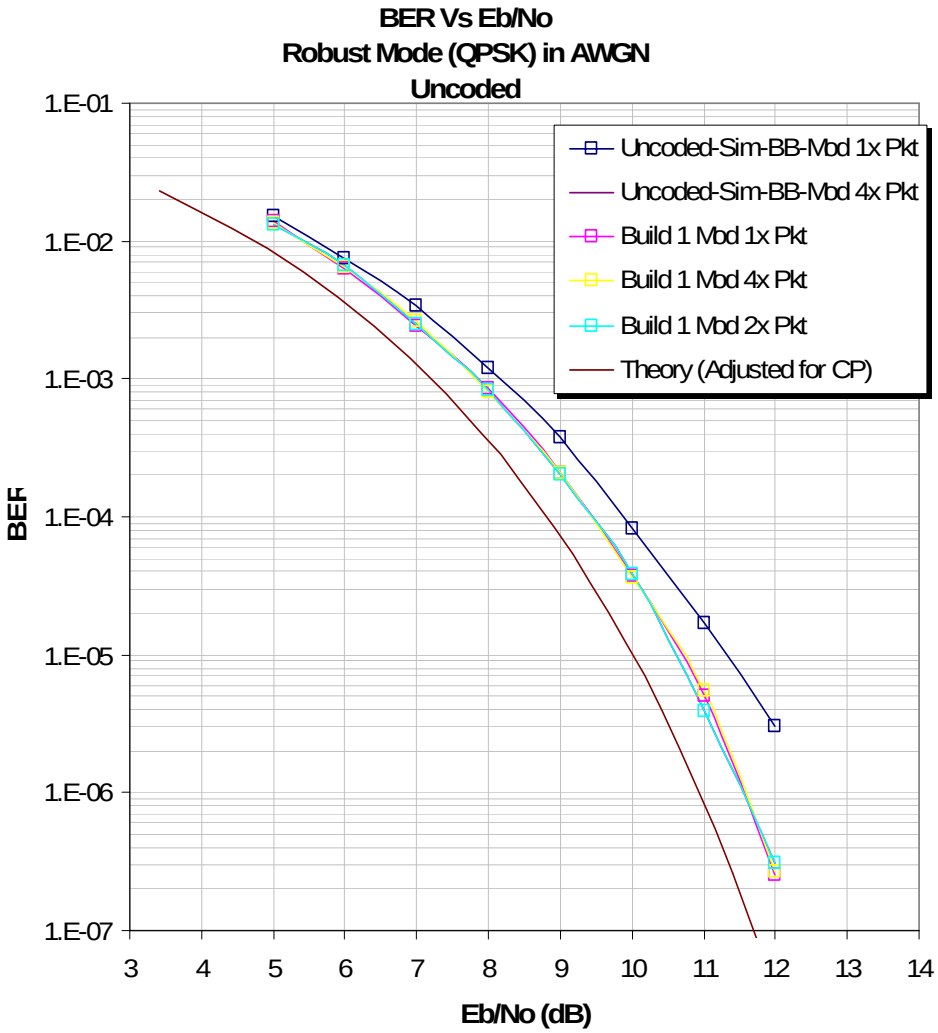

Results: Waveform Spectrum

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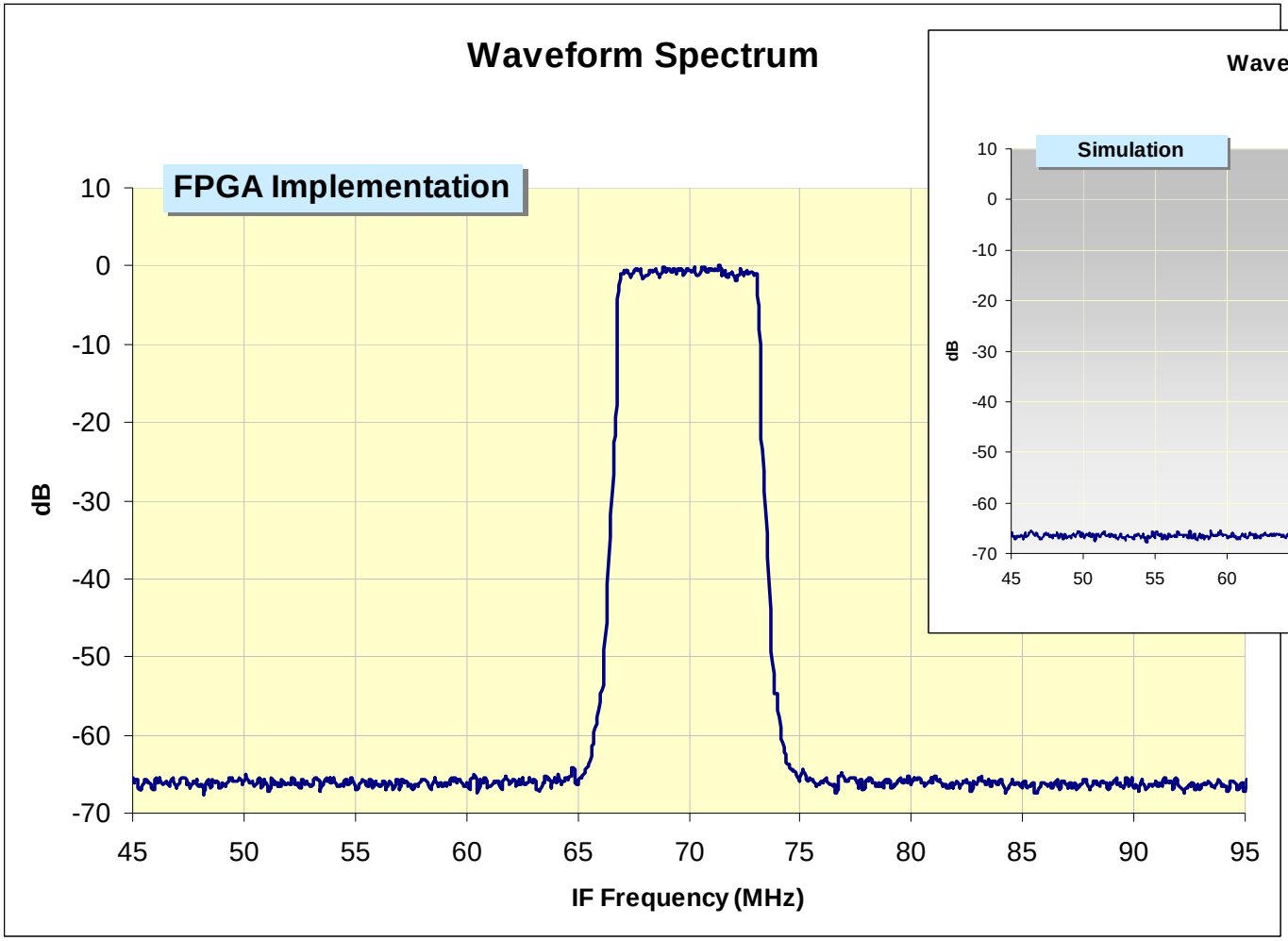

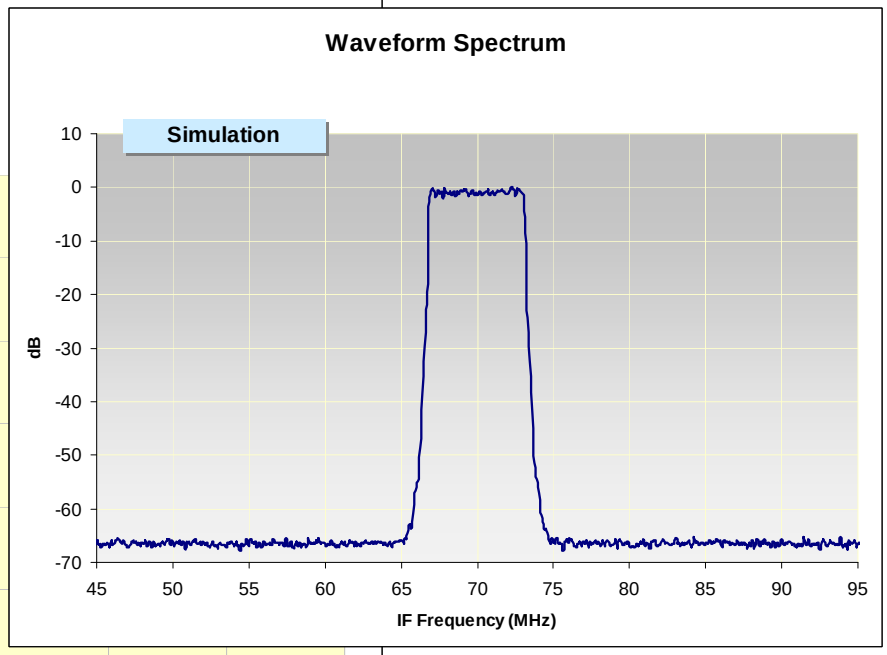

Conclusions

- We introduced a hardware-in-the-loop waveform test environment that uses a commercial off the shelf PCI card.
- Flexibility of COTs hardware and GUI application allow for specific functional testing, i.e. modulator, demodulator and end-to-end testing of the FPGA waveform processing
- Waveform test environment achieves our goals of shorter development cycles, product flexibility, adaptability, and decreased costs.