Packet Detection, Frequency Synchronization, and Channel Estimation/Equalization in OFDM-Based SDR Receivers

M.M. Ebrahimi, S.A. Bassam,
M. Helaoui, F.M Ghannouchi

SCHULICH School of Engineering

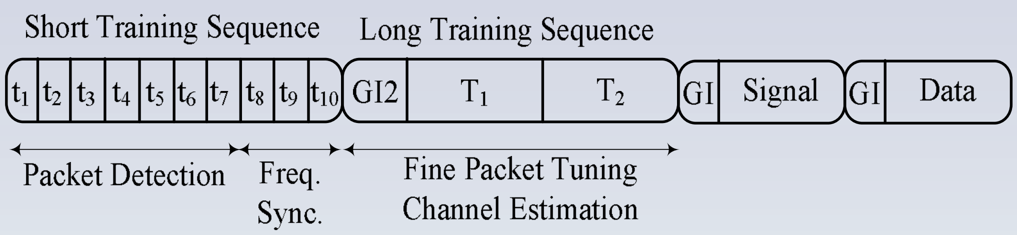
UNIVERSITY OF CALGARY

Outline

- OFDM Receivers
- Packet Detection and Frequency Synchronization
- Channel Estimation and Equalization
- DSP/FPGA Prototyping
- Conclusion

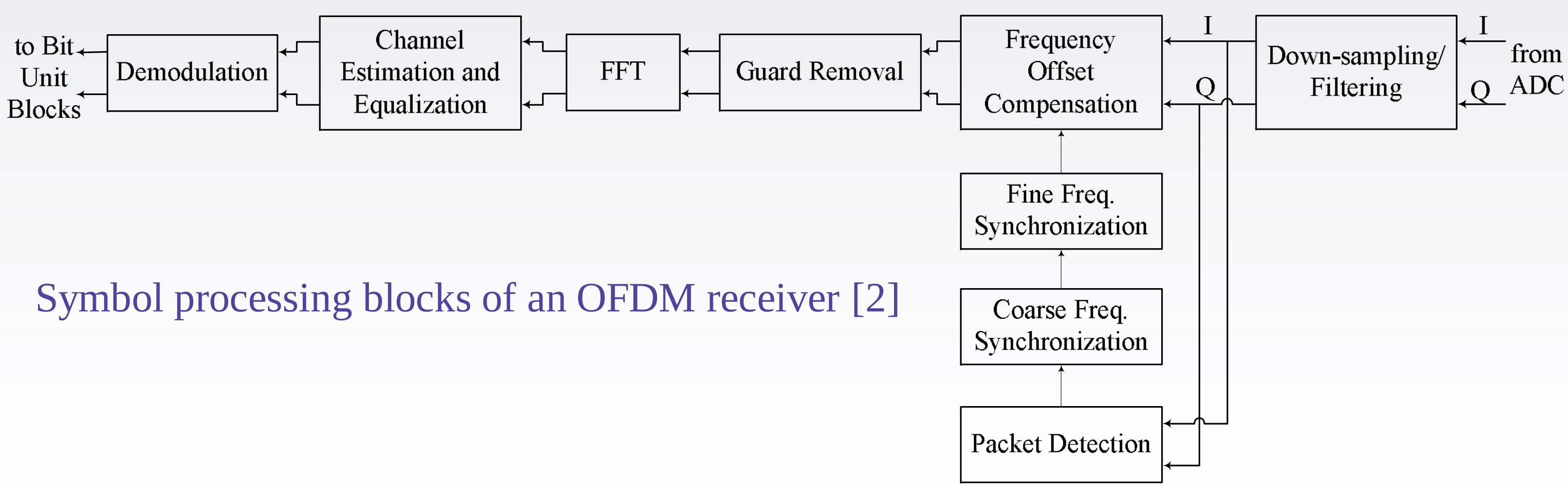
OFDM Receivers

- OFDM Scheme
  - Orthogonal FDM
  - Mostly burst structure



IEEE802.11a signal burst [1]

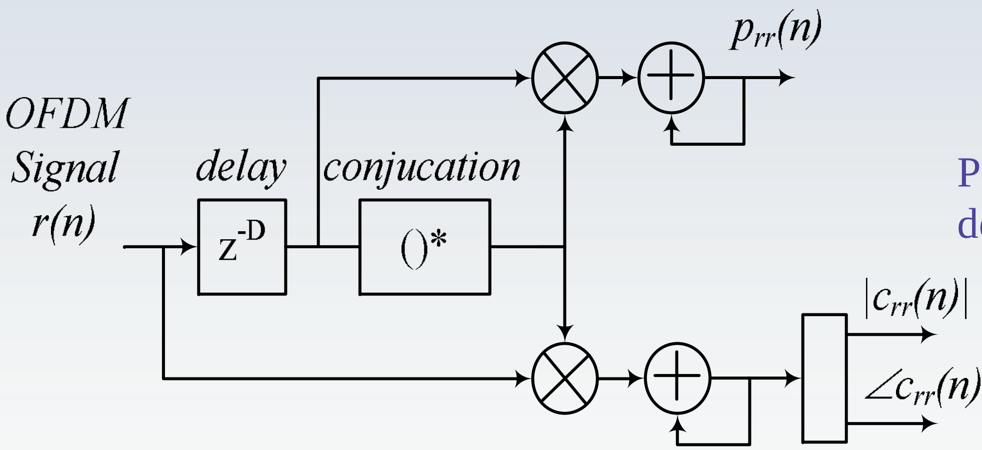
- Block Diagram of a General OFDM Receiver



Symbol processing blocks of an OFDM receiver [2]

Packet Detection and Frequency Synchronization

- Packet Detection
  - Shows the approximate beginning of the frame
  - Based on delay and correlation algorithm



Packet detection by applying delay and correlation algorithm

$$C_{rr}^{i}(n) = \sum_{k=0}^{L-1} r(n+k) r^*(n+k+iD)$$

$$p_{rr}(n) = \sum_{k=0}^{L-1} r(n+k+D) r^*(n+k+D) = \sum_{k=0}^{L-1} \left| r(n+k+D) \right|^2$$

$$thr(n) = \frac{\left| C_{rr}^{i}(n) \right|}{p_{rr}(n)}$$

Packet Detection and Frequency Synchronization

- Frequency Synchronization
  - Estimating frequency offset between transmitter and receiver
  - Performed on the short training sequence using delay and correlation algorithms

$$r(n) = s(n)e^{j2\pi f_t nT_s} e^{-j2\pi f_r nT_s} = s(n)e^{j2\pi f_\Delta nT_s}$$

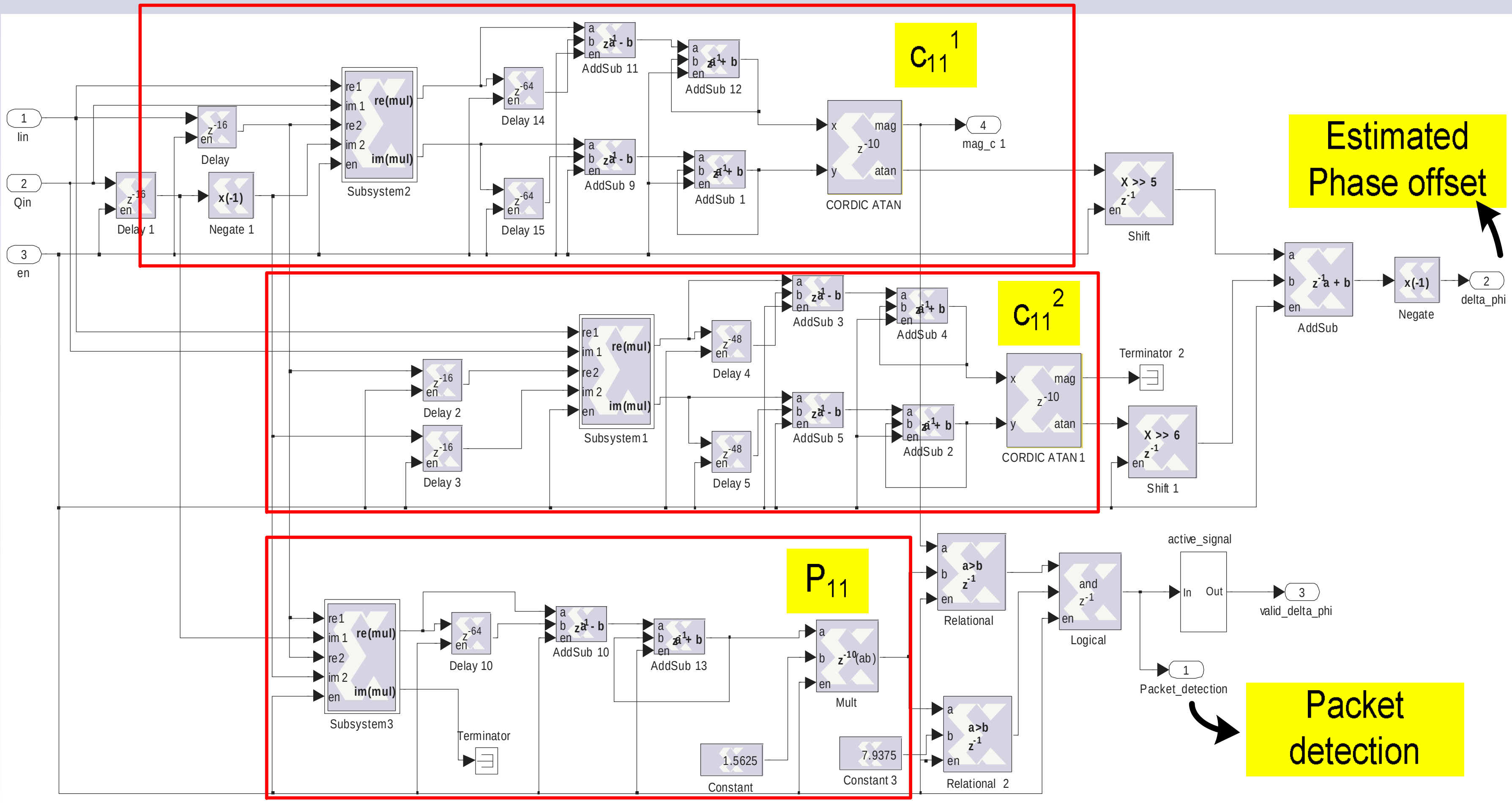
$$c_{rr}^{i}(n) = \sum_{k=0}^{L-1} r(n+k)r^*(n+k+iD) = e^{j2\pi f_\Delta iDT_s} \sum_{k=0}^{L-1} \left|s(n)\right|^2$$

$$f_\Delta = f_t - f_r = 0.5 \times \left(\frac{\angle c_{rr}^{1}(n)}{2\pi DT_s} + \frac{\angle c_{rr}^{2}(n)}{4\pi DT_s} \right) \qquad \Delta\varphi = \frac{2\pi f_\Delta}{f_s} = \frac{\angle c_{rr}^{1}(n)}{2D} + \frac{\angle c_{rr}^{2}(n)}{4D}$$

iradiolab

SCHULICH School of Engineering UNIVERSITY OF CALGARY

Packet Detection and Frequency Synchronization



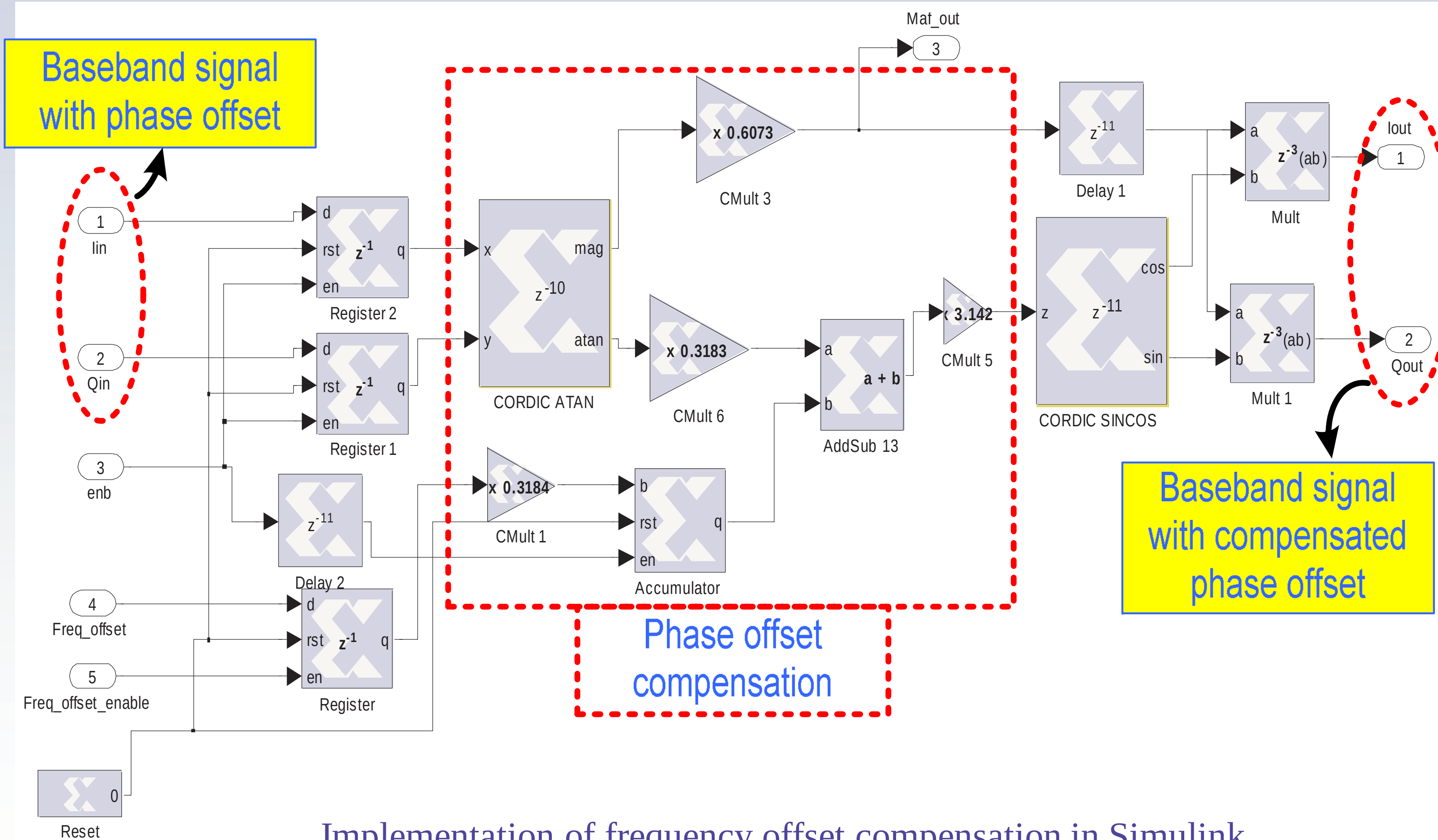
Implementation of packet detection and frequency offset estimation in Simulink

iradiolab

SCHULICH School of Engineering

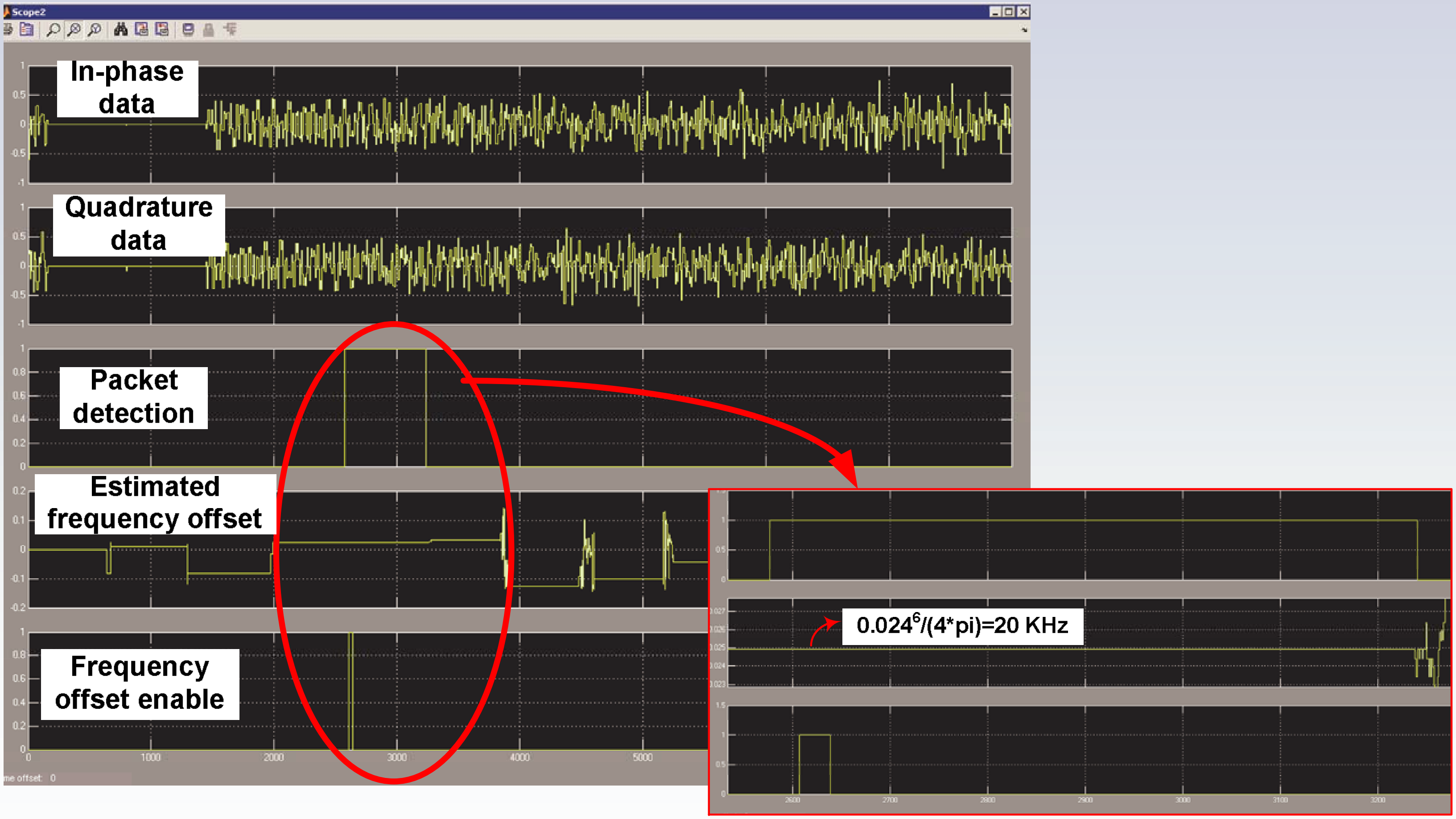
UNIVERSITY OF CALGARY

Packet Detection and Frequency Synchronization



Implementation of frequency offset compensation in Simulink

Packet Detection and Frequency Synchronization

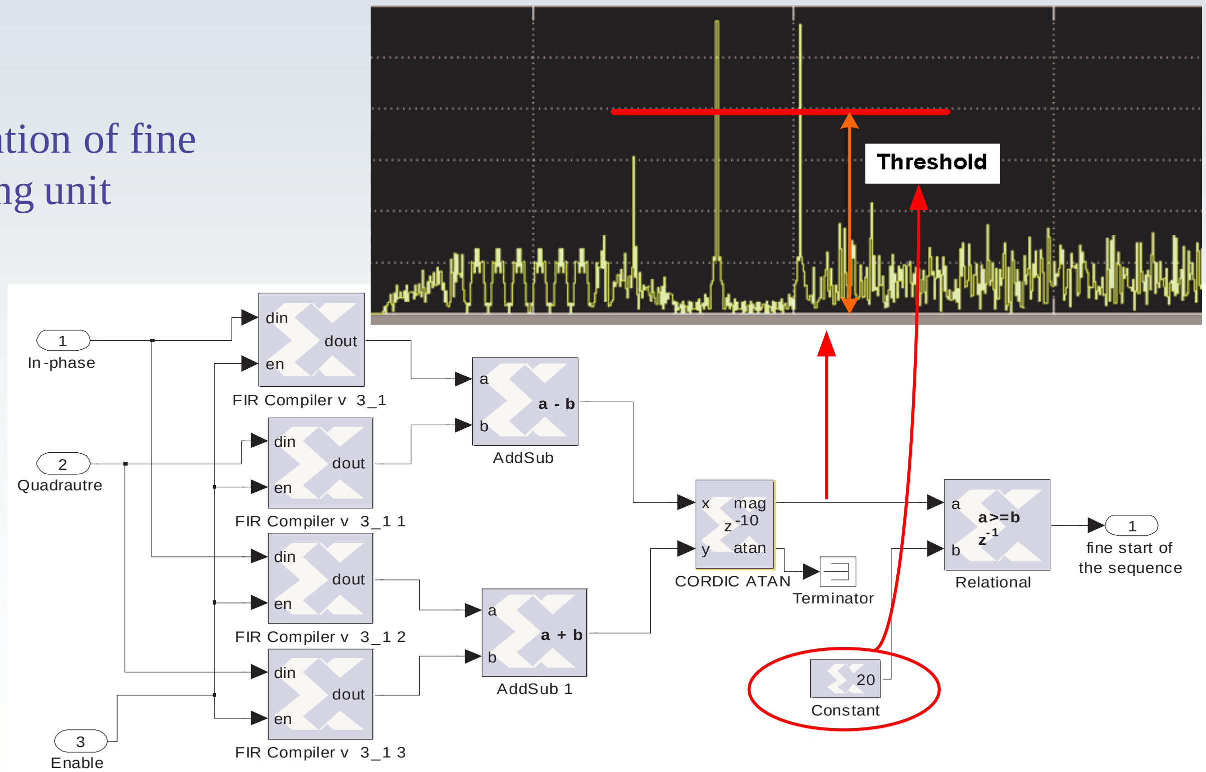


802.11a packet detection and frequency synchronization (frequency offset compensation) results

Packet Detection and Frequency Synchronization

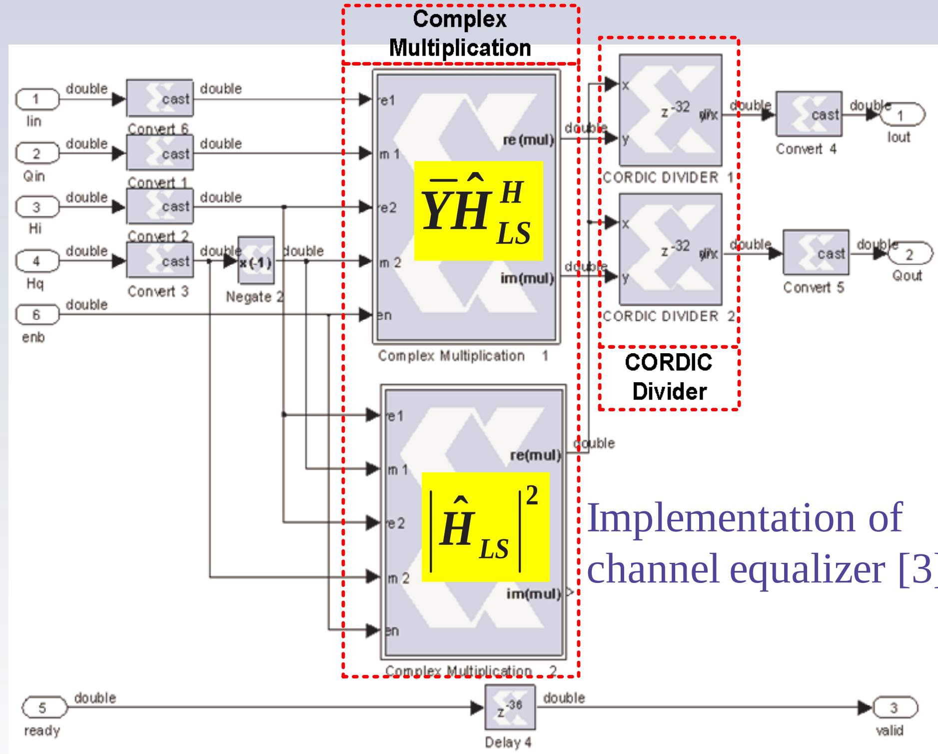
- Fine Packet Tuning (Fine Frequency Synchronization)
  - To find exact position of the beginning of the sequence
  - Performed on the long training sequence using correlation algorithm

Implementation of fine packet tuning unit



Channel Estimation and Equalization

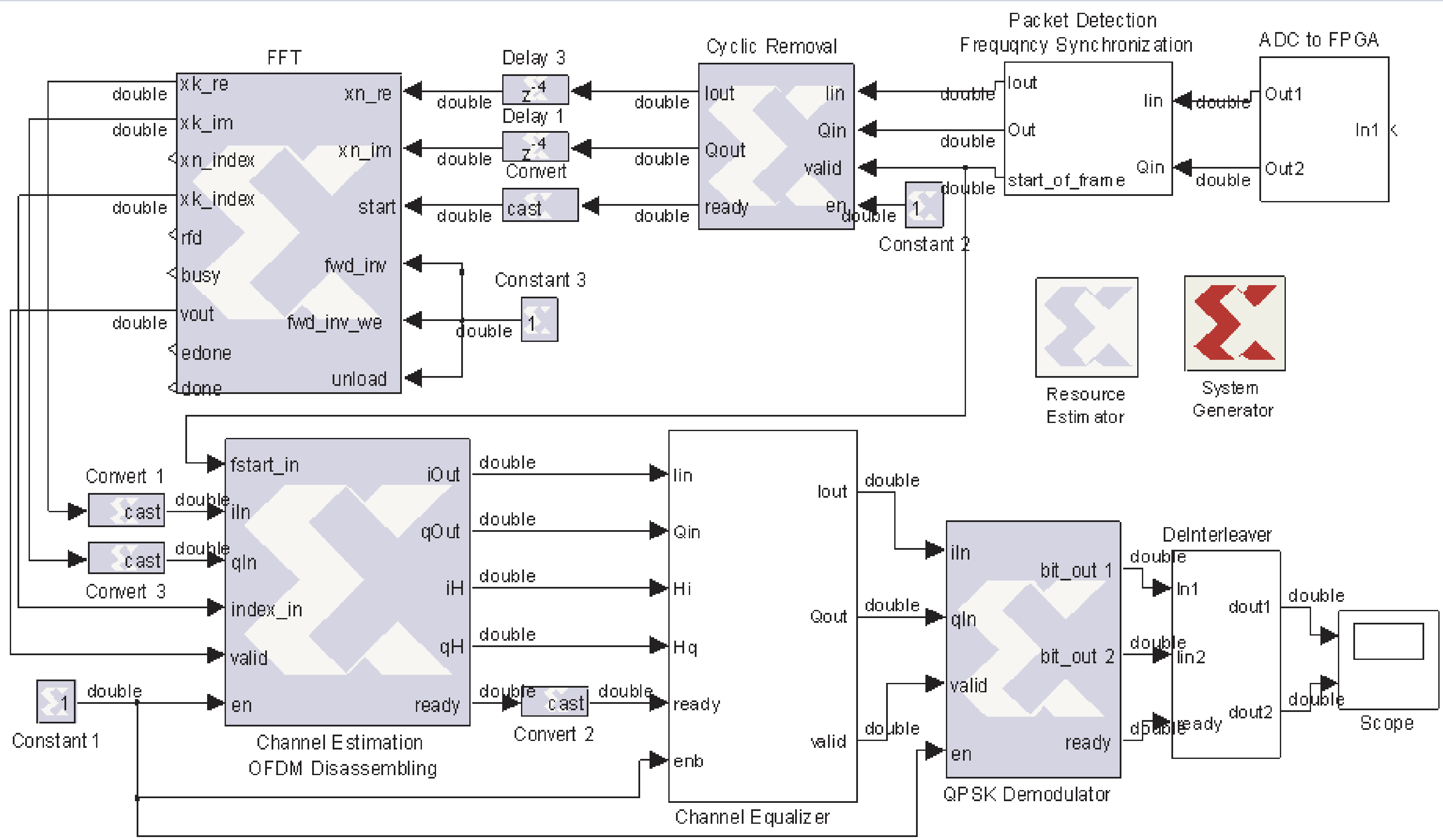
- OFDM channel estimation simplified like for narrowband signals
- Two estimation methods:
  - Least square (LS)
  - Minimum mean-square error (MMSE)
- LS
  - Less complexity ➔ more suitable for FPGA
  - Higher error



Implementation of channel equalizer [3]

$$\hat{X}_{est} = \overline{Y}\frac{\hat{H}_{LS}^{H}}{|H_{LS}|^{2}} = \overline{XH}\frac{\hat{H}_{LS}^{H}}{|H_{LS}|^{2}} + \overline{N}\frac{\hat{H}_{LS}^{H}}{|H_{LS}|^{2}} = \overline{X} + \overline{N}\frac{\hat{H}_{LS}^{H}}{|H_{LS}|^{2}}$$

OFDM Receiver



Implementation of all symbol processing blocks of an OFDM receiver

iradiolab

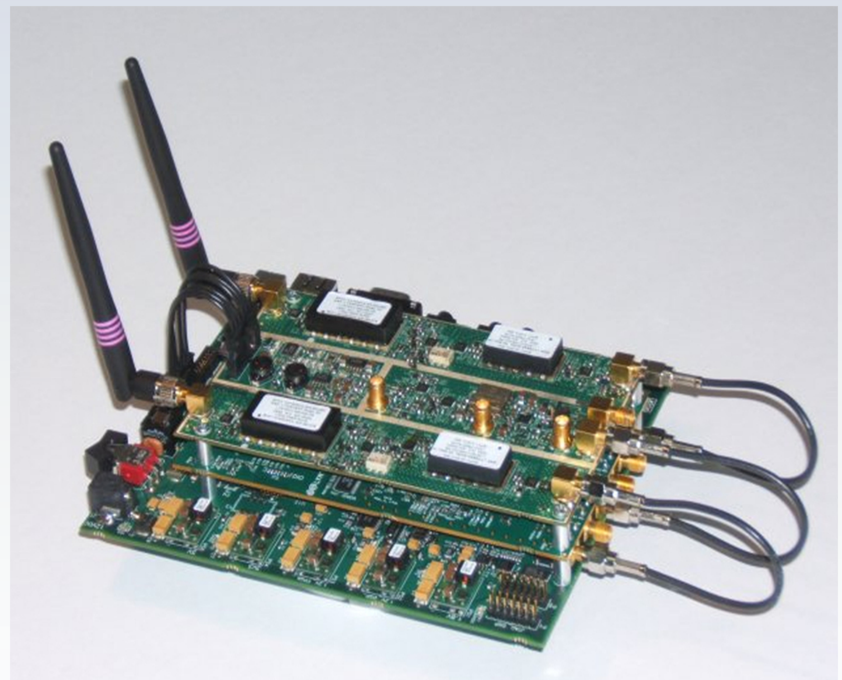
SCHULICH School of Engineering

DSP/FPGA Prototyping

- SDR development board from Lyrtech
  - FPGA: Xilinx's Virtex IV SX35 FPGA from,
  - ADC: TI's ADS5500
  - DAC: TI's DAC5687

Resource used to implement the OFDM-based receiver for SDR application

Slices	FFs	RAM Blocks	LUTs	Embedded MULs	IO Blocks
7500	8028	11	10891	70	14



Lyrtech Virtex-4 FPGA SDR Development Platform [4]

Conclusion

- Rapid prototyping of the PHY layer of OFDM based-receivers
- Theory and implementation of packet detection, frequency synchronization, and channel estimation/equalization
- Simultaneous utilizing of MATLAB/Simulink and VHDL code reduces the complexity and minimizes the required resource
- Estimation of the required resources for the implementation on the Xilinx FPGA VI based platform.
- Validation through implementation on an SDR development board from Lyrtech.

Reference

1. Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications, IEEE Std 802.11a-1999.
2. J. D. Guffey, A. M. Wyglinski, G. J. Minden, “Agile Radio Implementation of OFDM Physical Layer for Dynamic Spectrum Access Research”, GLOBECOM07 2007 , pp. 4051-4055.
3. J.-J. van de Beek, O. Edfors, M. Sandell, S.K. Wilson, P. O. Borjesson, “On Channel Estimation in OFDM Systems”, IEEE Vehicular Technology Conference, Vol.2, pp. 815-819, July 1995.
4. Small Form Factor (SFF) SDR development platform from Lyrtech. Product description can be found at: http://www.lyrtech.com/index.php?act=view&pv=SFF%20SDR%20development%20platforms.

Thank you