Teaching Digital Communications in a Developing Country using a Low Cost Software Defined Radio Laboratory

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Abstract - In this paper we shall outline a methodology for the teaching of digital communications courses in the senior undergraduate level in the Universidad Industrial de Santander, in Bucaramanga, Colombia, South America. The author will outline his experiences in teaching such courses as a visiting professor from Canada, using two low cost Software Defined Radio (SDR) laboratories developed by the author (costing US$200 and US$550, respectively). These laboratories are very inexpensive and based on Commercial Off The Shelf (COTS) FPGA boards and ADC/DAC boards, hence making them suitable for immediate deployment around the world, including (but not limited to) developing countries. Teaching and research in digital communications and SDR in a developing country, especially a troubled country such as Colombia, present unique challenges as compared to developed countries. This paper will also describe and elaborate upon some of these challenges, which sometimes turn out to be a blessing in disguise.

1. Introduction

Developing countries, depending on the definition used, contain upwards of 80% of the world's population. Regrettably, teaching of engineering topics in developing countries is often hampered by the lack of funds and lack of infrastructure. In this context, teaching of digital wireless communications courses often suffers in developing countries from the lack of modern laboratory equipment. In this paper we outline a methodology for the teaching of digital communications courses in the senior undergraduate level in Colombia, South America. The author will outline his experiences in teaching such courses as a visiting professor from Canada, using two low cost SDR laboratories developed by the author (costing US$200 and US$550, respectively).

The first of these laboratories was based on a Xilinx Spartan 3A Starter Kit costing less than $200, and was described in the paper "An Ultra Low Cost Software Defined Radio Laboratory for Education and Research" [1] presented in SDR'09. Though, as shown in [1], that laboratory is quite capable and useful, the limits of what is possible in terms of its FPGA capacity was reached. The small Spartan 3A FPGA had been pushed to its capacity limit, newer designs did not fit in the FPGA, and in order to add new features and modulations a new platform was needed. Hence the need for this second laboratory.

This second, new laboratory which is presented in this paper costs around US$550 and is based on the Altera DE2-70 board ($330) and an add-on ADC/DAC card, the Terasic GPIO-ADA ($220) daughterboard. This laboratory is shown in Fig. 1. The laboratory uses as its foundation a port to Altera FPGAs of the laboratory in [1] and includes a complete software defined system comprising a transmitter, a hardware channel simulator, and a receiver. The laboratory can generate transmission and reception at many signal-to-noise ratios and using more than 20 different wireless digital communications modulation types and hundreds of different variants of those modulations. The main features that the new laboratory adds include (a) support for offset modulations; (b) support for pulse shaping; (c) support for some CPM (continuous phase modulation); (d) enhanced control over sampling rates and carrier frequency; (e) better channel emulation; (f) much wider SNR range support; (g) much better quantization performance.

Though the cost of the new laboratory is higher than that presented in [1] ($550 vs. $200), it is still extremely inexpensive, typically several orders of magnitude lower than commercially available laboratories, and the fact that they are based on unmodified and inexpensive FPGA COTS boards, makes these laboratories very attractive for teaching of the subject of digital communications in developing (and, indeed, developed) countries. Moreover, as in [1], if the same FPGA boards are used for other courses, then the incremental cost of using the FPGA boards for the laboratory can theoretically tend to $0 if the cost of the FPGA boards is spread among all courses that use them.

In this paper, we shall present numerical data gathered via surveys conducted of students taught by the author at the Universidad Industrial de Santander in Colombia over 2 semesters. The results will show that the laboratories are very effective as a teaching aid, and that the current, improved laboratory is an even better teaching aid than the laboratory presented at SDR'09. Additionally, the author will comment in this paper on the unique challenges of teaching such an advanced subject with little resources in a developing country.

2. Chronological Background and Context

In late 2007, after receiving his Ph.D. in Electrical Engineering from the University of British Colombia, Canada, the author accepted a visiting professorship for 1 year at a private university, Universidad Pontificia Bolivariana (UPB) in Bucaramanga, Colombia. The purpose of this visiting professorship was, from the author's perspective, a chance to better understand the developing world, and, from the university's perspective, a chance to have an international faculty member. The experiences of the author in that university are briefly summarized in [1].

For a variety of reasons the author decided to extend his stay in Colombia for an additional year, but since January 2010 the author changed affiliation to the Universidad Industrial de Santander (UIS) in Bucaramanga, Colombia. The UIS is one of Colombia's largest public universities with about 20,000 students, mostly undergraduates. The university system in Colombia suffers from a multitude of severe problems. Most students, and sometimes also professors, have little English proficiency which greatly impedes their university education, especially in engineering. High-school education is deficient in all subjects and students enter the university under-prepared. The problem is compounded by ridiculous academic regulations, which, for example, allow

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students to repeat courses as many times as they wish, cancel courses up until the *very last day of classes*, and there is no time limit imposed for the students to graduate. Tuition (at least for public universities) is nearly free, due to government subsidies. Needless to say, such regulations promote an atmosphere of very lax academic standards, where students repeat and cancel many courses several times until they finally pass them. It is commonplace for many students to complete their *bachelor's* degree after 8, 9, or 10 years, or even more (!). Clearly, such regulations are not conducive to academic performance.

Regarding security, whilst the author's 1.5 year visit in the private UPB was uneventful, the UIS is a far different story. There is a well-known tradition of student activism in Latin America's public universities, Colombia in particular, but one cannot fully appreciate the severity of this problem from afar. At the UIS, the university is often evacuated due to violent protests by small groups of students. The protagonists of the disturbances will generally cite lofty political motives, such as opposition to a free-trade agreement signed by the government. The university administration and the police allege that rebel guerrilla groups have infiltrated the university and are responsible. While there is probably some truth to this, the author's personal conclusion is much more mundane. It seems to the author that the disturbances are caused mainly by the worst performing students which have no interest in actually studying but rather in vandalizing the university for personal pleasure and/or to avoid academic duties such as exams. The university's failure to forcibly put an end to the problem with police action is very puzzling and is also to blame. Thus, a small group of 10-20 violent "students", with their faces covered to conceal their identity, consistently manages to shut down the university several times a month with such violent disturbances, sometimes using homemade explosive artefacts which have in the past led to police, students, and staff being wounded and even killed. Indeed, while many of the SDR systems presented at the SDR'10 conference are designed to be deployed by militaries in battlefield situations, this paper probably presents the only SDR system whose *development* occurred under fire.

It is difficult to teach and conduct research in such an environment. Paradoxically, it makes the usage of the laboratory as a teaching aid even more necessary, because of the lack of strong mathematical foundations of the student body and because of the great difficulty of requiring autonomous, book-based learning. Moreover, as noted in [1], the lack of resources often is a blessing in disguise, as it indirectly promotes innovation, especially regarding compact SDR hardware structures for FPGA implementations, which is also a facet of the current laboratory, and will be a subject of future publications which are in the works.

3. Physical Platform

The laboratory is based on a 70,000 Logic Element Altera Cyclone II FPGA in the DE2-70 board (see Fig. 1). In addition to the FPGA, the board contains:

• USB connection	• 2-Mbyte SSRAM
• Two 32-Mbyte SDRAM	• 8-Mbyte Flash memory
• SD Card Socket	• 4 Pushbutton Switches
• 18 Toggle switches	• 50-Mhz and 28.63-Mhz Oscillators
• 9 Green + 18 Red LEDs	• VGA output
• 24-bit audio CODEC with line-in, line-out, and microphone-in	• 10/100 Ethernet Controller with a connector
• 2 TV Decoder (NTSC/PAL) and TV-in connector	• RS-232 transceiver and 9-pin connector
• USB Host/Slave Controller	• IrDA transceiver
• PS/2 mouse/keyboard connector	• Two 40-pin Expansion Headers

For additional details on the FPGA board the reader is directed to [2, 3]. The large selection of peripheral components and the abundant FPGA resources (about 7 times more logic resources than the previous FPGA used in [1]), make this board an exceptionally good option for general purpose FPGA-centered courses, e.g. in digital design, FPGAs, computer architecture, and networking. Indeed, many universities around the world use the DE2-70 board for a variety of such courses, and Altera offers tutorial and laboratory material specifically for these boards on its website [2]. The DE2-70 costs $330 for academic customers.

In the current laboratory implementation, the expansion slots were used to connect to an ADC/DAC daughterboard, namely the Terasic GPIO ADA card, which has 2 DACs and 2 ADCs, with the DACs operating up to 125 MSPS, and the ADCs operating up to 65 MSPS. This daughterboard can also be seen in Fig. 1. For more information see [3]. The daughterboard costs $220.

4. Implementation and Structure

The laboratory is activated by loading a configuration file into the FPGA (either via a connected computer's USB connection or an on-board FLASH memory). The FLASH also contains data for use in channel emulation [4]. For the current design, the FPGA EDA software (Quartus II Version 9.0) reports about 60% usage of the FPGA's capacity. The HDL code is written mainly in SystemVerilog and Verilog 2001, with some VHDL modules. No proprietary cores are used, and the HDL was written by the author.

4.1. Laboratory Architecture

A simplified functional diagram for the laboratory is shown in Fig. 2. Although the laboratory structure is similar to that of [1], there are many improvements and new features. The reader is strongly encouraged to review [1], since here we shall only concentrate on the improvements made to the laboratory and we shall not repeat the analysis of the innards of the laboratory which was conducted in [1] and which essentially applies here as well.

As with [1], the laboratory includes a data sequence generator, a modulator, a channel emulator (Gaussian noise addition, slow fading can also emulated), and a demodulator (coherent or differential). The demodulator includes BER (Bit Error Rate) measurements and SNR (Signal to Noise Ratio) estimation circuits. A new feature than has been added is the ability to emulate a saturated transmitter power amplifier, for example in order to emulate transmission via a satellite transponder. Examples of this will be shown shortly.

The modulation/demodulation combinations currently supported are BPSK, QPSK (4-QAM), 8-PSK, 16-PSK, DBPSK, DQPSK, D8PSK, D16PSK, QAM-16, QAM-64, QAM-256, OQAM-16, OQAM-64, OQAM-256, $\pi/4$-QPSK, $\pi/8$-8PSK, $\pi/4$-DQPSK, $\pi/8$-D8PSK, OQPSK, O-8PSK, and O-16PSK, and MSK. This modulation list is significantly expanded from [1]. Currently, work is ongoing to add CPM modulations such as GMSK. Transmission of GMSK has already been achieved, and the receiver side of GMSK is currently being designed.

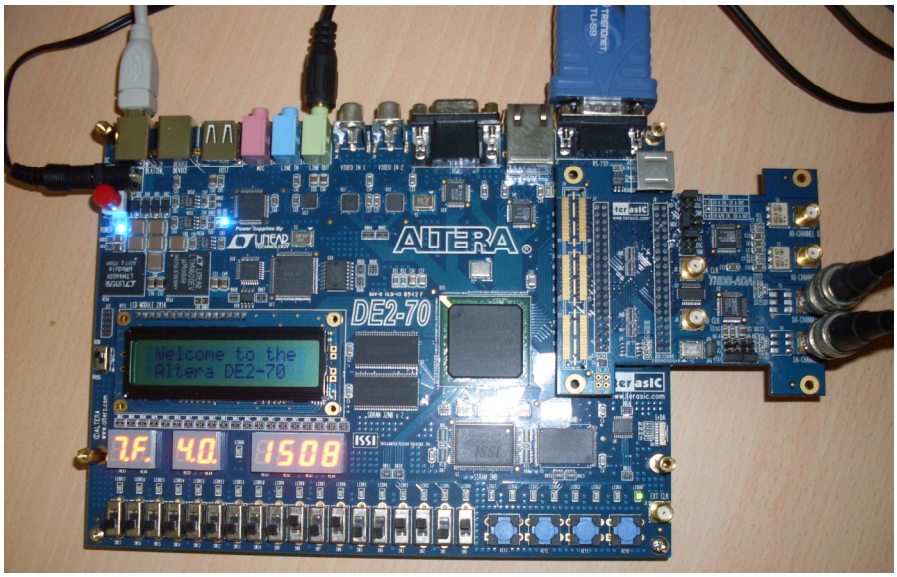

Fig. 1 –Altera DE2-70 board in which the lab is implemented. On the right-hand side the ADC/DAC daughterboard, the Terasic GPIO ADA card, can be seen, with the black BNC cables leading to the oscilloscope from the DACs. Also seen at the top of the card are the RS-232 connection and the audio and USB connections to the controlling computer, as well as the DC power input.

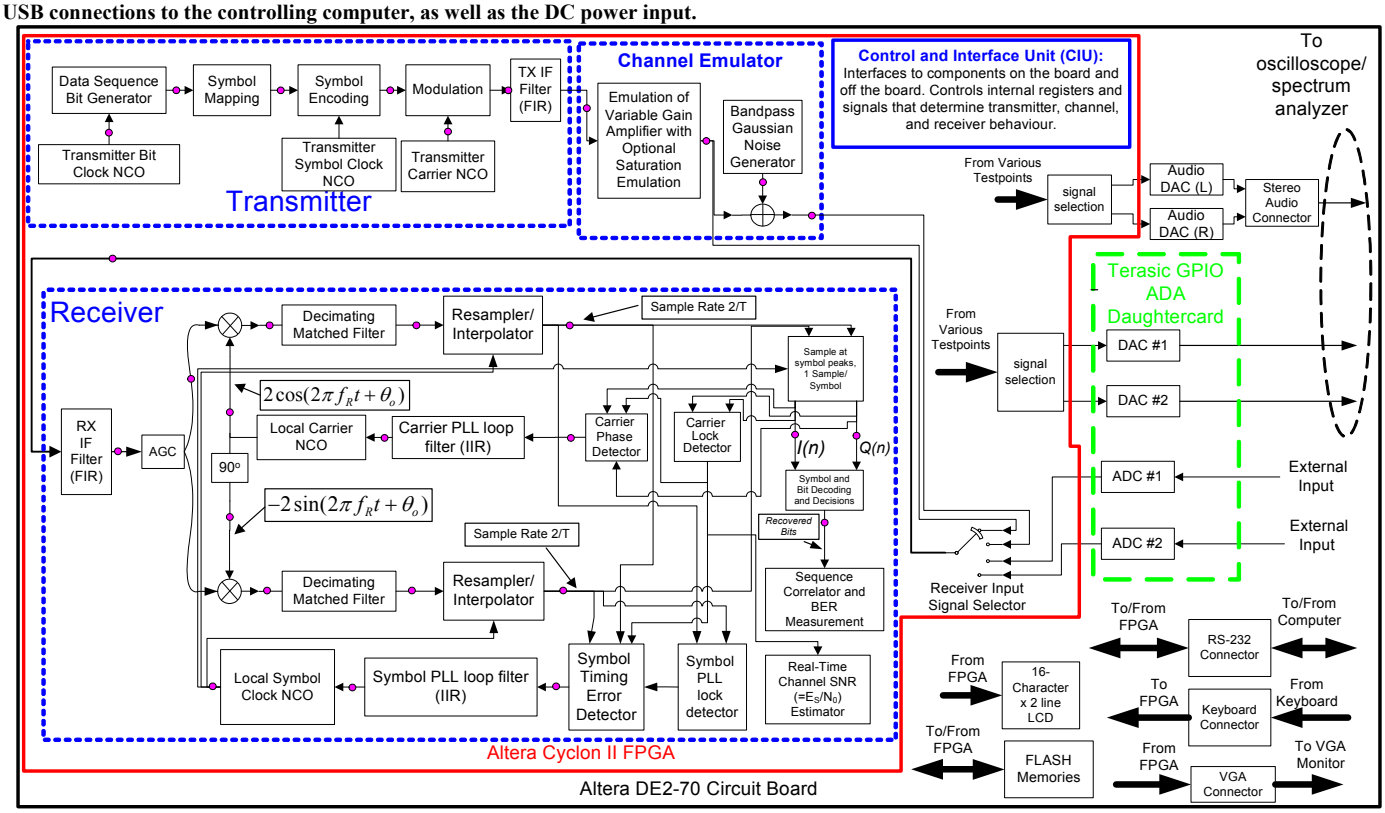

Fig. 2 – Simplified diagram of the wireless communications laboratory. Small magenta filled-in dots in the various paths represent some (but not all) of the possible test points that can be fed out to the DACs.

Another notable improvement is that pulse shaping has been added. Pulse shaping can be rectangular, Square-Root Raised-Cosine (rolloff factors of 0.35 and 0.85 are currently used) or user defined. The pulse shape is defined via 64-tap FIR filters in the I and Q arms in the transmitter that, via a multirate upconversion chain [5, 6 Chap. 13], generates the pulse shape for the modulation. In the receiver, a similar multirate downconversion chain [5, 6 Chap. 13] followed by 64-tap FIR matched filters in the I and Q arms complete the matched-filter reception.

The lab's architecture allows many exotic modulations forms to be generated and received (e.g.: Offset-$\pi/8$-D8PSK-with-half-sinusoidal-pulse-shaping). Though the practical importance of such exotic modulations is perhaps limited, academically they allow for deeper understanding of the various modulation

concepts, and can also be used to generate beautiful oscilloscope screenshots which heighten student interest and motivation. Many such example screenshots are given at the end of this paper.

Another subtle but very important improvement in the current laboratory as compared to [1] is that all the datapaths within the transmitter and receiver now use many more quantization bits (16 bits as opposed to 8 bits). This lowers the quantization noise significantly, allowing symbol SNRs of up to 40 dB to be generated in this laboratory, whereas the laboratory in [1] was limited to about 25 dB due to quantization noise.

The current parameters of the laboratory are summarized in Table 1. Although clearly the rates used do not approach the high data speeds that are possible to achieve with the FPGA, maintaining the carrier frequency and symbol rate low is desirable in an academic setting. By keeping the modulated signal within the 0-20 KHz range, and connecting the computer to the card via the card's audio-out DACs (see Fig. 1 and Fig. 2), a computer's audio card coupled with free spectrum analysis software can be used to

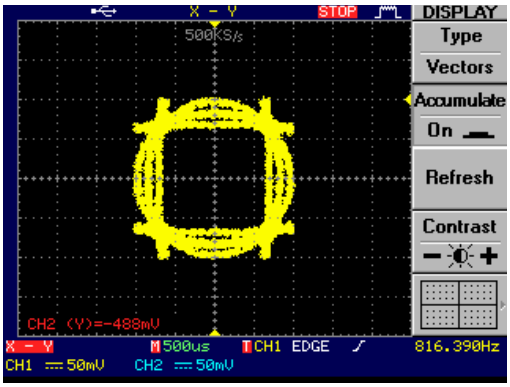

Fig. 3 – OQPSK transition diagram at receiver, rolloff = 0.85, SNR = 35 dB

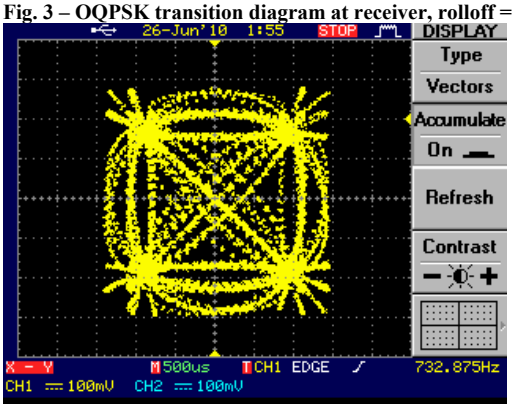

Fig. 4 - QPSK transition diagram at receiver, rolloff = 0.35, SNR = 35 dB

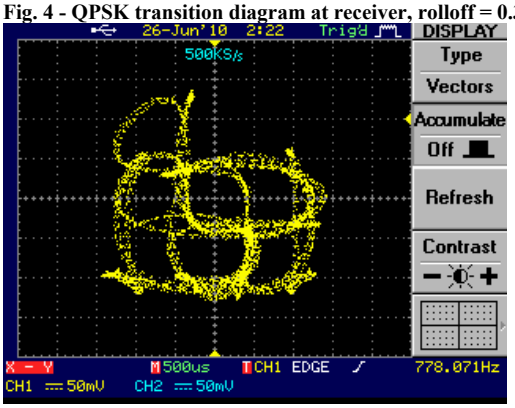

Fig. 5 – Partially formed transition diagram at the transmitter for Offset QAM-16 with a rolloff factor of 0.35

Table 1 – Summary of current wireless communications lab parameters

Parameter Name	Value
Symbol Coding	Differential coding, Gray mapping
Demodulation	Coherent or Differential
Carrier Frequency	User selectable up to 100 KHz
Symbol Rate	1/160 of the Sampling Rate
Sampling Rate	User selectable up to 1 MHz

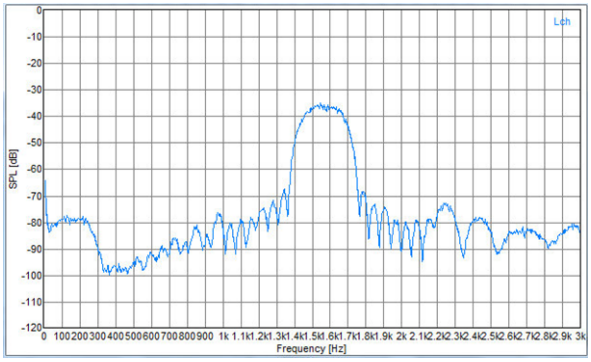

Fig. 6 - QPSK or OQPSK spectrum, rolloff = 0.85

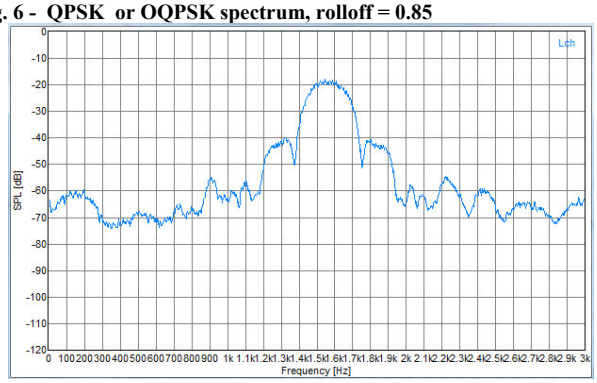

Fig. 7 – QPSK Spectrum, rolloff = 0.85, through saturated amplifier

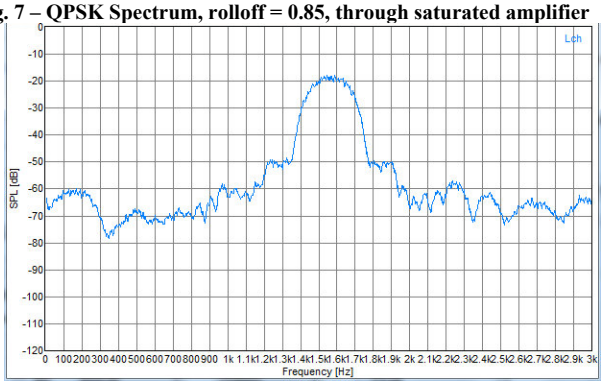

Fig. 8 – OQPSK Spectrum, rolloff = 0.85, through saturated amplifier

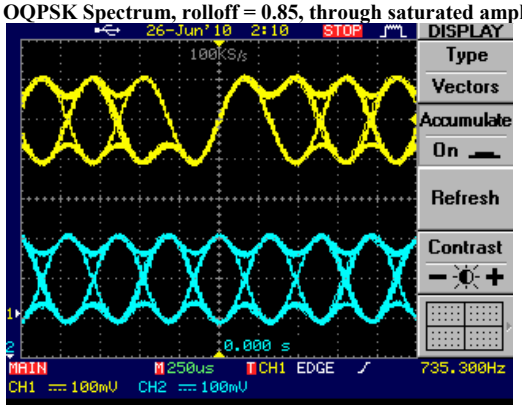

Fig. 9 – MSK eye diagram at the receiver for SNR=35 dB. *I* channel is shown on top, and *Q* channel is shown on the bottom.

analyze the spectrum of the signal, and also free oscilloscope programs exist which can be used to display the computer's audio signal. This allows a student to use the laboratory in his or her own home even if an oscilloscope and/or spectrum analyzer is not available. In universities in developing countries, where spectrum analyzers are scarce, this is quite necessary.

4.2. Receiver Structure and AWGN Channel Emulation

As in [1], the receiver structure conforms to the all-digital receiver structure in [7 Chap. 2-5], and include implementation of many of the structures in [8-20]. The AWGN (Additive White Gaussian Noise) channel emulation uses the bandpass Gaussian noise process generation method that is proposed in [4]. Accurate SNRs (from SNR = $-\infty$ dB to SNR = 40 dB) can thus be generated on the FPGA board without the need for external noise sources (note that SNR in this paper refers to E_S/N_0 where E_S is the symbol energy and $N_0/2$ is the AWGN power spectral density).

4.3. Probing and DAC/ADC Interface

The small circles on the various paths in Fig. 2 are some test points that can be channeled to the various DACs for observation via an oscilloscope or a spectrum analyzer. Many other test points are available within the various blocks and are not shown here due to space constraints. By choosing the appropriate signals the user can observe and analyze in real-time the internal signals in the transmitter, channel, and receiver.

4.4. Command and Control of the FPGA card

The FPGA card is currently controlled via a HyperTerminal connection via the RS-232. Unfortunately, this requires a high level of expertise since low-level knowledge of the FPGA's configuration is needed in order to manage the signal chains. A more user friendly Graphical User Interface (GUI) is being developed in order to make control of the laboratory easier.

4.5. Usage of the laboratory in class

In a classroom setting, the professor typically connects the laboratory to a controlling computer using an RS-232 cable, the audio output to the computer's audio input, a USB cable to an external oscilloscope (though it is possible to use a computer-based oscilloscope using the audio input in the host computer). If an external oscilloscope is used, BNC cables connect between the DAC outputs of the daughtercard to the oscilloscope inputs. The entire setup time for such a configuration is typically about 10 minutes, and is thus highly portable. In the example setup used by the author, an external GW-INSTEK oscilloscope was used and connected via USB to the computer. The computer screen is projected via a projector onto a screen in the lecture hall. Students can then follow the signal in real time by watching the oscilloscope screen capture which is projected through the computer. Similarly, they can see a connected or computer-based spectrum analyzer's screen as projected via the computer. A sample screenshot that is projected in class can be seen in Fig. 10.

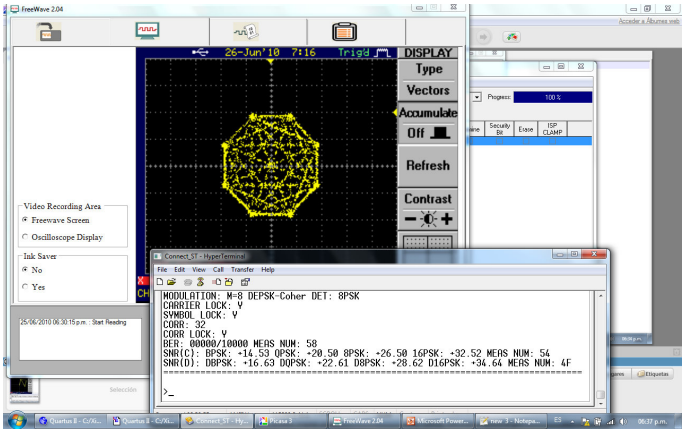

Fig. 10 - Screen capture of an example instruction session in class. The real-time capture of an external oscilloscope screen can be seen, along with the control terminal in the foreground. The oscilloscope is showing the transition diagram of an 8-PSK signal at the receiver.

5. Laboratory Graphs Examples

In this section we shall present several examples of graphs and measurements that can be generated via the laboratory. Literally thousands upon thousands of different graphs and measurements can be made using the laboratory, including all those that were presented in [1]. The reader is referred to [1] for many such examples. Here, we shall concentrate on showing examples of the new features of the laboratory, in particular the new modulations, pulse shaping, and channel amplifier saturation emulation.

In Fig. 3 we see the transition diagram at the receiver matched-filter output of *offset* QPSK with Square Root Raised Cosine pulse shaping with a rolloff factor of 0.85.

In Fig. 4 we see a QPSK signal transition diagram at the output of the receiver's matched filters for a system with Square Root Raised Cosine pulse shaping with a rolloff factor of 0.35.

In Fig. 5 we see a snapshot in time of a partially formed transition diagram at the transmitter for *offset* 16-QAM with a Square Root Raised Cosine pulse shaping with a rolloff of 0.35.

In Fig. 6 we observe the received spectrum of a QPSK or OQPSK signal with a Square-Root Raised Cosine pulse shaping with a rolloff of 0.85, for the standard case where the transmitter power amplifier is not saturated. The spectrums for OQPSK and QPSK are identical in this case. In Fig. 7 we see the measured spectrum of the same QPSK signal when the transmission amplifier is saturated, for example emulating a satellite link through a saturated transponder. Clearly, spectral growth of the secondary lobes due to saturation can be seen in Fig. 7. In Fig. 8 we see the OQPSK signal which passed through an amplifier which is saturated in the same manner. As can be seen, the OQPSK signal survives much better when passed through a saturated amplifier, as expected. This allows students to appreciate graphically, in real time, the advantage of OQPSK over QPSK in such channels [5 Sec. 5.4, 21 Chap. 6].

In Fig. 9 we see the eye diagram for MSK at the receiver. The MSK quadrature pulse shape decomposition can clearly be seen, as well as the fact that the I and Q arms are offset by one half of the symbol period.

6. Quantitative Teaching Experience Results

To quantitatively evaluate the success of the laboratory in teaching digital communications, two groups of senior undergraduate students from the UIS were surveyed. The first group, of 40 students, were taught by the author during the 2009/2010 fall/winter semester using the laboratory presented in SDR'09 [1]. The students were asked to answer a range of questions using the scale of 1 to 5 where 1 corresponds to "I completely disagree" and 5 corresponds to "I completely agree". The students were also asked to provide written observations. The

Table 2 - Survey results. The first group is of 40 students and used the laboratory [1] presented in SDR'09. The second group is of 30 students and used the new laboratory presented in this paper.

Question	SDR'09 Lab Average	SDR'09 Lab Std. Dev.	SDR'10 Lab Average	SDR'10 Lab Std. Dev.
The demonstrations done with the laboratory helped me understand the course material	3.83	0.93	4.27	1.01
Seeing the signals graphically using the laboratory is more useful than reading the course textbook	4.18	0.78	4.43	0.86
The demonstrations using the laboratory were clear	3.48	0.99	4.03	0.85
The demonstrations using the laboratory were useful	3.83	0.84	4.47	1.01
The activities and demonstrations using the laboratory were fun	3.18	1.08	3.73	0.78
The demonstrations using the laboratory incentivized me to further explore the subject of digital communications	3.70	0.94	3.77	1.10
I recommend using a similar laboratory for other courses in electronics in order to help in the teaching process	4.20	0.85	4.47	0.97
I learned more from the laboratory demonstrations than from the theoretical exposition on the blackboard	3.63	0.95	3.50	1.11
The use of this laboratory as a teaching aid must be made obligatory for teaching of this course in the future	4.10	0.84	4.43	1.10
The demonstrations using the laboratory were pretty	3.35	0.92	3.87	1.04
I like the subject of digital communications	3.93	0.86	4.03	0.85
The professor Yair Linn taught the course well	3.55	1.06	4.33	0.92
Average	**3.75**	**0.92**	**4.10**	**0.96**

second group of students surveyed was taught using the new laboratory presented in this paper during the 2010 spring semester. They were asked to respond to an identical questionnaire in order to evaluate the new laboratory. For both groups, it was emphasized to the students that the survey is anonymous and would not affect their grades. All surveys were conducted in Spanish, which was also the language in which the courses were taught.

The results of the surveys are summarized in Table 2. As can be seen there, the students were generally enthusiastic about both laboratories, as evident from the fact that all of the average marks are above 3 and many times above 4 (on a scale of 1 to 5). In total, the average mark given to the laboratory of SDR'09 is 3.75, whilst the average mark for the new laboratory presented here is 4.10. Both are excellent marks, and the new laboratory received better marks both in the average sense and also for nearly all individual questions. The low standard deviations show that the satisfaction from the laboratories was rather uniform among the student body.

In their written comments, the students generally praised the laboratory as something that significantly aided their comprehension of the subject matter, and were enthusiastic about the laboratory-assisted learning methodology. As for criticisms and suggestions, some students expressed their desire to be able to use the laboratory themselves instead of watching demonstrations by the professor. Some students also wanted a laboratory experiment guide to be written for this purpose. These issues are to be addressed in the continuing development of the laboratory.

7. Miscellaneous Demonstrations

After the references of this paper, many oscilloscope and spectrum analyzer screenshots are included, along with brief captions. These screenshots show only a small subset of the thousands of laboratory experiments, measurements and demonstrations that can be done using the current laboratory, which, as can be seen, rivals or even surpasses what can be done using many commercially available laboratories, many of which cost tens of thousands of dollars, i.e. orders of magnitude more than the system presented in this paper.

8. Conclusions

In this paper we presented a new laboratory for the teaching of digital communications for a senior undergraduate course. The laboratory is a further development of a laboratory that was presented in SDR'09. The new laboratory provides many enhancements, which was achieved using a different, more powerful FPGA. Survey results conducted to assess the efficacy of the current and former laboratory show that both laboratories have a positive and notable impact on the students' learning experience. Comparing survey results, it is seen that the new laboratory scores higher than the previous one. Since the new laboratory has an ultra-low cost ($550) and uses COTS parts, it is suitable for immediate deployment around the world. The necessary FPGA configuration files can be made available by contacting the author.

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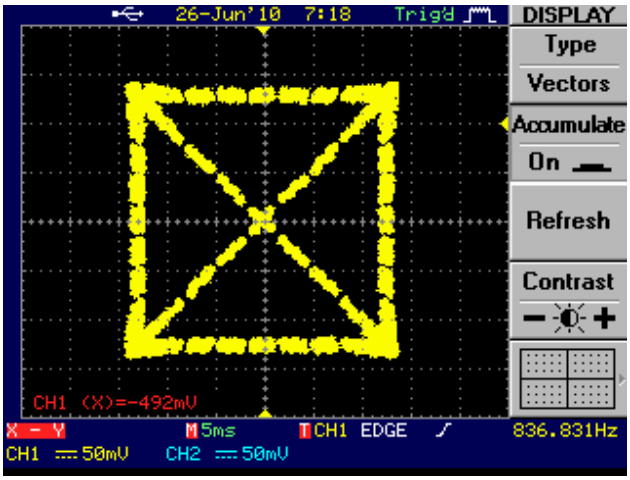

Fig. 11 – QPSK transition diagram at the receiver, SNR = 35 dB.

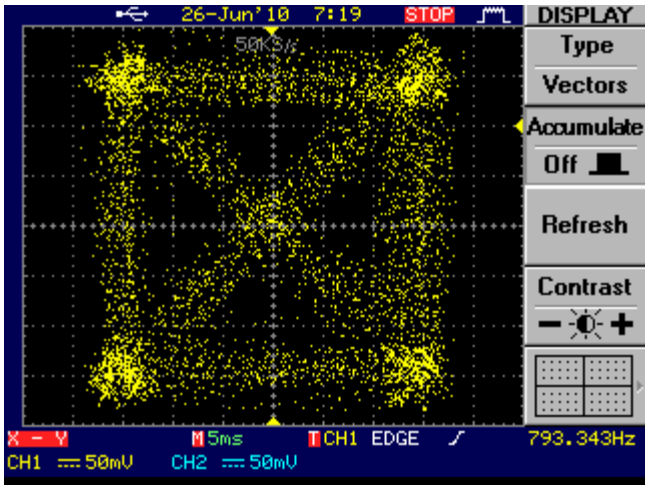

Fig. 12 – QPSK transition diagram at the receiver, SNR = 18 dB.

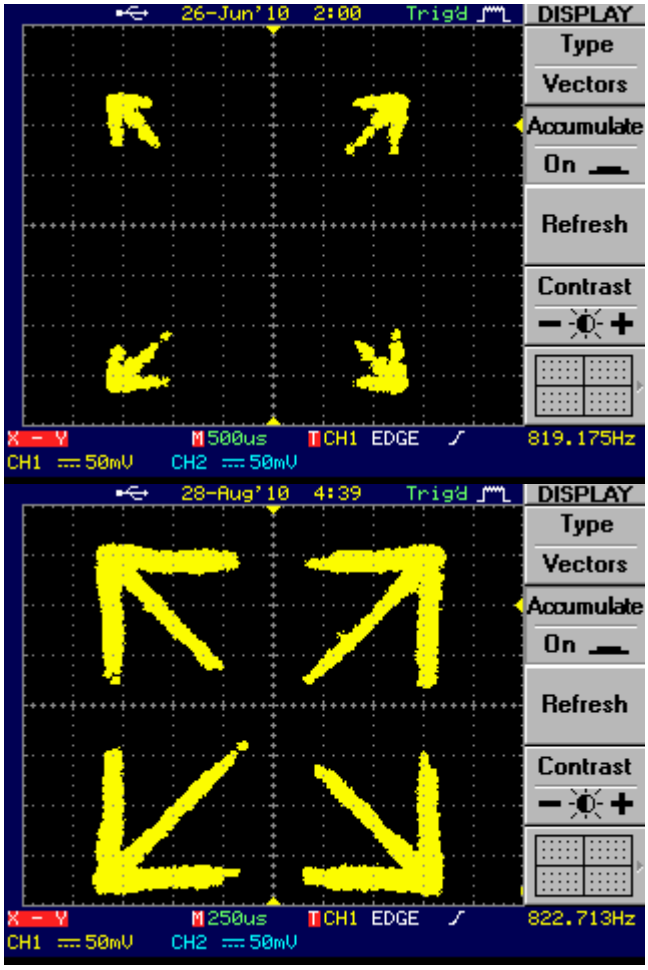

Fig. 13 - QPSK constellation at the receiver, SNR = 35 dB, but with significant symbol synchronization PLL jitter (i.e., non-ideal timing recovery). Top: moderate amount of timing jitter. Bottom: severe amount of timing jitter. Note how the non-ideal timing recovery causes the constellation diagram to partially draw the transition diagram, when the measurements are accumulated.

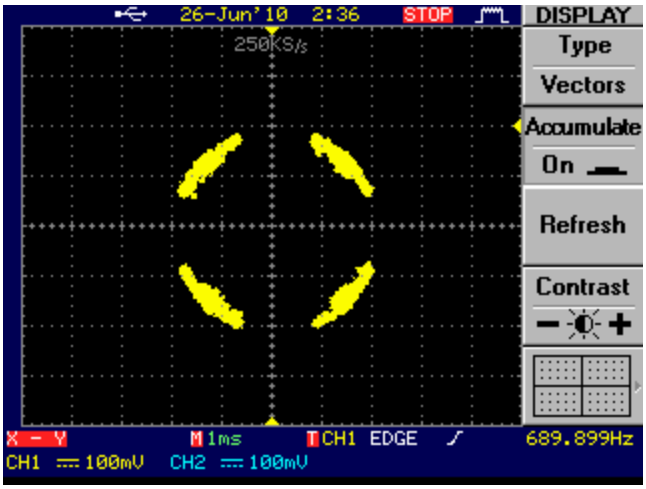

Fig. 14 – QPSK constellation at the receiver, SNR = 35 dB, but with significant carrier PLL jitter (i.e. non-ideal carrier recovery).

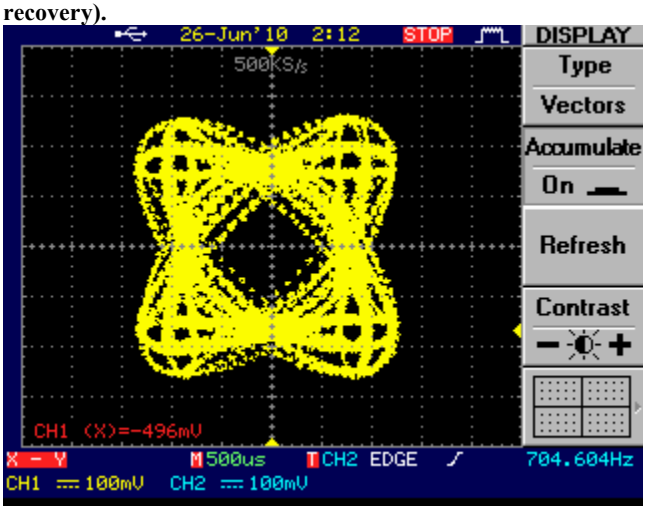

Fig. 15 – Transition diagram at the transmitter of OQPSK with SRRC pulse shaping with rolloff factor of 0.35

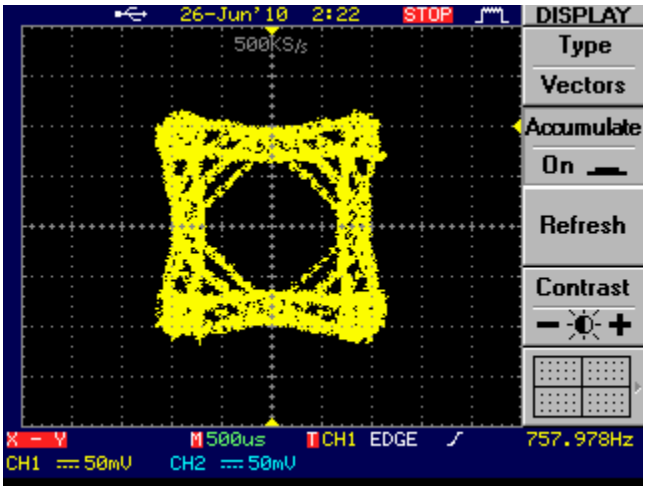

Fig. 16 - Transition diagram at the transmitter of OQPSK with SRRC pulse shaping with rolloff factor of 0.85

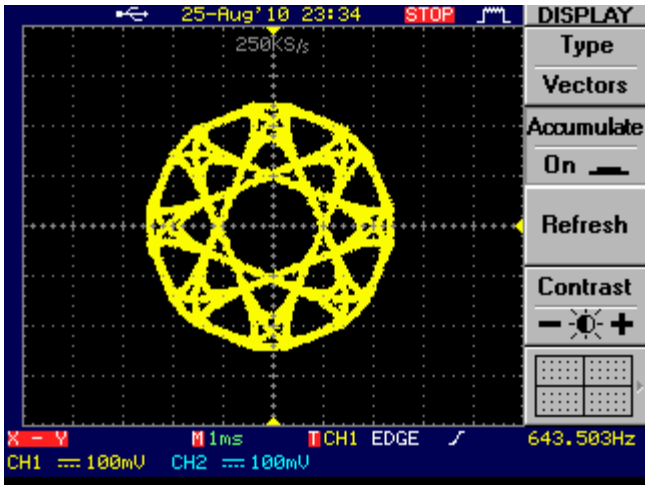

Fig. 17 - Transition diagram at the receiver of $\pi/4$-QPSK with Gaussian pulse shaping, SNR = 35 dB.

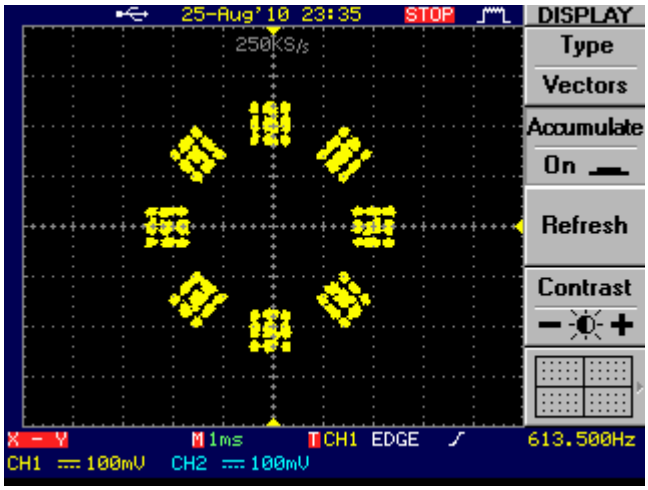

Fig. 18 – Constellation diagram at the receiver of $\pi/4$-QPSK with Gaussian pulse shaping, SNR = 35 dB. Note the evident ISI (Inter-Symbol Interference) which is inherent to Gaussian pulse shaping.

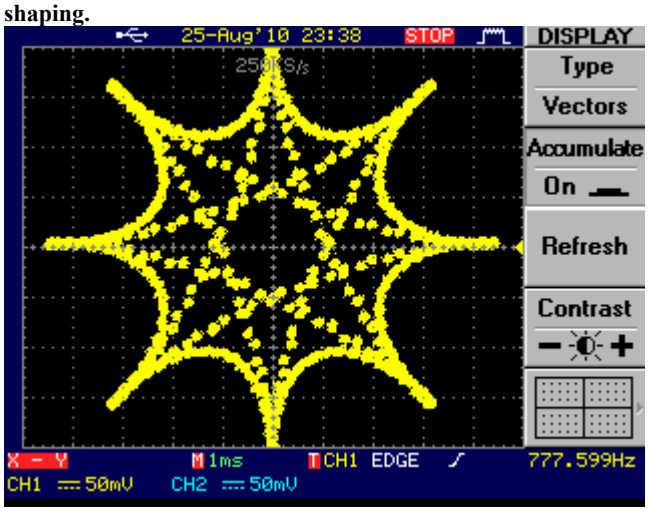

Fig. 19 – Transition diagram at the receiver of $\pi/4$ - QPSK with half-sinusoid pulse shape, SNR=35 dB.

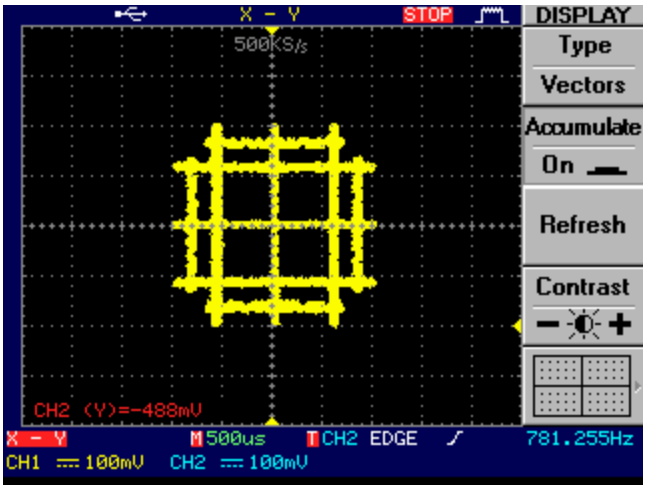

Fig. 20 - Transition diagram at the transmitter of Offset $\pi/4$-QPSK, rectangular pulse shape (note the small overshoots, due to filter imperfections in the multirate modulator signal chain).

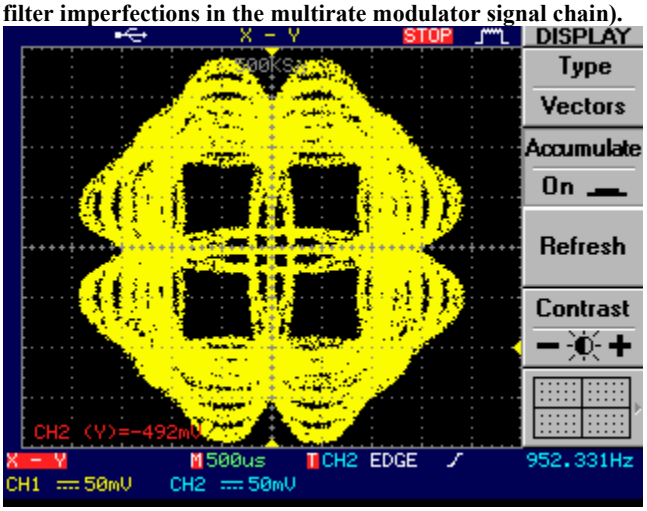

Fig. 21 - Transition diagram at the transmitter of Offset $\pi/4$-QPSK with SRRC pulse shaping with rolloff factor of 0.35.

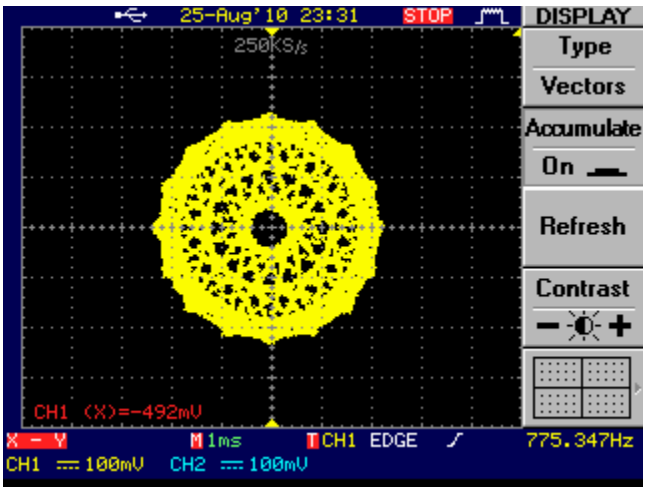

Fig. 22 - $\pi/8$- 8PSK transition diagram at the receiver, rectangular pulse shape, SNR = 35 dB.

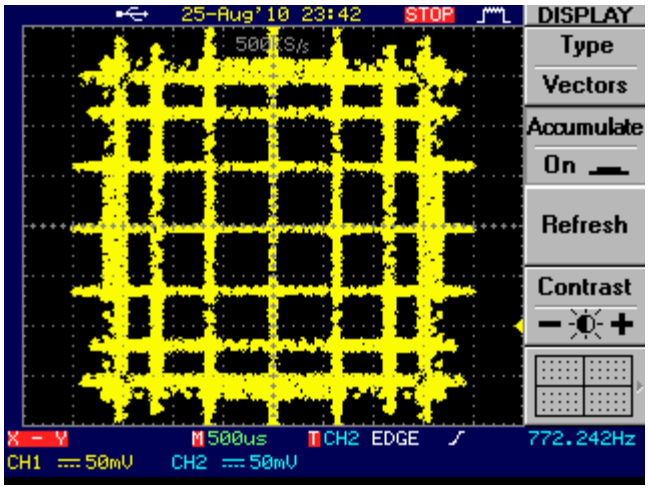

Fig. 23 - Transition diagram at the transmitter of Offset $\pi/8$-8PSK with rectangular pulse shape (note the small overshoots due to filter imperfections in the multirate modulator signal chain).

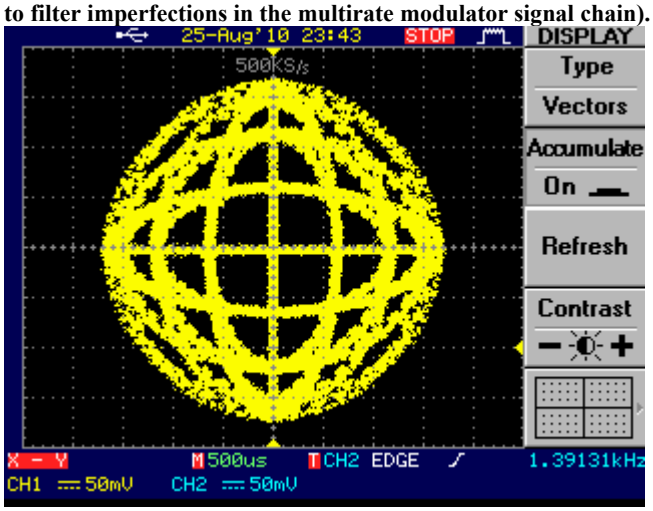

Fig. 24 - Transition diagram at the transmitter of Offset $\pi/8$-8PSK with half-sinusoid pulse shape.

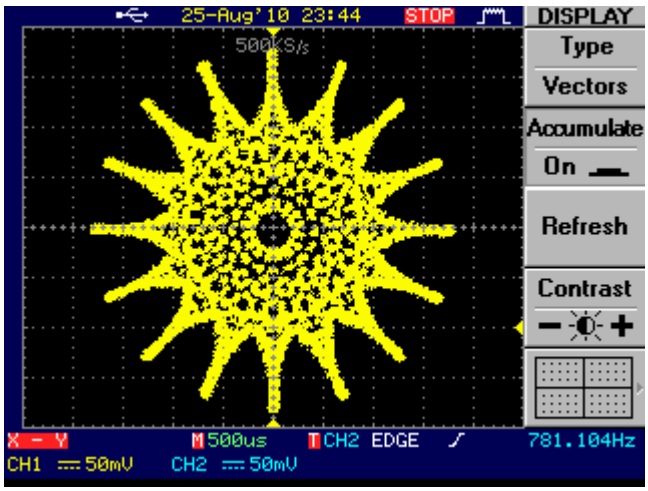

Fig. 25 - Transition diagram at the receiver of Offset $\pi/8$-8PSK with half-sinusoid pulse shape, SNR=35 dB.

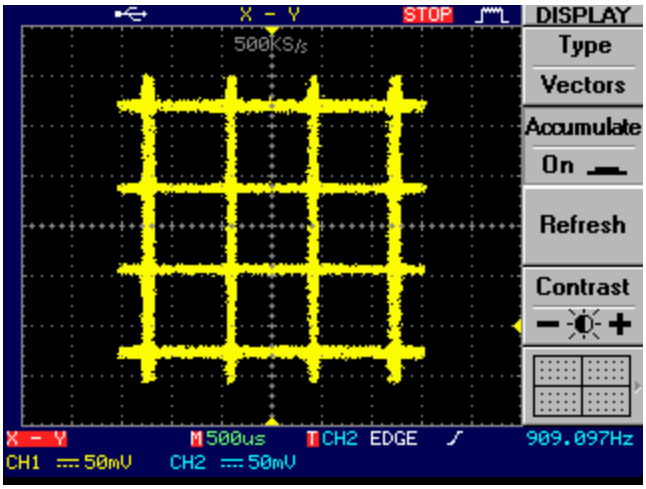

Fig. 26 – Offset QAM-16 transition diagram at the transmitter, rectangular pulse shape (note the small overshoots, due to filter imperfections in the multirate modulator signal chain).

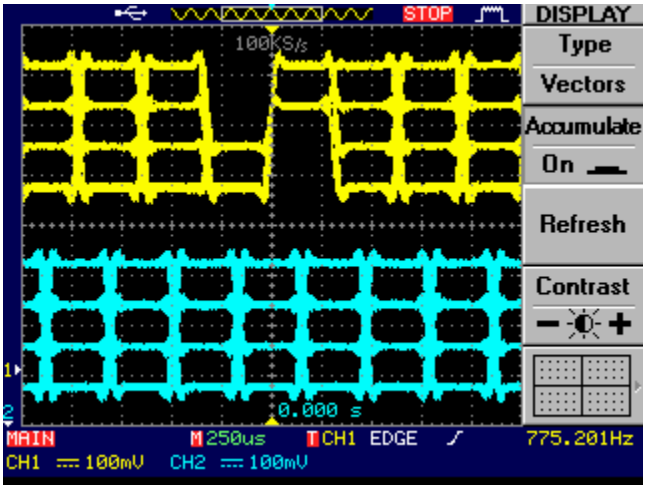

Fig. 27 – Offset QAM-16 eye diagram for I and Q channels at the transmitter, rectangular pulse shape.

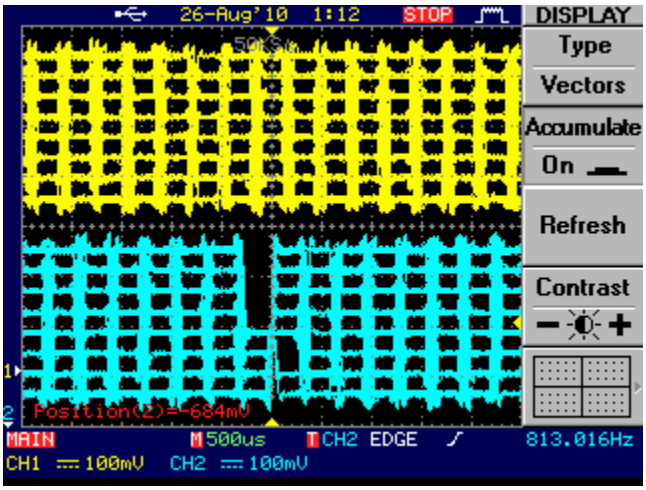

Fig. 28 - Offset QAM-64 eye diagrams for I and Q channels at the transmitter, rectangular pulse shape.

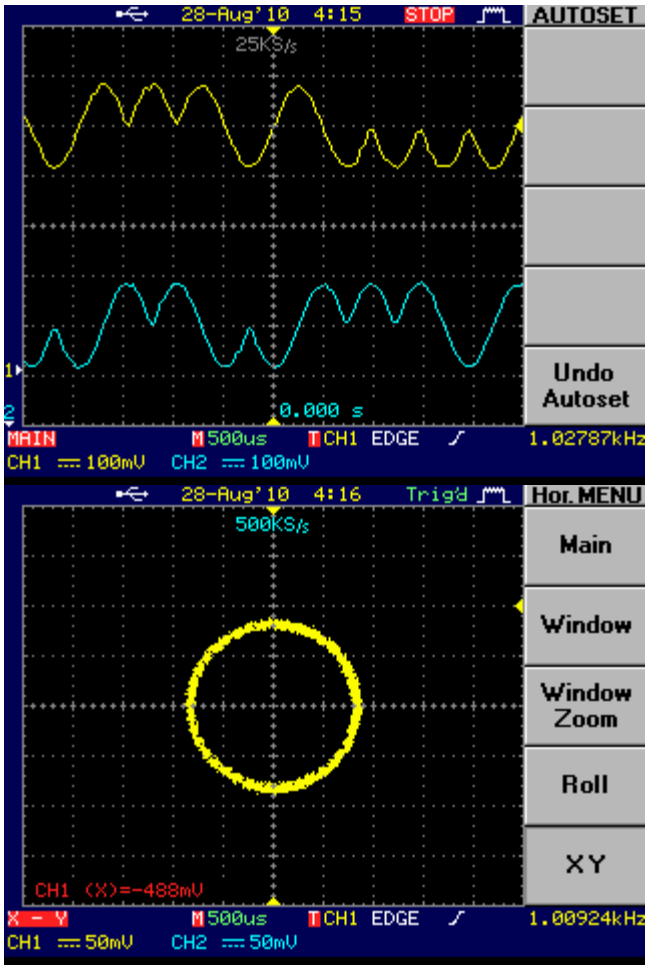

Fig. 29 – Top: I-Q arms at transmitter of MSK, clearly showing MSK as an OQPSK signal with half-sinusoid baseband pulse shape. Bottom: X-Y graph of the same I-Q signals, which clearly shows the constant-envelope property of MSK.

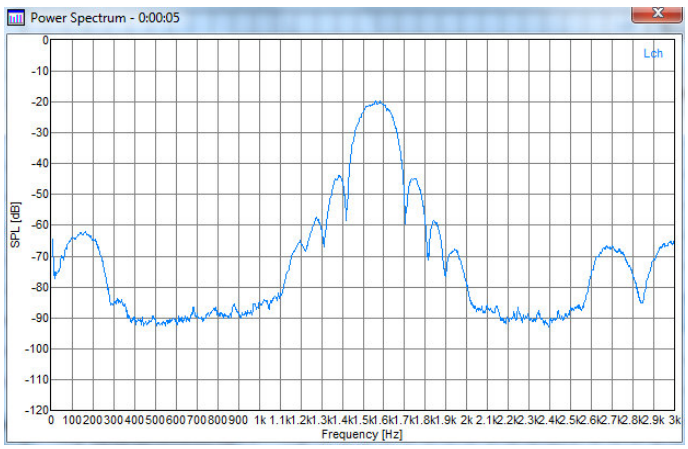

Fig. 30 – GMSK spectrum at output of transmitter, for BT = 0.8.