A CONTINUOUS-TIME COMPLEX BANDPASS SIGMA-DELTA ADC FOR SOFTWARE DEFINED RADIO

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ABSTRACT

A digitally enhanced sigma-delta ADC for narrowband LTE/WiMAX wireless receivers is proposed. A 5th order 2-bit continuous-time complex bandpass sigma-delta modulator is used to achieve the required dynamic range, attenuate the interferers, reject the image and meet power dissipation and area constraints imposed by mobile devices. Dithering and adaptive line enhancement techniques are employed to compensate for I/Q channel mismatch. The simulation results after calibration show an improvement of 16.93 dB in SINAD and 21.6 dB in image rejection.

1. INTRODUCTION

Software defined radio (SDR) technology has expanded from military to commercial applications, however, until recently, it worked only in applications which didn't need to have small area and low power consumption. Nowadays, new technologies allow the SDR implementation in mobile devices providing small area and low power consumption.

In this paper, a digitally enhanced continuous-time (CT) quadrature bandpass (BP) sigma-delta (ΣΔ) analog-to-digital converter (ADC) for SDR receivers is presented. Section 2 introduces the targeted standards and suitable receiver architecture along with a system level analysis performed to determine the ADC requirements. The design and simulation results of the proposed CT quadrature BP ΣΔ modulator topology for narrow bands WiMAX/LTE are presented in Section 3. Section 4 introduces the dither and adaptive line enhancement techniques employed to calibrate the ADC. Finally, in Section 5 the paper is concluded.

2. SYSTEM OVERVIEW

The future mobile radios should be able to integrate WiMAX/LTE standards in order to take advantage of the latest developments in mobile communications. This generates the need of novel designs that can support the standards stringent requirements while achieving low-cost and low power by using nanometer CMOS technologies.

2.1. Receiver Architecture

The standards targeted in this work are the narrowband channels of Long Term Evolution (LTE) [1] as well Worldwide Interoperability for Microwave Access (WiMAX) [2]. Both standards employ, in the downlink, high-spectral efficiency Orthogonal Frequency Division Multiple Access (OFDMA) modulations, such as Quadrature Phase Shift Keying (QPSK), 16 Quadrature Amplitude Modulation (QAM) and 256 QAM with scalable bandwidths ranging from 1.4 MHz (LTE) up to 20MHz (WiMAX). Furthermore, LTE should provide backward compatibility to legacy standards such as Global (GSM) and Universal Mobile Communication System (UMTS).

Two types of receiver architectures are mainly used nowadays in mobile wireless applications primarily depending on the characteristics of the input signal: Zero-Intermediate frequency (IF) [3] and Low-IF [4]. Zero-IF architecture is generally preferred due to its relative low complexity and its negligible image problem. However, because of its disadvantages in terms of sensitivity to DC offsets, flicker noise, and second order intermodulation (IM2) products [5], it might not be the optimum selection in certain conditions, such as narrowband channels or input signals that after down-conversion have most of their power close to DC. These conditions would impose very stringent or sometimes unachievable requirements on some of the receiver blocks. Low-IF topology, on the other hand, moves the wanted signal away from DC so as to mitigate DC offsets, flicker noise and IM2 products problems. It does, however, suffer from image rejection (IR) problems [6]. The latter topology has been chosen in this work due to the narrowband nature of the chosen channels.

2.2. ADC Architecture

Once the receiver architecture has been selected, the key requirements of the receiver building blocks, including the ADC need to be determined.

The required 75dB signal-to-noise-and-distortion ratio (SINAD) for the ADC [7] in the low-IF receiver was determined by taking into consideration [8]: (a) the

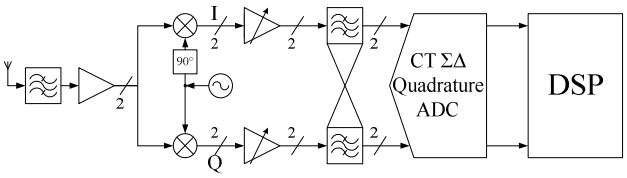

Fig. 1. Proposed low-IF receiver architecture for narrowband LTE/WiMAX applications.

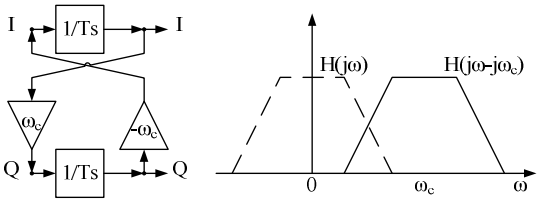

Fig. 2. Realization of a complex pole.

minimum required signal-to-noise ratio (SNR), plus some margin, in order to achieve the necessary bit-error-rate (BER)/percentage-of-throughput figure-of-merit (FOM), (b) margin to account for Raleigh fading so as to relax the automatic gain control (AGC) block bandwidth requirements, (c) margin to account for the envelope variations of OFDMA signals, and (d) margin due to blockers that were not completely filtered after the channel selection.

The signal bandwidth of 1.6 MHz is set accounting for all WiMAX/LTE narrowband channels supported by the low-IF architecture. Although not covered in this publication, it is worth to mention that it might be advantageous to slide the IF and modify the bandwidth of the ADC accordingly in order to save power.

Low-IF analog-to-digital conversion of I and Q signals can either be performed by using two real BP ΣΔ ADCs [4] or by using one complex BP ΣΔ ADC [9-11]. The latter structure is chosen due to its advantages of half area and less power consumption with respect to the former one. The proposed low-IF receiver architecture including the complex BP ADC is shown in Fig. 1.

In order to achieve low-cost, low-power, multi-standard mobile wireless devices for SDR, CMOS is the most suitable technology since it supports higher integration and performance levels for digital and mixed signal circuits. While CMOS technology scaling to nanometer levels have resulted in great advances in the digital area, such as the possibility to integrate high-count, low-cost blocks, the analog part of the wireless devices remains the main bottleneck. The analog performance is highly susceptible to random variations in process and operating conditions which do not scale with the process. Therefore, novel approaches to enhance the RF/analog performance are required to be proposed. Digital calibration is used in this work as a technique to mitigate such drawbacks by exploiting the advantages in nanometer technology.

3. CT COMPLEX BP ΣΔ MODULATOR DESIGN

A CT implementation has been chosen for the complex BP ΣΔ modulator, due to its advantages when compared to its discrete time (DT) counterpart. The key advantage of the CT implementation is that the sampling errors of the sample and hold (S/H) circuit are shaped as quantization noise since the S/H is placed inside the loop. Another advantage is that a CT circuit can operate at higher frequencies, as the sampling frequency is not limited by the charge transfer accuracy requirements. Moreover, the tuning frequency of a CT filter does not depend on the sampling frequency and a CT

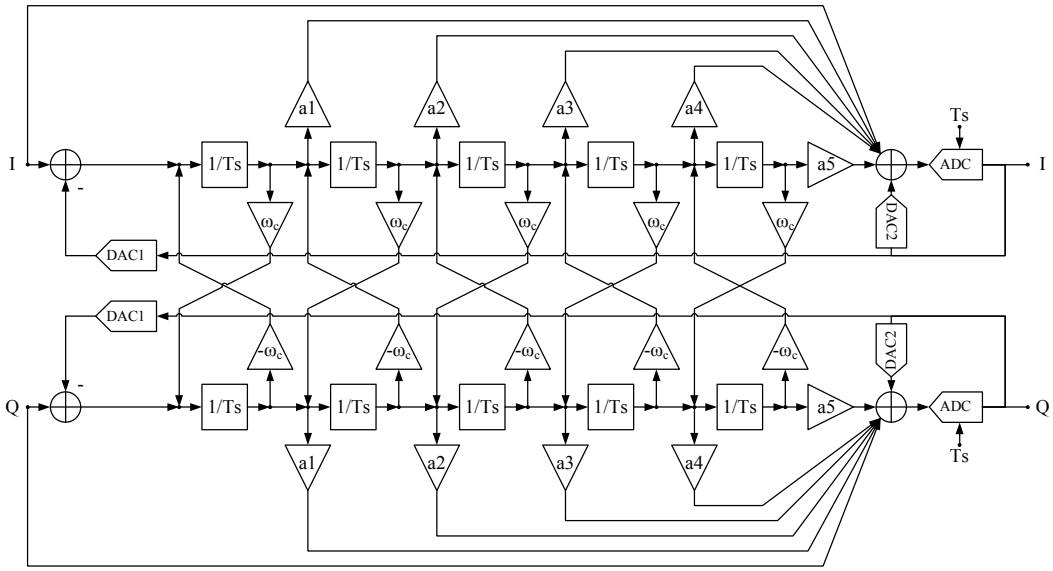

Fig. 3. Proposed 5th order 2-bit CT complex BP ΣΔ modulator (single-ended version).

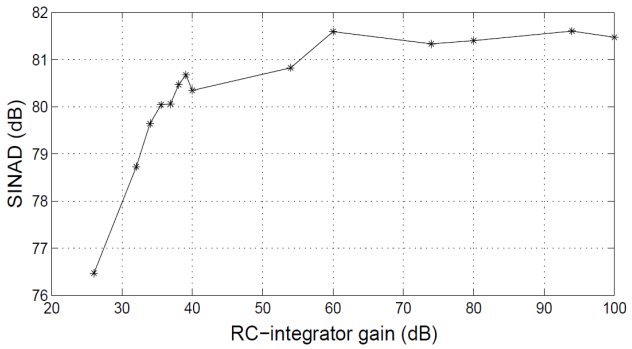

Fig. 4. SINAD vs amplifier finite gain of the RC-integrators.

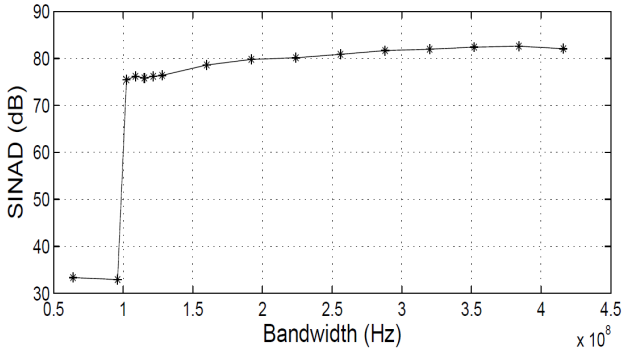

Fig. 5. SINAD vs amplifier finite gain-bandwidth product of the RC - integrators.

bandpass loop filter can be tuned at a frequency other than $f_s/4$ without requiring additional hardware. However, issues such as clock jitter, excess loop delay and loop filter accuracy become great challenges to the designer, especially at high sampling frequency. Therefore, special techniques should be applied to overcome these problems.

3.1. ΣΔ Modulator Topology

The complex BP ΣΔ ADC handles two real inputs as a complex signal (X=X1+jX2) and provides two real output signals that are combined together to provide a complex output. Furthermore, a complex filter transfer function can be simply generated by shifting in frequency the transfer function of a real low-pass filter. This frequency shift is obtained, for a continuous time filter, by applying the transformation:

$$s \Rightarrow s - j\omega_c \tag{1}$$

Such transformation is realized by duplicating the aforementioned low-pass filter and cross-coupling the two paths, as shown in Fig. 2.

The topology selection started with the low-pass ΣΔ modulator and takes into account the application requirements along with the trade-offs given by the theoretical Dynamic Range (DR):

$$\mathrm{DR}[dB] = 10\log\left(\frac{3}{2}\cdot\left(\frac{2\mathrm{L}+1}{\pi^{2\mathrm{L}}}\right)\cdot \mathrm{M}^{2\mathrm{L}+1}\cdot\left(2^{\mathrm{B}}-1\right)^2\right) \tag{2}$$

Later on, the selection was furthered refined by considering, at system level, the non-idealities described in the next section. Accordingly, a 5th order 2-bit CT ΣΔ modulator with an oversampling ratio (OSR) of 20 was chosen in order to achieve the required SINAD and IR and to meet the power dissipation and area constraints imposed by mobile devices. The cascade integrator feedforward (CIFF) topology has been chosen because of its better linearity and reduced output swing which makes it more suitable for low-voltage low-power applications. The selected low-pass modulator was then duplicated and cross-coupled to build the 5th order 2-bit CT quadrature ΣΔ ADC, as shown on Fig. 3.

Table 1. Specifications of the RC-integrators

Specification	Value
Transconductance	640 uA/V
DC Voltage Gain	40 dB
R_integrator	7.81 KOhm
C_integrator	2 pF
R_out (RO)	156.2 KOhm
C_load (CL)	20 fF
C_parasitc (CT)	20 fF
GBW	320 MHz

Table 2. Specifications of the Gm-C integrators

Specification	Value
Transconductance	64 uA/V
DC Voltage Gain	32 dB
C_integrator	1 pF
C_parasitc (CT)	10 fF

In order to cover all LTE/WiMAX narrowbands, a signal bandwidth of 1.6 MHz around an intermediate frequency of 0.85 MHz has been chosen, providing 50 KHz spacing from DC so as to mitigate DC offsets, flicker noise and IM2 products.

3.2. Non-ideal behavior

The critical blocks are the loop filter, especially the first integrator, as well as the feedback digital-to-analog Converter (DAC). In order to estimate the ΣΔ modulator performance and establish the required circuit specifications, the main circuit non-idealities were included in the MATLAB behavioral model by using Simsides [12].

The error in the loop filter comes mainly from two sources: the non-idealities in the amplifiers, such as finite DC gain and finite bandwidth, and the variations in RC and Gm-C products which create discrepancies in the

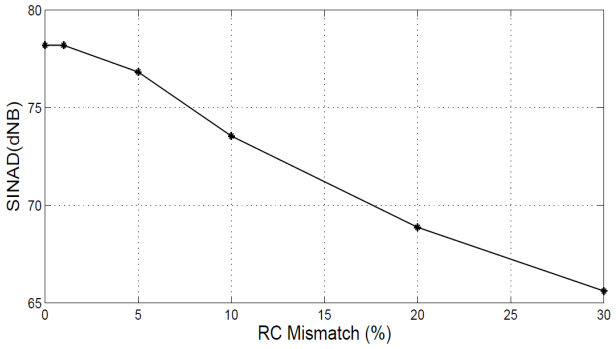

Fig. 6. SINAD vs RC coefficient mismatch.

coefficients. Due to linearity and power dissipation constraints, the first integrator was implemented as an active-RC, while the rest of them were realized as Gm-C. As the distortion on each integrator stage will be suppressed by the gain of the previous stage, the impact that the first integrator will have on the ΣΔ modulator is greater than the rest of them and its circuits non-idealities has to be carefully examined. Fig. 4 and 5 show the impact in the ΣΔ modulator SINAD of the active-RC non-idealities in the amplifier. Similar simulations were performed for the Gm-C integrators which contributed to the specifications depicted in Table 1 and 2.

Resistors and capacitors values can typically change 20% and 10% respectively due to process, voltage and temperature (PVT) variations which can lead to coefficient variations of up to 30% in active-RC integrators. Fig. 6 shows the impact in the ΣΔ modulator SINAD of such variations. From this figure it is already possible to appreciate the need of calibration, as the modulator would not comply with the SINAD specifications when accounting for PVT variations.

The most relevant DAC non-idealities come from the timing errors in the feedback pulse and from non-linearities when using multi-bit DAC. The high-sensitivity to timing errors turns the DAC implementation extremely critical for the overall CT ΣΔ ADC performance. Such timing errors can be further divided in excess loop delay (ELD) and clock jitter. ELD sensitivity is compensated by introducing a second DAC, half clock delayed, feeding back to the quantizer input [13]. Moreover, jitter sensitivity is alleviated by using multi-bit quantization and Non-Return-to-Zero (NRZ) coding schemes. Having a multi-bit quantizer requires a multi-bit DAC in the feedback path which, as stated before, will suffer from non-linearities. Gain error, integral non-linearity (INL) and DC offset were included in the DAC behavioral model and several combinations were tested in order to finally select a 2-bit quantizer as a compromise between jitter sensitivity and DAC non-linearity.

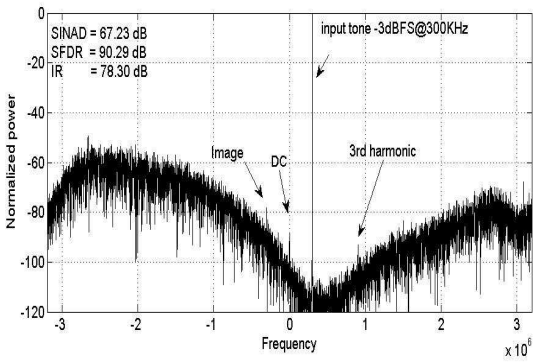

Fig. 7. Modulator output power spectrum when accounting for non-idealities.

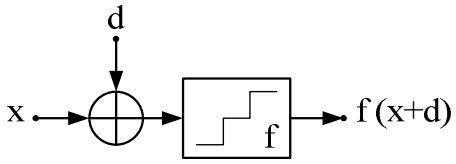

Fig. 8. Dithering technique.

The ΣΔ ADC performance was determined when all critical non-idealities were included. Fig. 7 shows the output power spectral density (PSD) when accounting for random variations of 30% in the RC integrators, 10% in the feedforward coefficients and 0.1% DAC mismatch. The simulation results confirm the need for calibration in order to comply with the WiMAX/LTE specifications. The modulator has also been implemented at behavioral level in Cadence-AHDL, with the first I and Q integrators implemented at circuit level. The simulation results show good agreement with the behavioral level simulation results from MATLAB.

4. DIGITALLY ENCHANCEMENT TECHNIQUES

Dithering and adaptive filtering calibration techniques were combined so as to compensate for distortion and noise [14]. Therefore, design constraints can be relaxed and large process variation can be tolerated without degrading the required performance of the ADC. Both techniques will be discussed in the following sections.

4.1. Dithering

Dithering is used in many applications so as to reduce the quantization error and improve the ADC performance. Dithering is performed by randomizing the least significant bit (LSB) which leads to a whitening of the quantization error in the output spectrum. In addition to this, dithering decorrelates the signal from the noise, resulting in a decrease of harmonic distortion [15] [16].

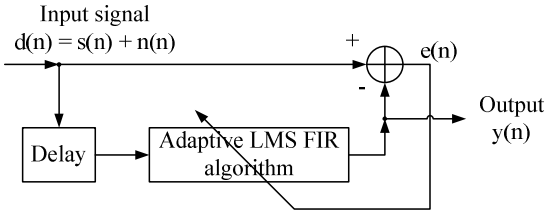

Fig. 9. ALE adaptive filtering technique.

The randomization is done by adding a dither signal *d* before the quantizer as shown in Fig. 8. Eq. (3) defines the dither averaged power of an ideal quantizer:

$$f(x) = \int_{-\inf}^{\inf} f(x+d) * p(d) \cdot dx \qquad (3)$$

where *f(x)* defines the transfer function and *p(d)* the power density function (PDF) of the dither signal.

When a dither signal *d* is added to the input signal *x*, the observed average quantization error function *q(x)* is:

$$\overline{q(x)} = \int_{-\inf}^{\inf} q(x+d) * p(d) \cdot dx \qquad (4)$$

Three types of PDF were simulated in this work: rectangular PDF (RPDF), triangular PDF (TPDF) and Gaussian PDF (GPDF). Simulations based on (4) showed that GPDF and TRDF suppress the harmonics more than RPDF for the same dither level, although RPDF has better linearity [16]. From implementation point of view it is easier to implement TPDF than GPDF. Therefore a TPDF dither with a power of lsb/2 has been used.

It is worth to notice that, once the dithering method has been applied, the linearity improves but the overall noise floor increases. Since the distortion is spread into the band as white noise, an extra calibration technique, such as adaptive filtering, is needed in order to compensate for this increment.

4.2. Adaptive Filtering

Adaptive line enhancement (ALE) [17] [18] type of adaptive filtering is used in this application in order to mitigate the noise floor increment.

As shown on Fig. 9, the input to the ALE is a delayed version, *d(n-1)* of d(n) composed by the desired signal, *s(n)* and the additional noise, *n(n)*. The adaptive filter attempts to generate a copy, *y(n)*, of the desired signal, which is then subtracted from the *d(n)*, resulting in a pure noise output signal *e(n)* which is used as a reference to tune the filter. The mean squared of this error is given by:

$$E\left[e^2\right] = E\left[(d-y)^2\right] = E\left[(s+n-y)^2\right] \qquad (5)$$

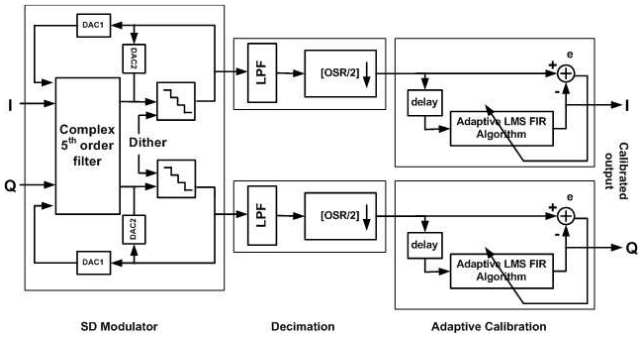

Fig. 10. Block diagram of calibrated sigma-delta ADC.

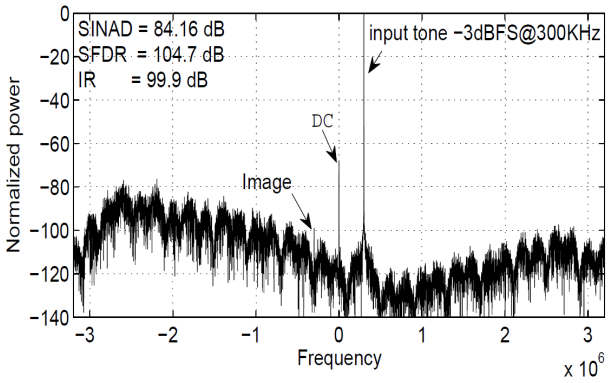

Fig. 11. Modulator output power spectrum after calibration.

which results in:

$$E\left[e^2\right] = E\left[(s-y)^2\right] + E\left[n^2\right] + 2 \cdot E\left[n \cdot (s-y)\right] \qquad (6)$$

The adaptive filter uses a least mean squared (LMS) finite impulse response (FIR) algorithm so as to minimize Eq. (6). The ALE is applied to the complex output of the ADC after the decimation filter and it introduces little extra complexity to design of the ADC.

The block diagram of the ADC with both calibration techniques included is shown in Fig. 10. As stated before, it combines dithering with ALE techniques so as to exploit the advantages and compensate the drawbacks of each other. Fig. 11 shows the PSD when both calibration methods were implemented in MATLAB. It can be seen an improvement of 16.93 dB in SINAD and 21.6 dB in IR when compared with the un-calibrated ΣΔ ADC.

5. CONCLUSIONS

A digitally enhanced 5th order 2-bit CT complex BP ΣΔ ADC for narrowband LTE/WiMAX has been proposed. Simulation results, where I & Q mismatches were introduced, confirmed the need for calibration in order to comply with stringent WiMAX/LTE requirements. Dithering and adaptive filtering techniques were employed to compensate for I/Q channel mismatch. The calibrated ΣΔ

ADC enables an improvement of 16.93 dB in SINAD and 21.6 dB in image rejection.

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7. REFERENCES

[1] 3rd Generation Partnership Project, "User Equipment (UE) radio transmission and reception," TSG RAN, 3GPP TS 36.101 V8.0.0 (2007-12), 2007.

[2] "mobile WiMAX Technical Specifications: IEEE Std 802.16e-2005-Amendment to IEEE Standard for Local and Metropolitan Area Networks - Part 16: Air Interface for Fixed Broadband Wireless Access Systems- Physical and Medium Access Control Layers for Combined Fixed and Mobile Operation in Licensed Bands", 2006.

[3] A.A. Abidi, "Direct-conversion radio transceivers for digital communications," *Solid-State Circuits, IEEE Journal of* , vol.30, no.12, pp.1399-1410, Dec 1995.

[4] J. Crols and M.S.J. Steyaert, "Low-IF topologies for high-performance analog front ends of fully integrated receivers," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on* , vol.45, no.3, pp.269-282, Mar 1998.

[5] B. Razavi, "Design considerations for direct-conversion receivers," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on* , vol.44, no.6, pp.428-435, Jun 1997.

[6] J. Groe , "A Multimode Cellular Radio," *Circuits and Systems II: Express Briefs, IEEE Transactions on* , vol.55, no.3, pp.269-273, March 2008.

[7] S. Rodriguez, A. Rusu, and M. Ismail, "Design considerations for 4g nanometer radio receivers," *IEEE ISSCS 2009*, Iasi, July 9-10, 2009 (in press).

[8] D. K. Shaeffer, "WiMAX receiver architectures and challenges", 4th RaMSiS Summer School, 2008.

[9] L.J. Breems, R. Rutten, R.H.M. van Veldhoven and G. van der Weide, "A 56 mW Continuous-Time Quadrature Cascaded ΣΔ Modulator With 77 dB DR in a Near Zero-IF 20 MHz Band," *Solid-State Circuits, IEEE Journal of* , vol.42, no.12, pp.2696-2705, Dec. 2007.

[10] R. Schreier, N. Abaskharoun, H. Shibata, D. Paterson, S. Rose, I. Mehr and Q. Luu, "A 375-mW Quadrature Bandpass ΣΔ ADC With 8.5-MHz BW and 90-dB DR at 44 MHz," *Solid-State Circuits, IEEE Journal of* , vol.41, no.12, pp.2632-2640, Dec. 2006.

[11] S. Jantzi, K. Martin, and A. Sedra, "Quadrature bandpass sigma-delta modulation for digital radio," *Solid-State Circuits, IEEE Journal of* , vol. 32, no. 12, pp. 1935-1950, Dec 1997.

[12] J. Ruiz-Amaya and J. de la Rosa, "Simsides," High-Performance Analog and Mixed-Signal IC Design Group Institute of Microelectronics of Seville, 2002.

[13] S. Yan and E. Sanchez-Sinencio, "A continuous-time sigma-delta modulator with 88-db dynamic range and 1.1-mhz signal bandwidth," *Solid-State Circuits, IEEE Journal of* , vol. 39, no. 1, pp. 75–86, Jan. 2004.

[14] A. Leonida, O. Hazar and A. Rusu, "A digitally calibrated CT Quadrature Bandpass ΣΔ ADC for WiMAX/LTE", IEEE *Signals, Circuits and Systems, 2009. ISSCS 2009. International Symposium on* , in press, July 2009.

[15] P. Carbone and D. Petri, "Effect of additive dither on the resolution of ideal quantizers," *Instrumentation and Measurement, IEEE Transactions on* , vol. 43, no. 3, pp. 389–396, Jun 1994.

[16] M. Wagdy, "Effect of various dither forms on quantization errors of ideal a/d converters," *Instrumentation and Measurement, IEEE Transactions on* , vol. 38, no. 4, pp. 850–855, Aug 1989.

[17] B. Farahani and M. Ismail, "Adaptive sigma delta adc for wimax fixed point wireless applications," *48th Midwest Symposium on Circuits and Systems*, pp. 692–695 Vol. 1, Aug. 2005.

[18] L. Yu and W. M. Snelgrove, "A novel adaptive mismatch cancellation system for quadrature if radio receivers," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 46, no. 6, pp. 789–800, June 1999.