ENERGY EFFICIENT ANALOG-TO-DIGITAL CONVERTERS FOR SOFTWARE DEFINED RADIO

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ABSTRACT

Recent advances in the area of power-efficient analog-to-digital converters (ADC) for software-defined radio (SDR) front-ends are presented. A novel charge-sharing successive approximation (SAR) ADC architecture eliminates all power bottlenecks of the classical SAR implementation and reaches a figure of merit (FoM) of only 54fJ/conversion-step. As a converter that requires less analog baseband filtering, a multi-mode reconfigurable continuous-time (CT) sigma-delta (ΣΔ) ADC is presented that reaches up to 10MHz bandwidth and retains low power consumption over all modes. Finally, as a demonstrator for a true ADC-at-the-antenna system, a 6th order RF bandpass Sigma-Delta ADC operating on the 2.4 GHz ISM band suitable for direct RF sampling is proposed.

1. INTRODUCTION

The increasing number of wireless standards drives the need for flexible receiver systems that can operate optimally in different modes. Such a fully reconfigurable receiver should handle present and future standards seamlessly and should not consume more power than required by the desired quality of service and channel conditions. A critical building block to address this challenge is the ADC as it enables to exploit the efficient digital signal processing and reconfiguration capabilities in deep sub-micron CMOS technologies. Recently, ADC architectures have been demonstrated in these technologies able to support a wide variety of wireless standards with state-of-the-art power consumption in each mode/standard. Furthermore, the speed advantages of advanced CMOS technologies also allows to revisit the classical partitioning of the wireless receiver functionality by shifting more of the analog signal conditioning (channelization and downconversion,) to the digital domain and as such pave the way towards a true software radio.

These different aspects will be illustrated in the following sections with 3 recent ADC achievements each improving the state-of-the-art for energy efficiency in their architecture. This is illustrated in Figure 1. Section 2 will cover a novel charge-domain signal method that enables extremely efficient Nyquist-rate SAR ADCs. In section 3, advances in reconfigurable ΣΔ ADCs are reported that combine optimized low-power architecture and circuits with multi-mode operation. Section 4 discusses the implementation of a first ADC-at-the-antenna system that uses an RF bandpass ΣΔ, a technique that could in time evolve into a true software radio for cognitive systems. Finally, section 5 concludes this paper.

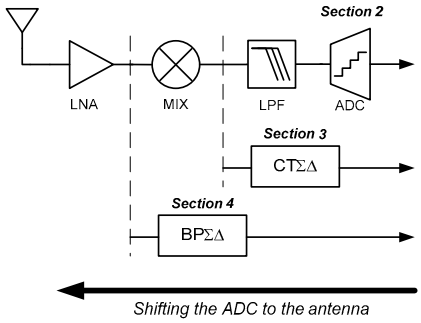

Figure 1: SDR receiver architectures with different ADC options

2. CHARGE-SHARING SAR ADC

ADCs with 8 to 10 bits accuracy at several 10s of MS/s have for a long time been the territory of pipeline architectures. But in scaled CMOS these specs become well in range of SAR ADCs. Most SAR ADCs use an operating principle similar to the charge redistribution architecture [1]. This requires fast settling opamps in both the input and the reference voltages, able to settle their output voltage in a very short time while driving large capacitive loads. Also the high-speed clock for the controller that has to run at 10x the sampling speed must be available.

A new SAR architecture is proposed that uses passive charge sharing (instead of active charge redistribution) to both sample the input signal and to perform the binary scaled feedback during the successive approximation [2]. The basic architecture depicted in Figure 2 works

completely in the charge-domain. The input is sampled on a capacitor and during the SAR algorithm charge is added or subtracted until the result converges to zero. No active circuits are used to add/subtract these charges. Instead, simple passive switches do this. The signal is not represented anymore by the voltage at the comparator input, but instead by the total charge accumulated on the set of capacitors.

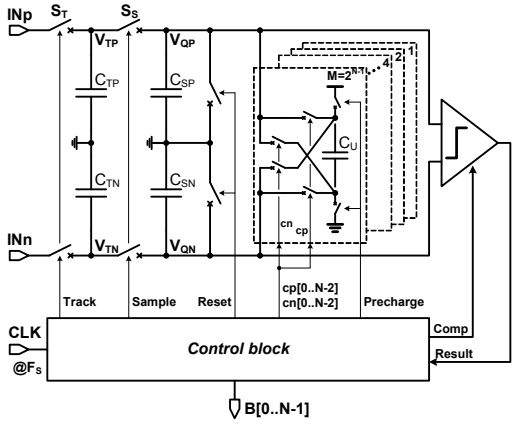

Figure 2: Basic charge-sharing SAR architecture

The binary scaled array of unit capacitors is pre-charged to the reference, and it is these charges that will be used to provide the feedback DAC function in the SAR ADC. Since this pre-charging happens *before* the actual A-to-D conversion, and is hence *signal-independent*, there are no tough constraints imposed on this "reference".

The fundamental power limits of the original SAR architecture have been removed by doing all the charge-redistribution passively. This way the only remaining active element in the ADC is the comparator itself and the digital controller. Another advantage is the completely digital implementation, requiring only MOS switches and MOM capacitors, which makes it portable to new CMOS technologies.

The comparator schematic is based on [3] and includes a programmable capacitor array to calibrate its offset voltage. It does not consume any power when inactive, and thus enables for the whole ADC the feature that its power consumption scales linearly with the sampling frequency. An extra 'valid' output is added that indicates when the comparison is done, which is used by the asynchronous SAR controller as a trigger to continue the conversion process by closing one of the sharing switches.

A first 9-bit 50MS/s prototype based on this concept was realized in a 90nm 1P9M digital CMOS [2]. The measured power consumption was as low as 700µA from a 1V supply at the maximum sampling frequency. Underestimated comparator noise limits the SNR to 49dB (7.8 ENOB) but despite that the resulting FoM as defined by

$$FOM = \frac{P}{2^{ENOB} \cdot F_S} \quad (1)$$

is with 65fJ/conversion-step a factor 2.5X lower than earlier designs, clearly showing the power advantage of the charge-sharing architecture.

To solve the issue of comparator noise, a noise-robust design approach that leverages redundancy in the search algorithm is further developed [4]. Two comparators are used, one which is sized large enough to have sufficiently low noise (but also an increased power consumption) and one that uses less power but is more likely to make an erroneous decision due to noise.

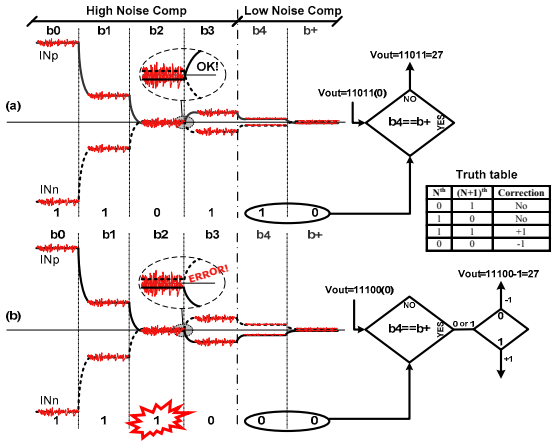

Figure 3: Comparator noise correction algorithm in case of no error (a) and error (b)

The strategy behind the correction technique relies on the fact that if the input comparator rms noise is properly sized, at most 2 out of N comparisons during the SAR operation are likely to be critical because of thermal noise, i.e., the one when the signal is right below the threshold and the one when it is right above. One of those critical decisions will certainly be the last one: an error in this decision can be avoided by using the comparator in its low noise state. The other one can be any of the previous (N-1) comparisons, and avoiding it with a low-noise comparator is not power efficient.

As shown in Figure 3 for a 5-bit example, the SAR algorithm uses the comparator in its low-power state during the first (N-1) iterations, thus allowing errors in these cycles. The ADC then switches into its low-noise mode to avoid errors for the N^{th} comparison, and an extra $(N+1)^{th}$ iteration is added to correct for the error possibly made in the first phase. If the last 2 comparisons give different results, no error was made and no action has to be taken. In case the last 2 bits are equal, then a digital addition or subtraction needs to be performed on the final N-bit result. This correction is effective not only for thermal noise, but also for other noise sources, including static non-linearities, as far as they are not bigger than 1 LSB.

This prototype also used a time-interleaved sample&hold structure at the input with a bootstrapped switch [5] to improve the input linearity. A die photo is shown in Figure 4, and the measured ENOB versus frequency and near-nyquist FFT are visible in Figure 5. An ENOB of 8.6bit is reached, while the power consumption is only increased to 820µW at 40MS/s. Without redundancy, the power consumption would have to be increased by a factor 4 for a 1-bit increase in ENOB due to noise, which clearly shows the effectiveness of the noise-robust architecture. The resulting FoM is 54fJ/conversion-step.

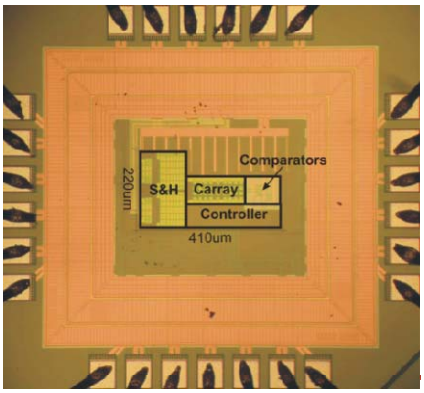

Figure 4: Noise-robust charge-sharing SAR ADC die micrograph

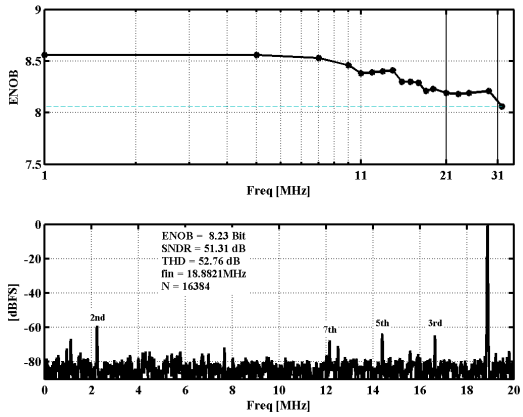

Figure 5: ENOB versus input frequency and near-nyquist FFT at 40MS/s

The demonstrated breakthroughs in ADC power efficiency enable to make new architecture trade-offs for multi-mode radio systems. As the ADC power consumption scales linearly with the sampling frequency, it can without any effort be used in every system and hence realizes a perfect building block for an SDR. Since the ADC power consumption is now in the order of 1mW, it is not visible anymore in the total radio power budget. Higher ADC sampling frequencies can be used, allowing to reduce the analog baseband filtering order, thus reaching a low-power SDR implementation.

3. MULTI-MODE CONTINUOUS-TIME ΣΔ ADC

An ADC architecture that allows to further reduce or sometimes even completely eliminate the analog baseband filter is the continuous-time sigma-delta (CTΣΔ). This is however in most cases limited to low-bandwidth systems, and multi-mode realizations offer only limited performance, which makes them not suited for an SDR system.

To solve this challenge, a fully flexible CTΣΔ has been developed [6][7], programmable over all signal bandwidths from 500kHz (Bluetooth) up to 10MHz (WLAN) illustrating multimode operation. A high resolution (Dynamic Range (DR) from 83dB to 67dB) with low power consumption is obtained thanks to a large flexibility in the core circuitry (OTA, DAC and quantizer) of the modulator. By implementing every building block as a matrix of switchable unit cells, the lowest power consumption for a specific resolution and bandwidth is reached. This technique also allows to scale the power consumption in a certain mode to the required accuracy.

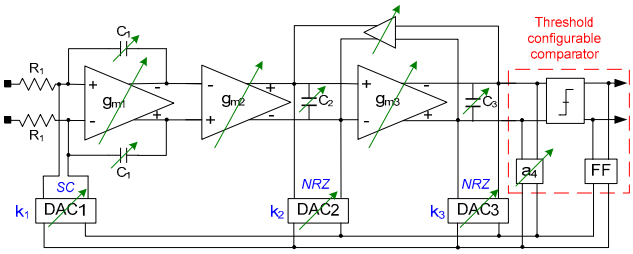

Figure 6: Architecture of the 3rd order flexible CTΣΔ.

Figure 6 shows the architecture of the CTΣΔ. It consists of a 3rd order feedback loop filter with tunable notch and scale factors k_i in the feedback path. From a linearity/speed trade-off, the loop filter is a cascade of one OTA-RC and two gm-C stages. The single bit quantizer uses a threshold configurable comparator whose threshold adaptation emulates the direct feedback path a_4 needed for loop delay compensation without additional hardware or power. The first feedback DAC uses a switched capacitor implementation for its reduced sensitivity to jitter and its easy integration with an OTA-RC integrator using the virtual ground. The 2nd and 3rd DAC are current switched NRZ DACs where the current is fed back into a low impedance node (source cascode) of the gm-C integrators.

Traditionally, the sampling frequency (80MHz-640MHz) and the filter coefficients are modified at system level for multimode operation. In this design, also the feedback coefficients (k_i in Figure 6) are scalable up to a factor three to control the internal signal level allowing the best noise-linearity trade-off. To further enhance the flexibility, extensive reconfigurability is introduced at circuit level. This is achieved by bringing this flexibility into the core of all building blocks in combination with passive component arrays and adjustable biasing. Therefore,

every building block is split into a matrix of switchable unit cells. Careful design of these unit cells ensures that the performance is not deteriorated by the switches. Hence, optimal performance and high flexibility is achieved at low power consumption.

A prototype chip has been fabricated in 1.2V digital 90nm CMOS (Figure 7) with an active area is less than 0.4mm^2. In Figure 8, the SNDR is plotted vs. the input amplitude for different modes. For UMTS, this is done in a high resolution – moderate power mode (78dB DR for 6.44mW) and for a moderate resolution – low power mode (73dB DR for 4.34mW). The former uses a larger scale factor k to reduce the signal swing at the input of the g_m-C integrator. Clearly, power can be saved when less resolution is required. A DR of 67/72/78/83dB is achieved in maximum performance mode for WLAN, DVB, UMTS and BT for a power consumption of 6.8/5.5/6.4/5.0mW respectively.

The resulting FoM ranges from 0.8 down to 0.24pJ, which an excellent number beating even state-of-the art single-mode designs. This shows that a reconfigurable CTΣΔ ADC, which requires less or even no analog baseband filtering, is also a viable path for SDR receivers.

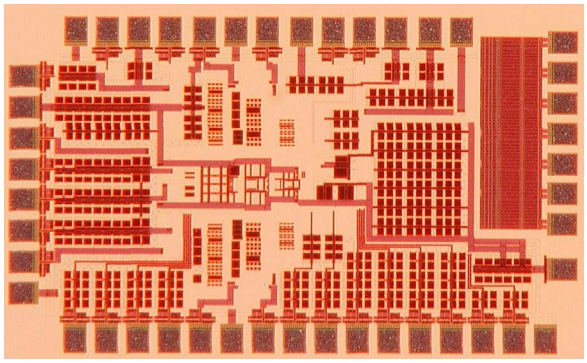

Figure 7: Multi-mode power-performance scalable CT ΣΔ die photo

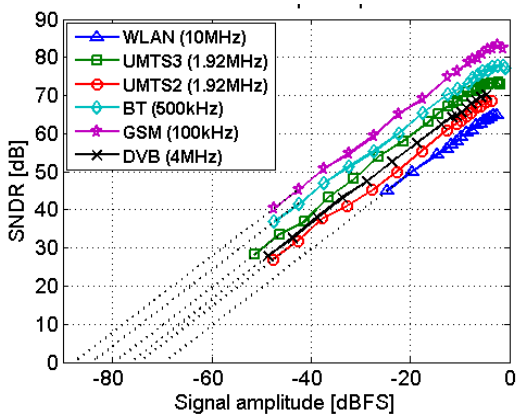

Figure 8: SNDR versus input amplitude in several modes

4. RF BANDPASS ADC

Moving the boundary of the ADC even further towards the antenna is however a gigantic task. Flash ADCs can operate today at GHz speeds but their resolution remains limited to a few (~5-6) bits [3]. By placing the flash converter in a ΣΔ loop, the oversampling ratio and the order of the loop filter can provide a higher resolution in a limited bandwidth. Therefore, a bandpass (BPΣΔ) ADC centered at the desired frequency band appears as an ideal candidate for an RF ADC architecture. Moreover, the bandwidth of the converter can be made large enough to capture a complete RF band at once and allow multiple channels to be simultaneously processed. In this section, we propose such a design that targets SDR application in the 2.5GHz ISM band [8]. If it would be possible to capture the full ISM band in one ADC, simultaneous reception of several RF streams would be possible with only one analog front-end. The circuit is realized in a standard 90nm CMOS technology and consumes only 40mW. Several techniques are used to achieve this low power consumption.

First we exploit the mirrored-image technique which allows a reduction of the clock frequency. Traditionally, BPΣΔ ADCs are centered on integer fractions of the sampling clock below the input signal Nyquist frequency (e.g. Fs/4). But because of the discrete-time nature of the ΣΔ loop, the noise shaping actually occurs at all aliases as well. So the loop filter center frequency can be positioned on for example the first alias above the Nyquist frequency (e.g. 3Fs/4). This large clock frequency reduction heavily lowers the required power consumption.

For the loop filter, a 6th order bandpass structure as proposed in [7] based on a cascade of Gm-LC resonators is chosen. The filter consists of a high quality high gain path (Gm-LC1, Gm-LC2), ensuring sufficient noise shaping in the useful band, stabilized by a feedforward path with a lower Q (1+Gm-LCx). A negative Gm (-R) is incorporated in each resonator to compensate for the low Q of on-chip inductors.

The architecture of the complete ADC is shown in Figure 9. The feedback signal is injected as a current in the first resonator tank such that the first Gm stage lies outside the ΣΔ loop. A direct feedback path F adds the quantized signal directly to the quantizer input compensating for loop delay. The single-bit quantizer is made of two interleaved comparators clocked at half the speed. This reduces the power consumption in the comparator. Both outputs are then multiplexed to produce the output bit stream.

The ΣΔ has been processed on a standard 1P9M 90nm CMOS technology and the chip microphotograph is given in Figure 10. It operates at 2.4GHz in 4Fs/5 mode, so with a sampling frequency of 3GS/s.

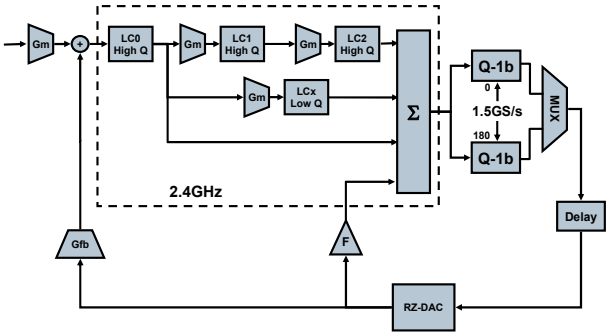

Figure 9: RF BP ΣΔ architecture

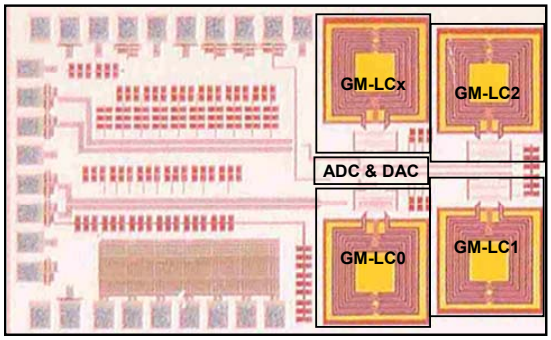

Figure 10: RF BP ΣΔ chip micrograph

Figure 11 shows the spectrum plot of a 2.41GHz RF signal applied to the input of the ΣΔ clocking at 3GS/s. Note that the spectrum is plotted around the image frequency at 600MHz (3GHz–2.4GHz). In a 60MHz bandwidth, 40dB SNDR (6.3 ENOB) is reached, which is of course not sufficient for an SDR, but shows the capabilities of modern CMOS technology for these applications. Further work will try to improve this performance by using e.g. higher sampling frequencies, other loop filters, multi-bit quantizers, etc.

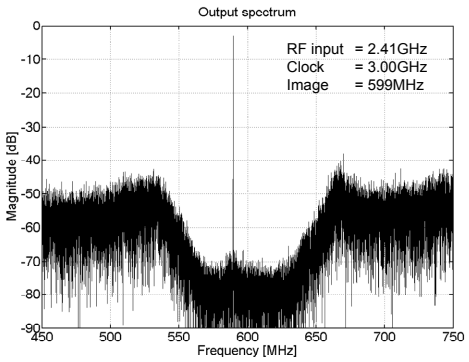

Figure 11: Spectrum of the output digital bit stream around the image (Fs/5)

5. CONCLUSIONS

Several innovations in the area of power-efficient analog-to-digital converters (ADC) for software-defined radio (SDR) front-ends have been presented, each targeted to a different radio architecture shifting the ADC closer towards the antenna.

A Nyquist-rate SAR ADC architecture is proposed with record FoM, while multi-mode performance of CTΣΔ ADCs has been shown without any power disadvantage. Finally, a first step towards an RF-sampled SDR has been demonstrated with an RF bandpass ΣΔ ADC for the ISM band.

REFERENCES

[1] J. McCreary and P. Gray, "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques - Part I", *IEEE Journal of Solid-State Circuits*, vol. 10, no. 6, pp. 371-379, Dec. 1975.

[2] J. Craninckx and G. Van der Plas, "A 65fJ/Conversion-Step 0-to-50Ms/s 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS", *ISSCC Dig. Tech. Papers*, pp. 246-247, Feb. 2007.

[3] G. Van der Plas, S. Decoutere and S. Donnay, "A 0.16pF/conversion-step 2.5mW 1.25GS/s 4b ADC in a 90nm digital CMOS process", *ISSCC Dig. of Technical Papers*, pp. 566-567, Feb. 2006

[4] V. Giannini et al. , "An 820µW 9b 40MS/s noise-tolerant dynamic SAR ADC in 90nm digital CMOS", *ISSCC Dig. Tech. Papers*, pp. 238-239, Feb. 2008.

[5] A.M. Abo and P.R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter", *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599-606, May 1999.

[6] P. Crombez, G. Van der Plas, M. Steyaert, and J. Craninckx, "A 500kHz-10MHz Multimode Power-Performance Scalable 83-to-67dB DR CT Sigma-Delta in 90 nm Digital CMOS with Flexible Analog Core Circuitry", *IEEE Symp. VLSI Circuits, Dig. Tech. Papers*, June 2009

[7] P. Crombez, G. Van der Plas, M. Steyaert, and J. Craninckx, "A Single Bit 6.8mW 10MHz Power-Optimized Continuous-Time Delta Sigma with 67dB DR in 90nm CMOS", *European Solid-State Circuits Conference (ESSCIRC)*, Sept 2009

[8] J. Ryckaert et al. , "A 2.4GHz 40mW 40dB SNDR/62dB SFDR 60MHz bandwidth mirrored-image RF bandpass Sigma- Delta ADC in 90nm CMOS", *A-SSCC. Dig. Tech. Papers*, pp. 361-364, November 2008

[9] C. Lalandais-Perrault et al., "A parallel structure of a continuous-time filter for band-pass sigma-delta A/D converters", *IEEE Int. Conf. Electronics Circuits and Systems*, vol. 3, pp. 954-957, Dec. 2003.