Area-Efficient HW-Implementation of the FFT for OFDM Applications

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Overview

1. OFDM-Systems and FFT/IFFT Requirements
2. Pipeline FFT/IFFT Algorithms and their Number of Computing Elements
   1. Cooley Tukey FFT
   2. Bruun FFT
3. Error Analysis for CT-FFT and Bruun FFT
4. Chip Area Estimations for ASIC- and FPGA-Design
5. Conclusion

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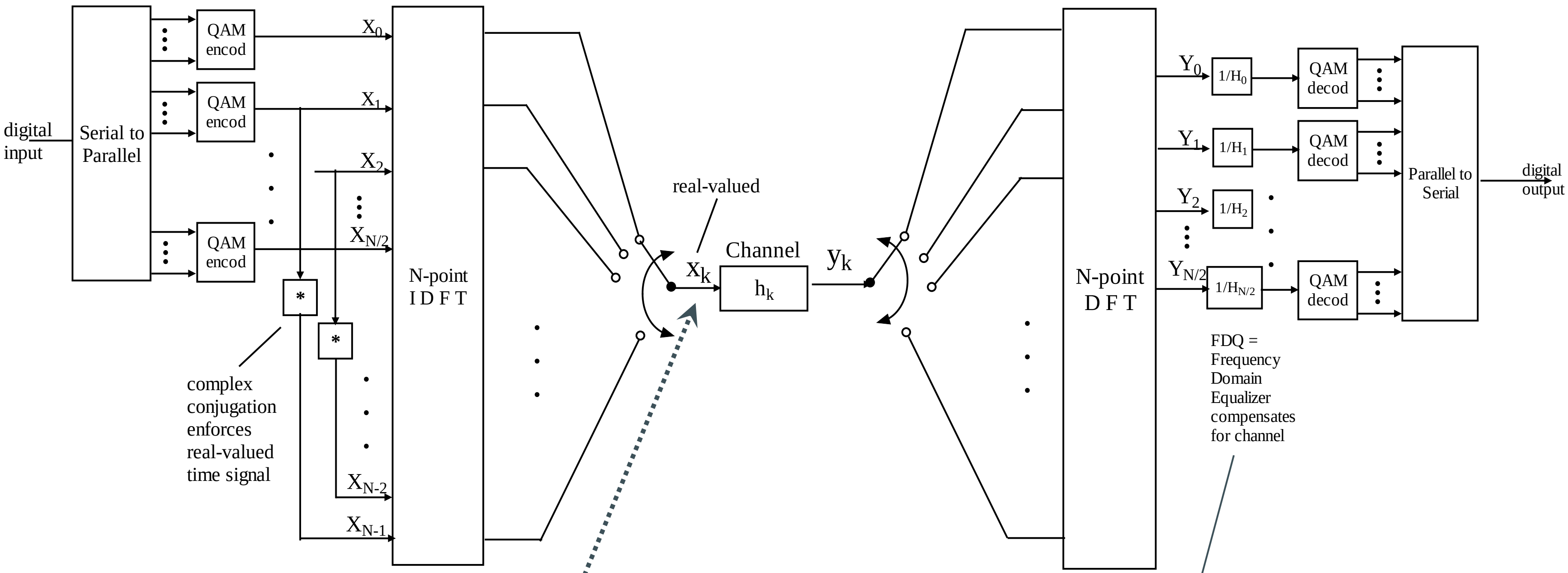
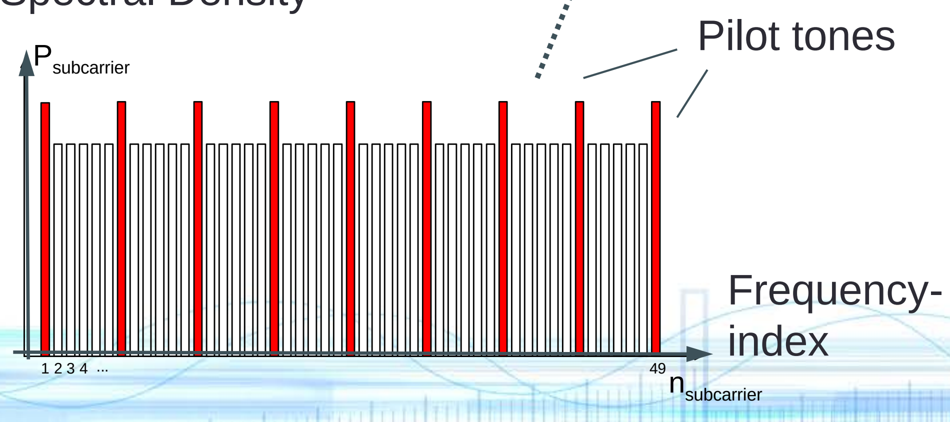
OFDM: working principle



Power Spectral Density

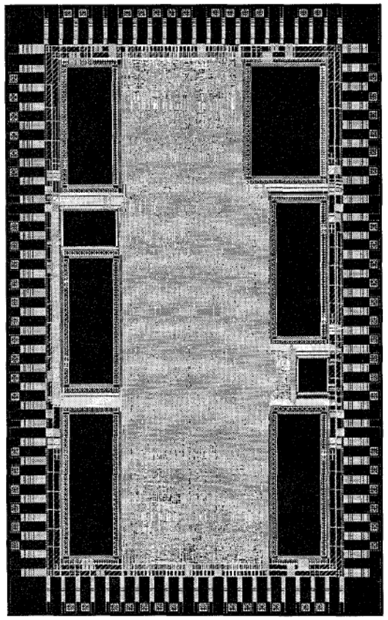


multiplication in frequency domain corresponds to Cyclic convolution in the time domain → cyclic prefix needed

(I)DFT = (Inverse) Discrete Fourier Transform

OFDM-based standards

Standard [1), 2), 4)]	No. of Carriers N	wordlength
DAB	192, 384, 768, 1536	~ 10 – 20 bits (depends on N)
DRM	181, 203	
DVB-T, DVB-H	2048, 4096, 8192	
WLAN, HiperLAN	52	
WiMAX	256, 2048	



N=1024 FFT-Pipeline-Processor [3)]

DAB = Digital Audio Broadcast
DRB = Digital Radio Mondiale
DVB = Digital Video Broadcast
WLAN = Wireless LAN
HiperLAN = High Performance Radio LAN
WiMAX = Worldwide Interoperability for Microwave Access

[1)] Rauwerda, G. K., Heysters, P. M., Smit, and Gerard J.M., An OFDM receiver implemented on the coarse grain reconfigurable Montium processor, 9th Intl. OFDM-Workshop 2004, Dresden, pp. 1 - 5 .

[2)] Posega, R., Advanced OFDM Systems for Terrestrial Multimedia Links, PhD Diss., EPFL, Lausanne, 2005 .

[3)] Shousheng He and Mats Torkelson., Designing Pipeline FFT Processor for OFDM (de)Modulation, ISSSE ’98, 1998.

[4)] Yu-Ju Cho et alii., Efficient Fast Fourier Transform Processor Design for DVB-H System, VLSI 2007.

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Cooley-Tukey FFT (CT-FFT)

DFT: $$F_{N,m} = \sum_{n=0}^{N-1} f_n \cdot W_N^{mn}; \quad m = 0,1,\dots,N-1; \quad W_N = e^{-j\frac{2\pi}{N}}$$

IDFT: $$f_n = \frac{1}{N}\sum_{m=0}^{N-1} F_{N,m} \cdot W_N^{-mn}; \quad n = 0,1,\dots,N-1$$

Divide and Conquer Approach of Cooley and Tukey (decimation in time):

$$F_{N,m} = \sum_{n=0}^{N-1} f_n \cdot W_N^{mn}$$

even time samples

odd time samples

$$= \sum_{n=0}^{\frac{N}{2}-1} f_{2n} \cdot W_N^{m2n} + \sum_{n=0}^{\frac{N}{2}-1} f_{2n+1} \cdot W_N^{m(2n+1)}$$

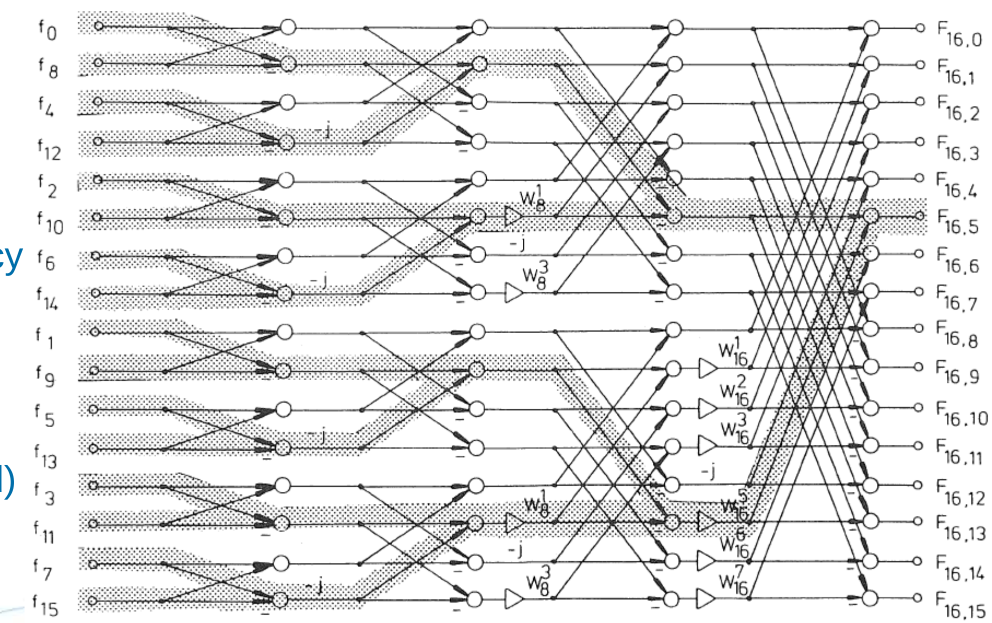
$$= \sum_{n=0}^{\frac{N}{2}-1} f_{2n} \cdot W_N^{m2n} + W_N^m \sum_{n=0}^{\frac{N}{2}-1} f_{2n+1} \cdot W_N^{m2n}$$

first half of frequency samples

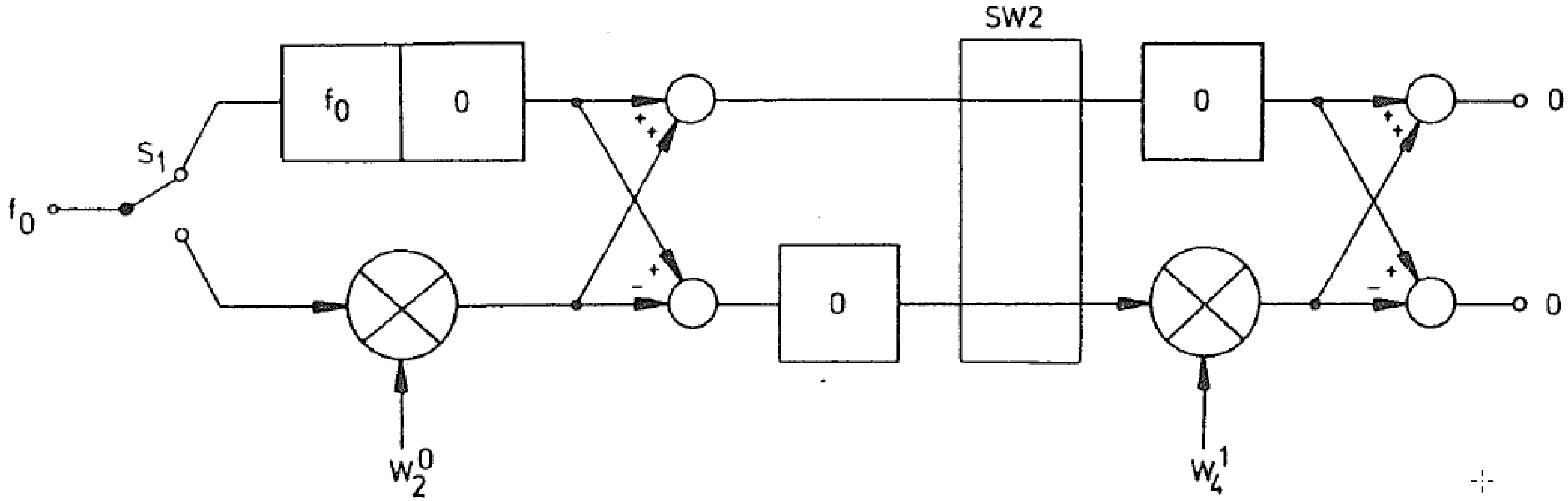
$$= \sum_{n=0}^{\frac{N}{2}-1} \left(f_{2n} + W_N^m \cdot f_{2n+1}\right) \cdot W_N^{m2n}; \quad m = 0,1,\dots,\frac{N}{2}-1$$

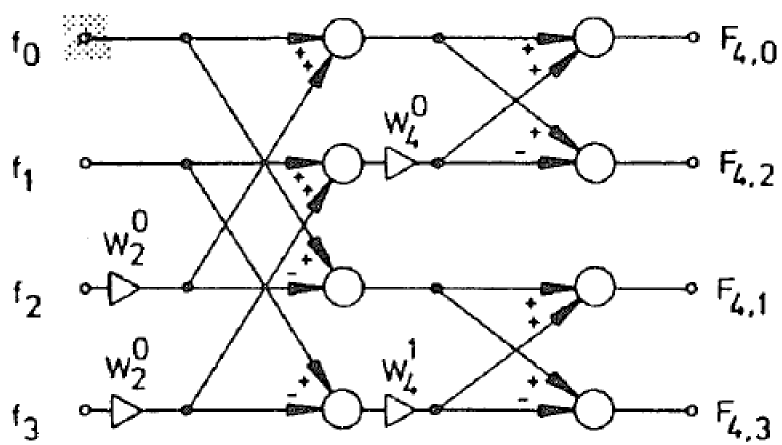
twiddle factor (complex-valued)

$$F_{N,m+\frac{N}{2}} = \dots = \sum_{n=0}^{\frac{N}{2}-1} \left(f_{2n} - W_N^m \cdot f_{2n+1}\right) \cdot W_N^{m2n}$$



Cooley-Tukey FFT Pipeline Architecture for $N = 2^2$





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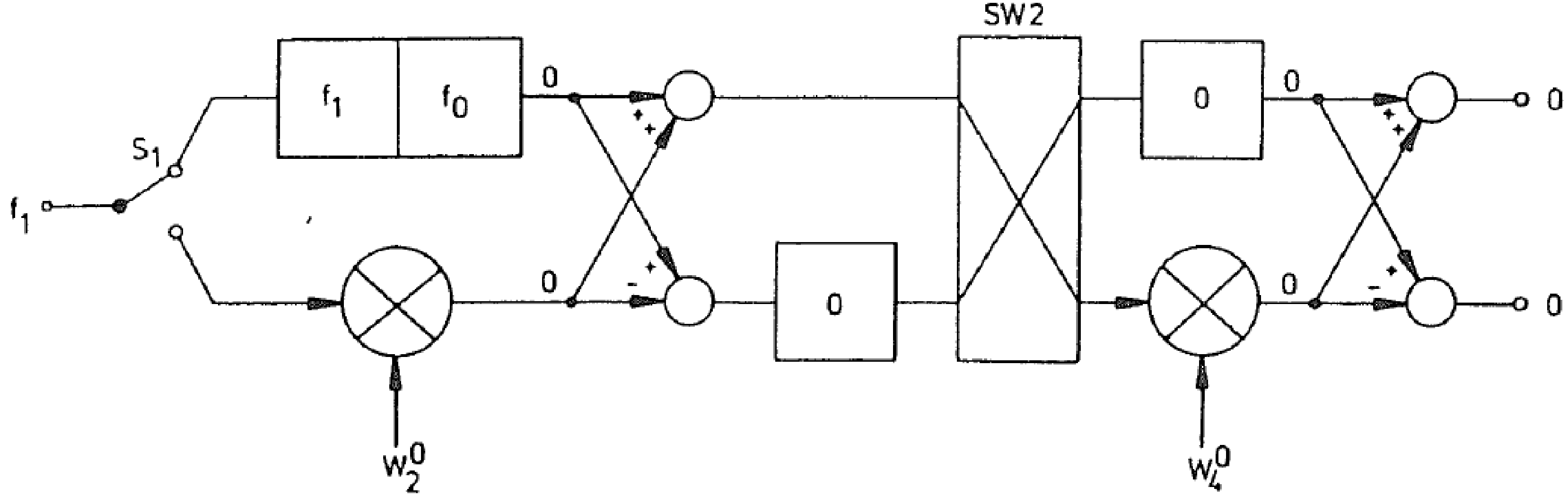

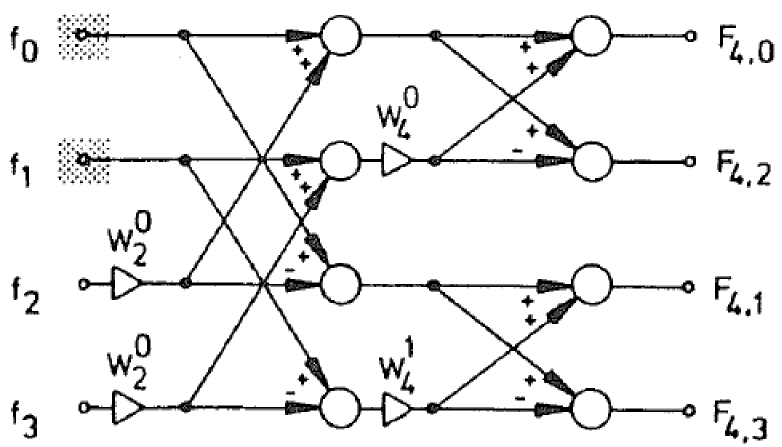

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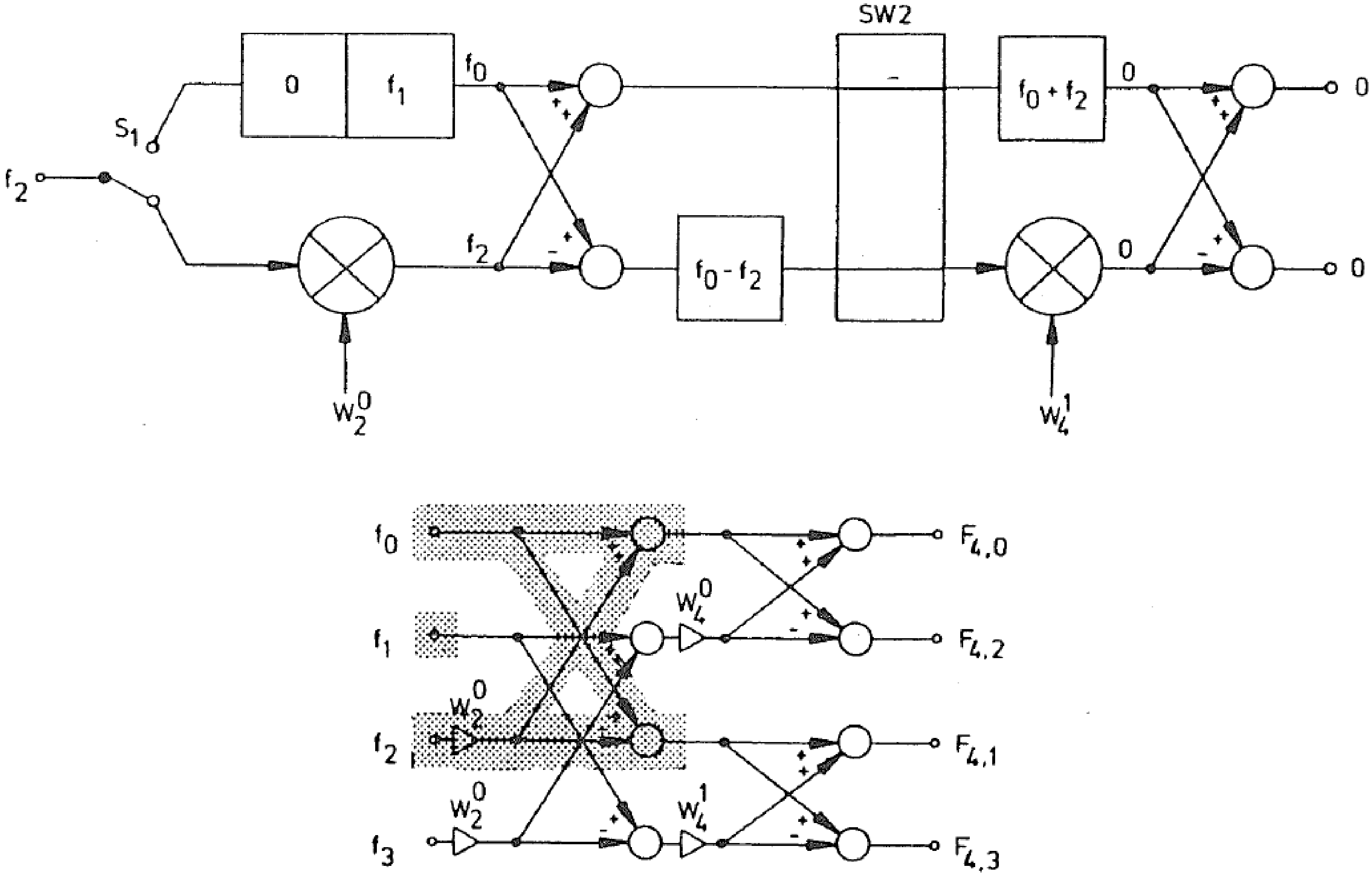

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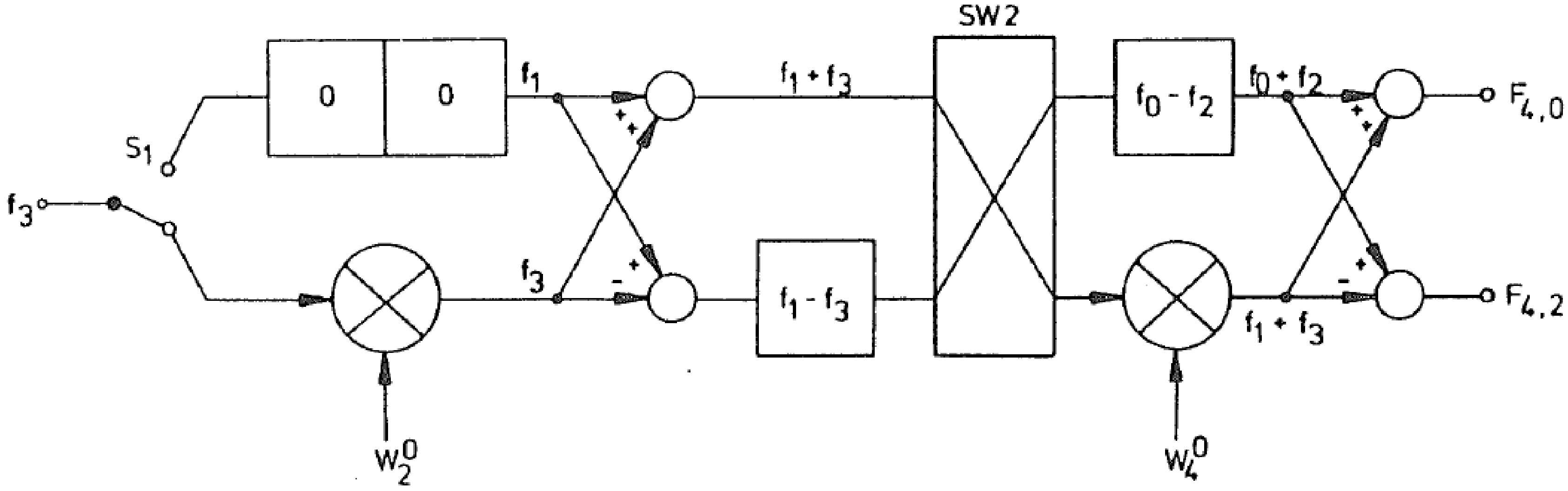

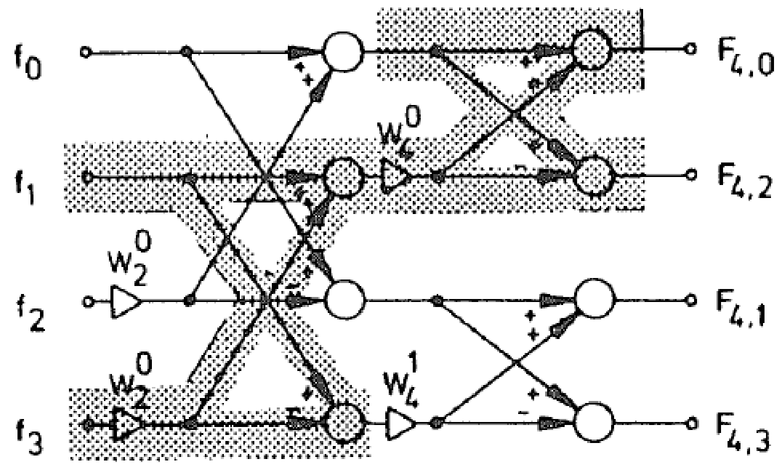

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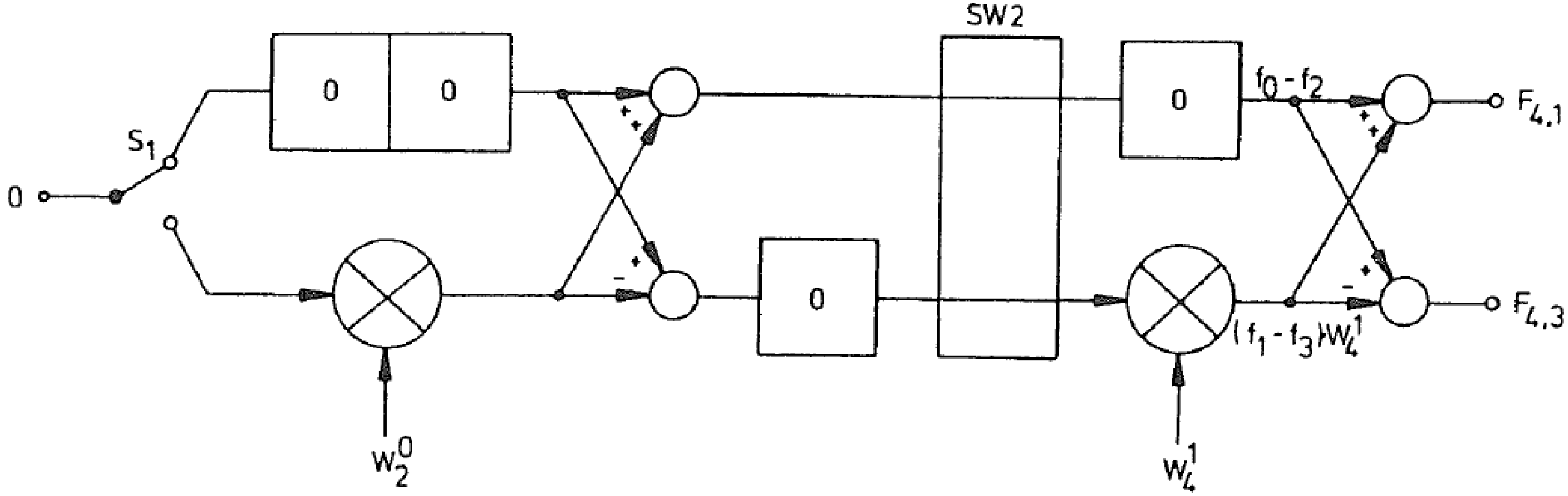
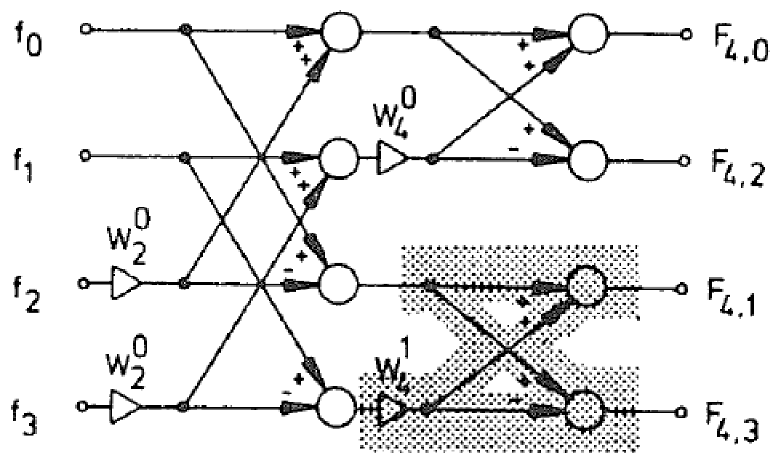
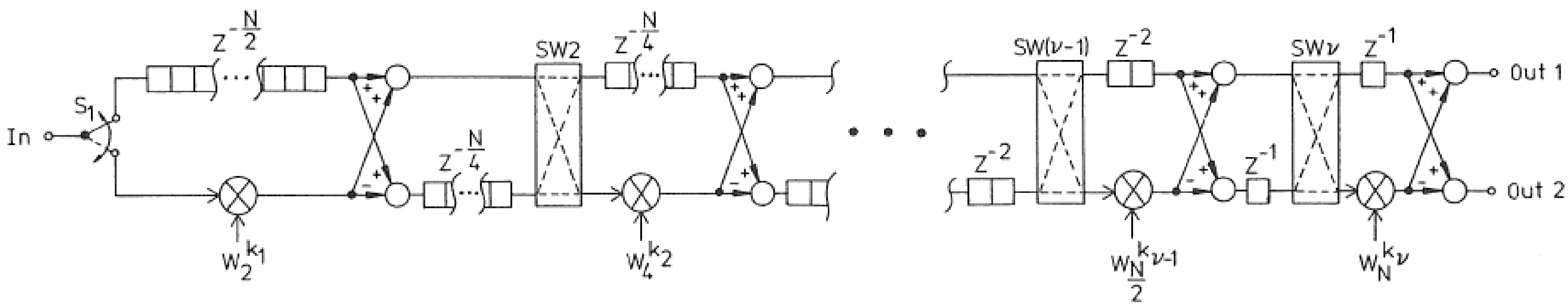




Cooley-Tukey FFT-Pipeline for N = 2^ν, ν integer



No. of real-valued multipliers $$n_{mult} = 4 \cdot \sum_{k=0}^{\nu-3} k = 4 \cdot (\nu - 2)$$

No. of real-valued adders $$n_{add} = 6 \cdot (\nu - 1) + 2$$

No. of real-valued delay-elements $$n_{delay} = \frac{N}{2} + 2 \cdot \frac{N}{4} + 2 \cdot \sum_{k=1}^{\nu-3} 2^k = \ldots = 2^\nu + 2^{\nu-1} - 4$$

No. of real-valued twiddle-factors $$n_{coeff} = \sum_{k=0}^{\nu-1} (2^k - 2) + 1 = \ldots = 2^\nu - 2 \cdot \nu$$

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Bruun FFT → FIR-Filtering Approach of Bruun [1)]

Let $$f(z) = f_0 + f_1 \cdot z^{-1} + f_2 \cdot z^{-2} \ldots + f_{N-1} \cdot z^{-(N-1)} = \sum_{n=0}^{N-1} f_n \cdot z^{-n}$$

and $$B_m(z) = W_N^{-m} \sum_{n=0}^{N-1} b_n \cdot z^{-n}; \quad \textit{where} \quad b_n = \left(W_N^{-m}\right)^n$$

Then $$A_m(z) = f(z) \cdot B_m(z) = \sum_{n=0}^{N-1} a_{m,n} \cdot z^{-n} \quad \textit{and} \quad F_{N,m} = a_{m,N-1}$$

Use $$B_m(z) = \ldots = \frac{z^{-N} - 1}{z^{-1} - W_N^{-m}} \overset{x=z^{-1}}{=} \frac{x^N - 1}{x - W_N^{-m}}$$ **and the following 3 identities [2)] to decompose the numerator of $B_m(z)$:**

$$\left(x^Q - 1\right) = \left(x^{\frac{Q}{2}} - 1\right) \cdot \left(x^{\frac{Q}{2}} + 1\right) \quad \textit{for} \quad Q = 2^\rho > 1; \rho \quad \text{integer}$$

$$\left(x^M - 2 \cdot x^{\frac{M}{2}} \cdot \cos\frac{\pi}{r}k + 1\right) = \left(x^{\frac{M}{2}} - 2 \cdot x^{\frac{M}{4}} \cdot \cos\frac{\pi}{2r}k + 1\right) \cdot \left(x^{\frac{M}{2}} - 2 \cdot x^{\frac{M}{4}} \cdot \cos\frac{\pi}{2r}(2r-k) + 1\right) \quad \textit{for} \quad M = 2^\mu > 2; \mu \quad \text{integer}$$

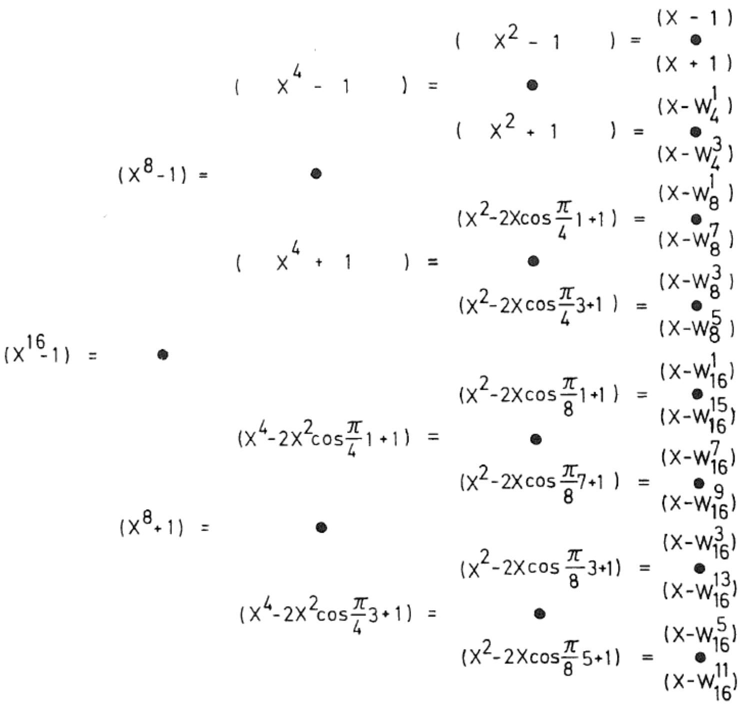
$$\left(x^M - 2 \cdot x^{\frac{M}{2}} \cdot \cos\frac{\pi}{r}k + 1\right) = \left(x^{\frac{M}{2}} - W_{2r}^{k}\right) \cdot \left(x^{\frac{M}{2}} - W_{2r}^{-k}\right) \quad \textit{for} \quad M = 2$$

1) Bruun, G., Z-Transform DFT-Filters and FFTs, IEEE Trans. ASSP 26, Feb. 1978, pp. 56 - 63 .

2) Storn, R., Storn, R., On the Bruun Algorithm and its Inverse, Frequenz 46 (1992) 3-4, pp. 110 – 116 .

Bruun FFT

After some lengthy rearrangements we get (for the example N=16)



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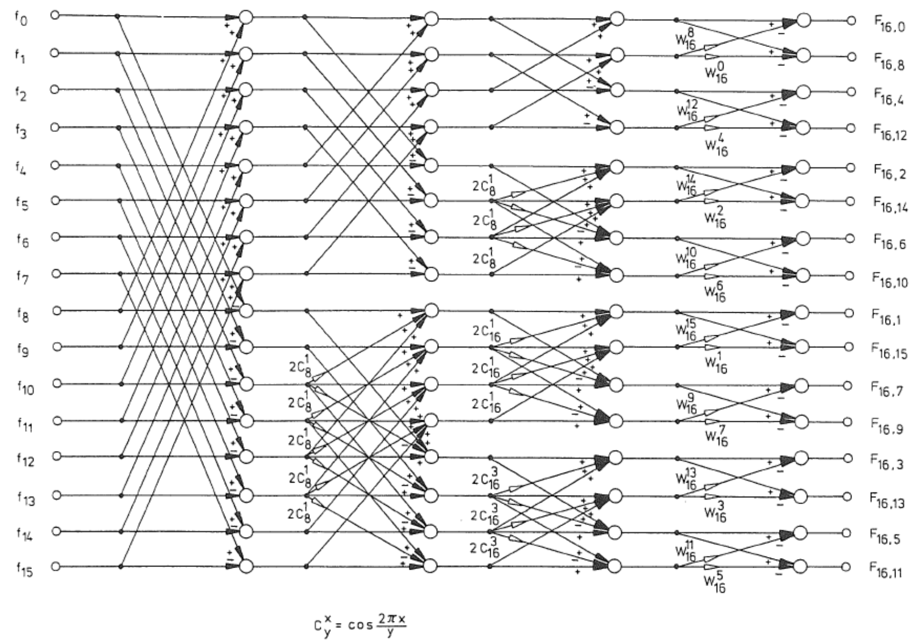
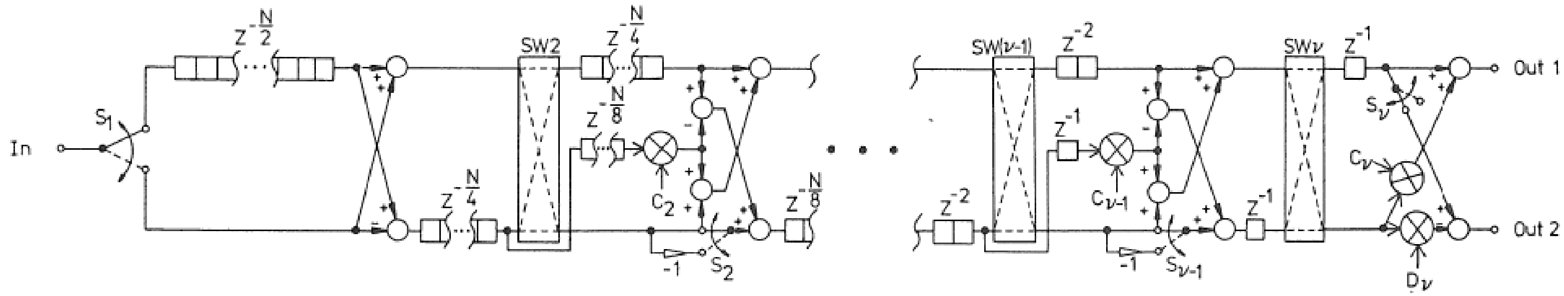


Decomposition tree for x^{16} - 1

Bruun-FFT for N=16

Important! : Twiddle factors are all real-valued except for the last stage

Bruun FFT-Pipeline for N = 2^ν, ν integer [1)]



No. of real-valued multipliers $n_{mult} = \nu$

No. of real-valued adders $n_{add} = 4\cdot(\nu-2)+4 = 4\cdot(\nu-1)$

No. of real-valued delay-elements $n_{delay} = \sum_{k=1}^{\nu-1} 2^k + \sum_{k=1}^{\nu-3} 2^k + \sum_{k=1}^{\nu-2} 2^k \ldots = 2^\nu + 2^{\nu-1} + 2^{\nu-2} - 6$

No. of real-valued twiddle-factors $n_{coeff} = \sum_{k=0}^{\nu-1}\left(2^k-1\right) + 2^\nu - 2 = \ldots = 2^{\nu+1} - \nu - 3$

[1)] Storn, R., A Novel Radix-2 Pipeline Architecture for the Computation of the DFT, in IEEE Proc. ISCAS 1988, pp. 1899-1902.

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Noise to Signal Ratio for CT-FFT and Bruun-FFT

Safe scaling assumed, i.e. overflow is prevented by right shifts

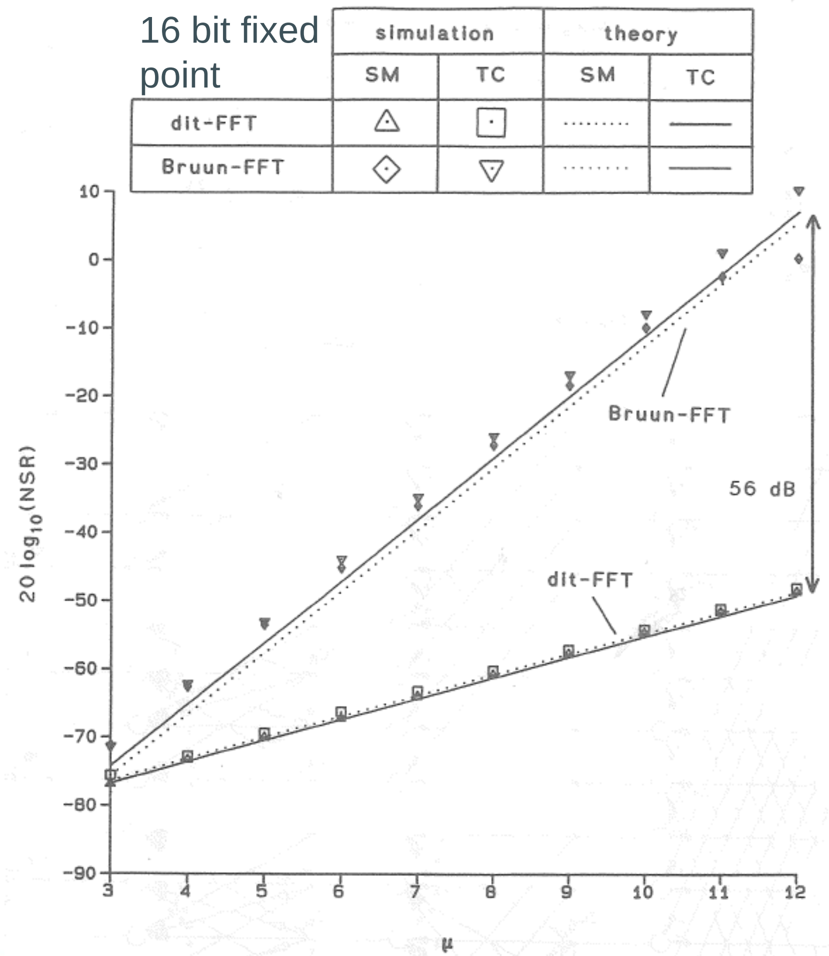
Noise-to-signal Ratio:

$$NSR = \sqrt{\frac{N^{-1} \cdot \sum_{m=0}^{N-1} E[e_m]^2}{E\left[\left|F'_{N,m}\right|^2\right]}}$$

Additional bits For Bruun-FFT:

$$\Delta b = \left\lceil 20 \cdot \log_{10}\left(\frac{NSR_{Bruun}}{NSR_{CT}}\right) / 6 \right\rceil$$

Exponent ν	Transform Length N=2^ν	Δb
3	8	0
4	16	1
5	32	2
6	64	3
7	128	4
8	256	5
9	512	6
10	1024	7
11	2048	8
12	4096	9



[1)] Storn, R., Some Results in Fixed Point Error Analysis of the Bruun-FFT Algorithm, IEEE Trans. Signal Proc., Vol. 41, No. 7, July 1993, pp. 2371 – 2375 .

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Full custom ASIC implementation (65nm process)

1-bit full adder: $A_{fa} = 429.53 \mu m^2$

1-bit full shifter: $A_{sh} = 51.00 \mu m^2$

AND-gate: $A_g = 107.13 \mu m^2$

Area estimation for Booth multiplier:

$k_{Booth} = 1.3$

$$A_{mult} = k_{Booth} \cdot \left[(b-1)^2 \cdot \left(A_{fa} + A_g\right) + (2b-1) \cdot A_g\right] + k_{Booth} \cdot \left[(b-1) \cdot A_{fa}\right]$$

RAM and ROM:

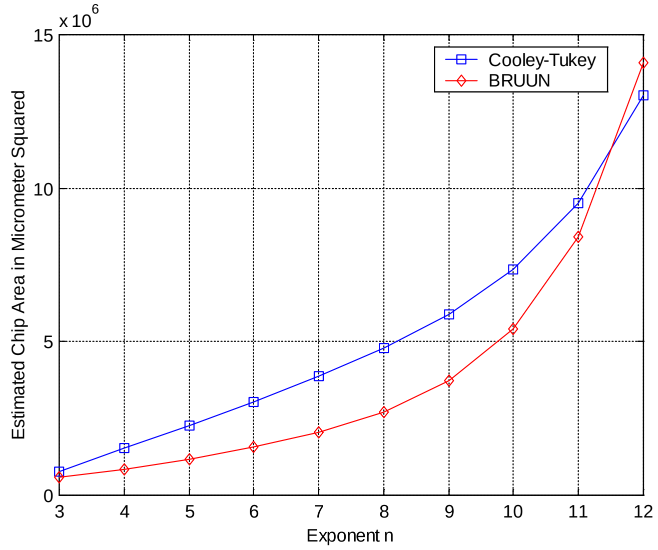
$$A_{RAM} = k_{1,RAM} \cdot 2^{2R} + k_{2,RAM} \cdot R \cdot 2^R$$

$$A_{ROM} = k_{1,ROM} \cdot 2^{2R} + k_{2,ROM} \cdot R \cdot 2^R$$

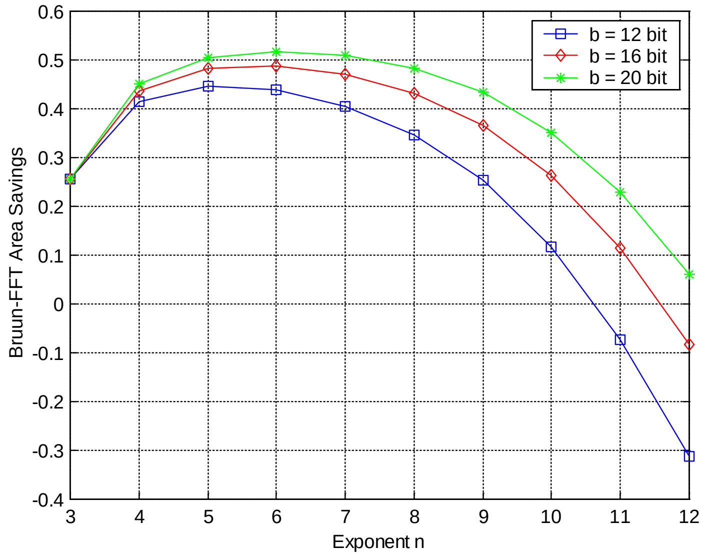
constants	in μm^2
$k_{1,RAM}$	29.97 μm^2
$k_{2,RAM}$	398.44 μm^2
$k_{1,ROM}$	2.75 μm^2
$k_{2,ROM}$	287.11 μm^2

[1] Storn, R., Algorithmen und Architekturen der diskreten Fouriertransformation zur schnellen Faltung reeller Signale, PhD diss., Univ. Stuttgart, Germany, 1990 .

Area estimation for CT-FFT and Bruun FFT (ASIC)



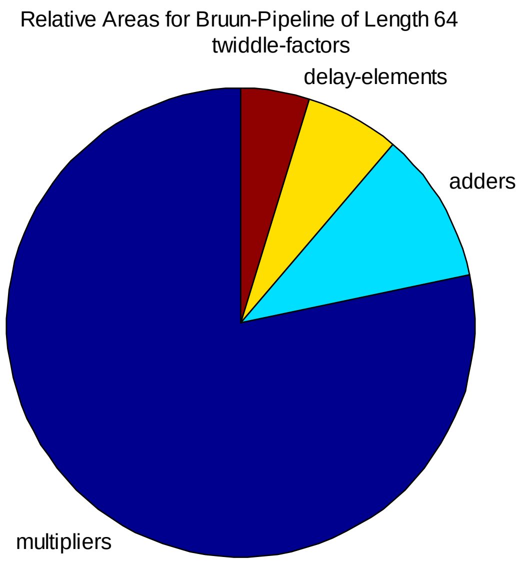
Estimated chip area of the Cooley-Tukey- and the Bruun-Pipeline for a 65nm-process, 16-bit wordlength equivalent.



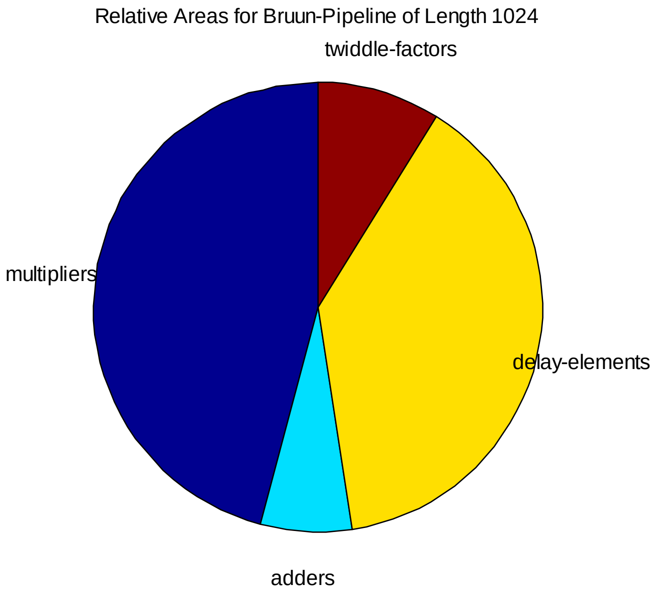
Area savings of Bruun-Pipeline over Cooley-Tukey-Pipeline depending on the FFT-size, and wordlength b.

- **Largest area savings for N = 32 to N = 64 → 40% to 50% (WLAN)**
- **For N = 1024, 2048 still up to 25% savings (DAB, WiMAX, DRM)**

Reason for Bruun FFT Advantage



Relative Areas for Bruun-Pipeline of Length N=64, b=16.



Relative Areas for Bruun-Pipeline of Length N=1024, b=16.

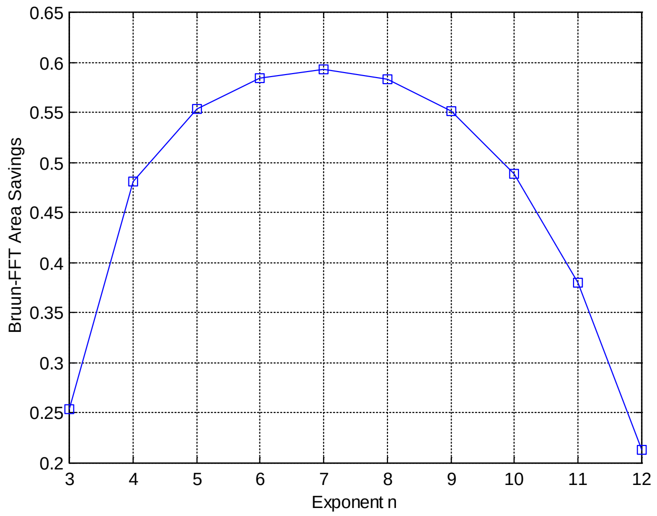
No. of real-valued multipliers:

$$n_{mult,CT} = 4 \cdot (\nu - 2)$$

$$n_{mult,Bruun} = \nu$$

→ For transform lengths where area of multipliers is dominant the Bruun FFT excels

Area estimation for CT-FFT and Bruun FFT (FPGA)



Area savings of Bruun-Pipeline over Cooley-Tukey-Pipeline depending on the FFT-size, assuming a fixed size 25x18-bit multiplier (e.g. Xilinx Virtex6 ®). Coefficient wordlength assumed to stay at 16 bits.

- **Largest area savings for N = 128 → almost 60%**
- **Even for N = 4096 still more than 20% savings**

[1] Storn, R., Some Results in Fixed Point Error Analysis of the Bruun-FFT Algorithm, IEEE Trans. Signal Proc., Vol. 41, No. 7, July 1993, pp. 2371 – 2375 .

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- OFDM systems require FFT/IFFT-algorithms that operate on real-valued time samples
- High-speed requirements make pipeline FFT architectures attractive
- Bruun FFT lends itself to a very efficient pipeline implementation with a low number of multipliers
- Even though Bruun FFT exhibits higher quantization noise it requires less chip area for ASIC and FPGA implementations
- Depending on the transform length N the area savings peak around 50% for ASIC designs and 60% for FPGA designs

Thank You For Your Attention !