SOFTWARE DEFINED RADIO – DIFFERENT ARCHITECTURES FOR DIFFERENT APPLICATIONS

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ABSTRACT

The development of low cost flexible hardware solutions for Software Defined Radio (SDR) to service multi-band multi-protocol devices continues to be a challenging task. Software Defined Radio has the potential to offer the commercial world multi-purpose platforms which can help them profitably deliver low cost and flexible solutions. Reconfigurability will lead to dramatically reduced development cycles and enables faster time to market.

To realize those benefits, a multi-mode, multi-protocol SDR consumer device which can support multiple applications must be able to deliver the performance required by each application. Much time has been spent both in literature and development on evaluating and solving the modem portion of SDR architectures. This paper will focus on the benefits of different reconfigurable Radio Frequency (RF) hardware approaches. These approaches are evaluated and contrasted to one another. RF super-sampling, RF sub-sampling, multi-transceiver integration and tunable architectures are compared for a selection of different requirements. Voice, video and data radio protocols are considered in this discussion.

Tunable architectures in particular offer designers the ability to better optimize the radio performance since it offers more degrees of freedom to the system engineer who implements a particular application on the radio architecture. Until now tunable RF architectures have proven difficult to implement due to the inherent complexity involved in designing components with multiple operating points on silicon. Recent advances in silicon development and component architectures have enabled the implementation of tunable RF architectures which meet commercial goals for cost, size, performance and time to market.

1.0 INTRODUCTION

The continued demands from consumers for mobile connected devices such as handsets, PDAs, gaming devices, MP3 players and other wireless devices that provide better connectivity and more features drive continued innovation in architectures and components. While the flexibility to support these new features is a relatively new requirement, it has always been necessary that they be offered in small footprints and with greatly reduced bill-of-material (BOM) prices. The historical approach in transceiver design has been higher and higher levels of integration. Integration has progressed from chip on board to system in a package to system on die. But the ability to integrate for cost and die area savings has become more and more difficult. Transceivers are analog devices and analog circuitry does not scale like digital circuitry does.

The ability of digital microprocessors to deliver an extraordinarily wide range of applications through a programmable architecture provides a model for radio designers. A reconfigurable radio architecture offers clear benefits to customer, carriers and OEMs. However, the question of how best to obtain cost savings while delivering improved performance, still begs for a conclusive answer and the challenge remains to provide a RF hardware platform which can be controlled by software and which is capable of providing a wide range of performance and which supports a wide range of radio protocols.

Today, system designers of single mode radio designs evaluate a set of possible architectures against the specified radio requirements to select the optimal architecture. Yet the performance required by a multi-mode, multi-protocol radio varies widely with each possible combination of applications and makes it difficult for system designers to converge on a simple architectural solution. As a result, each unique combination of bands and protocols requires a unique hardware solution. With rapidly increasing number of protocols and an increase in licensed spectrum, RFIC Independent Device Manufacturers (IDMs) must deliver more products at an accelerating rate to the market. Unfortunately, the long lead time associated with new RF products makes it difficult to predict future integration preferences and to staff the design team in a timely fashion. IDMs are forced to find other means to deliver the solutions quickly but without the tools or architectures to enable a reduced time to market, the IDMs will become increasing challenged to keep up the pace of development.

2.0 THE BENEFITS OF RECONFIGURABLE ARCHITECTURES

Software Defined Radio with reconfigurable RF architectures offer both a solution to the current challenges faced by wireless device manufacturers as well as a path to quickly creating new applications and functionality. Cognitive Radio (often defined as a radio capable of modifying its transmission characteristics to avoid interference) has been predicated on the development of a reconfigurable radio. SDR has long promised to be the foundation for cognitive radio, maybe it's time has finally arrived.

Reconfigurable architectures offer many benefits through the complete wireless value chain. Users seek devices that offer more applications in a single device than ever before. Reconfigurable devices can also provide adaptive performance and modify their operating characteristics (such as sensitivity and power) to suit the RF environment which currently surrounds them. Carriers will be able to provide software upgrades to RF performance and device functionality over-the-air (OTA). Device manufacturers will be able to deploy one platform into many product programs and simplify their supply chains. Inventory costs can be driven down. Reconfigurable radio has something to offer all members of the wireless value chain.

3.0 THE CHARACTERISTICS OF RECONFIGURABLE ARCHITECTURES

As was mentioned earlier, any new wireless architecture must meet commercial goals for performance, cost, size and power efficiency if it hopes for widespread adoption. The successful implementation of a reconfigurable or programmable architecture will depend upon the designers and architects ability to meet those fundamental technical and business requirements.

Although it is never simple to navigate the ocean of available bands and protocols and implement an architecture for a new application, the complexity is reduced when device vendors follow the tried and true path of integration. In moving to a reconfigurable architecture, system engineers and circuit designers must instead assess the required performance envelope and through a thorough survey of the required applications, identify the challenging performance benchmarks which exist for each protocol to be integrated. Once the performance envelope is identified, these same system engineers must then verify the ability of the reconfigurable device to meet those requirements.

In general, we can say that in order for a reconfigurable architecture to support multiple bands and protocols, it must:

- Change operating frequency band over the range of commercial communication bands
- Offer variable bandwidth
- Provide tunable and sufficient dynamic range
- Efficiently support both constant/non-constant envelope protocols
- Provide analog and digital filtering sufficient to meet protocol specifications for blockers and out of band emissions.
- Provide sufficient selectivity mode by mode
- Retune / reconfigure fast enough to allow for the handoff between multiple protocols (this could be the switching time necessary to implement compressed mode UMTS or also the time to switch between an outdoor GSM network and indoor UMA coverage)
- Minimize cost so that the reconfigurable architecture BOM is no more expensive than a single band/protocol BOM
- Provide an energy efficient architecture such that the power consumption in any mode does not exceed the power consumption of a single band/protocol RF ASIC

In past SDR solutions, attempts to cover multiple protocols result in over-designed solutions. Designers tried to meet each 'worse case' parameter for different bands and protocols simultaneously and the composite performance

Architecture	*Cost*	*Power*	*Size*	*Performance*	*Time to Market*
Supersampling	**Low**	**High**	**High**	**Highest**	**Short**
Subsampling	**Low**		**Med**	**Med**	**Long**
Multi-transceiver	**High**	**Lowest**	**High**	**High**	**Long**
Blended / Tunable Components	**Low**	**Low**	**Low**	**High**	**Short**

Table 1 Architecture Comparison

envelope becomes incredibly challenging resulting in a large and power hungry design.

Instead, today's successful reconfigurable architectures will be able to self-optimize for the application, band, protocol and environment in use. This ability to self-optimize and re-allocate resources within the transceiver will allow for a smaller more power-efficient design.

4.0 COMMERCIAL CONSIDERATIONS

. "Know your Customer" or a mantra just like it is often repeated within the marketing and engineering teams as a products are envisioned, defined and designed. But most customers have similar vision of quality. A quality product is a product that does the desired task at a price the customer can better afford than the previous product and comes in a small and appealing package. Price, Power and Size lie at the heart of almost every component decision made in designing consumer products today.

New architectures must provide a path to meet those goals as well as bring value beyond that. Time to market is a major concern in consumer applications and is an issue that can be addressed through reconfigurable solutions. A reconfigurable solution which meets price power size and time to market goals will certainly be one that demands the full attention of wireless device manufacturers

5.0 RADIO ARCHITECTURES

Super-sampling, Sub-sampling and Multi-transceiver architectures all carry their own particular advantages and disadvantages. In general, each architecture is most power-efficient in its designed operating band and mode. A comparison of those architectures is provided in table 1.

Super-sampling (or oversampling) architectures, where the sample rate is much greater than the Nyquist rate, enable the implementation of powerful digital filtering and post-processing to extract the signals of interest. This high sampling rate has the disadvantage that it requires a very high speed analog to digital converter (ADC) to provide that sample rate. For example, a 4x over-sampled signal requires a clock that is 8x the signal frequency. If one considers that doubling the clock doubles the power, then a 4x over-sampled signal will require 4x more power (in the ADC) than that of a signal sampled at the Nyquist rate. Therefore there is a tradeoff of power for performance which must be considered when evaluating super-sampling RF architectures for use in portable devices. In general, a highly over-sampled signal allows for the processing of low bandwidth high resolution signals yet quickly demands more power as the oversampling rate or desired signal bandwidth increases.

Sub-sampling architectures have not often appeared in the handset industry. A sub-sampled signal is commonly described as an architecture where an IF is sampled at the Nyquist Rate for the information when that rate is less than the IF. Sub-sampling presents a challenge in that the sampling circuitry must function at the IF frequency while the sampled data is at baseband. The additional circuitry required to manage that is complex and a final digital downconversion is required. An IF SAW may also be required.

Multi-transceiver architectures are generally based on traditional Low-IF and Zero-IF architectures. While design of these architectures is well understood and can be efficiently implemented, a multi-transceiver architecture still must scale with the bands and protocols needed in the application. A unique circuit (and associated silicon area) is required to support each unique protocol with incremental silicon for each band. Cost and die area reduction is limited by the designer's ability to further integrate these multiple transceiver paths on a single die.

An architecture consisting of tunable analog/mixed signal, RF and digital functional blocks offers the best of all worlds including the efficiency of the multi-transceiver design, the resolution of the super-sampled architecture and the smaller cost and size of the sub-sampled architecture.

6.0 ARCHITECTURAL COMPARISON

Super-sampling architectures (Figure 2) have been traditionally used in application requiring lower bandwidth with high resolution.

Pros

- High resolution
- Blocker rejection

Cons

- Power

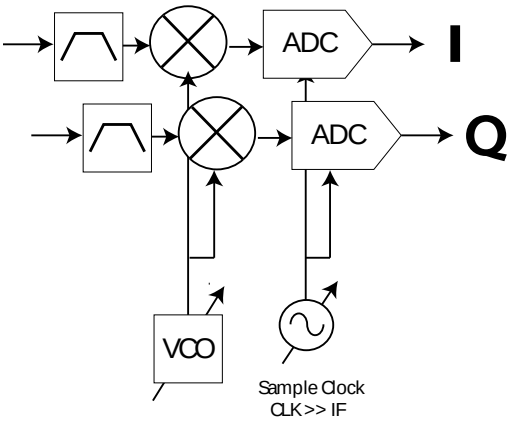

Figure 2 Super-sampling Architecture

Sub-sampling architectures (figure 3) have not often appeared in handset architectures as the architecture

typically requires the use of an IF SAW to limit the images prior to sampling in the ADC. RFCO, a California startup, attempted a sub-sampling RF Transceiver but was unable to bring a product to market before closing their doors.

Pros

- Smaller size (One ADC)
- Low cost

Cons

- Power

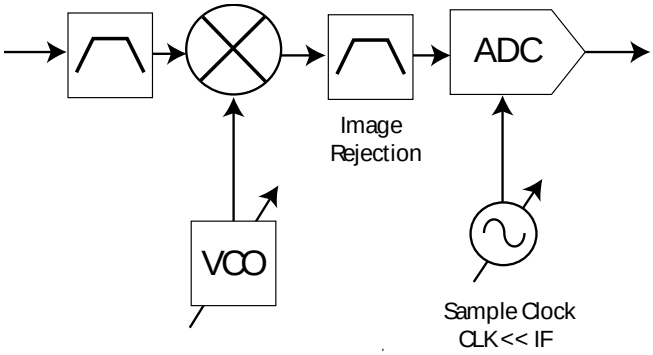

Figure 3 Sub-sampling Architecture

Multi-transceiver architectures (figure 4) have been the architecture of choice for handset designs however the rate at which designers can squeeze additional performance and die area out of existing architectures appears to be slowing.

Pros

- Power efficient in each band

Cons

- Size (scales with number of bands and protocols).

Tunable Components have only found limited application as the cost and power of SDR architectures has been high

Pros

- High resolution
- Blocker rejection
- Power efficient

Cons

- More complicated systems analysis

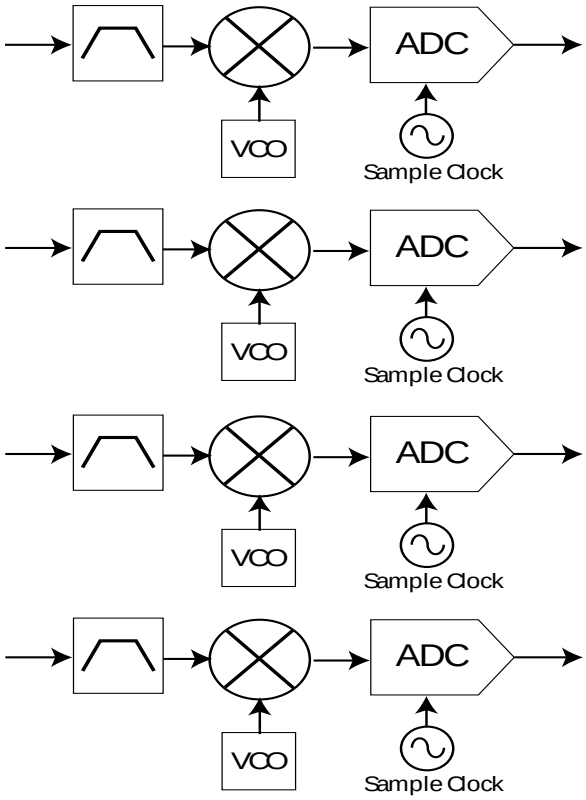

Figure 4 Multi-transceiver Architecture

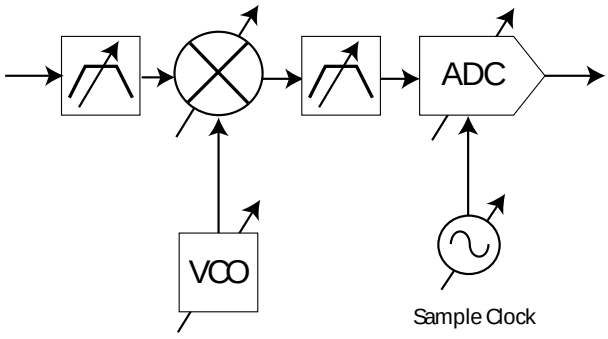

Figure 5 Tunable Component Architecture

Architecture	*Voice*	*Data*	*Video*
Supersampling	Improves resolution of NB signals		
Subsampling	Information rate must be << IF		
Multi-transceiver	Each transceiver path optimally designed for a unique band/protocols		
Blended / Tunable Components	Reconfigurable to deliver best performance for each band/protocol with minimal power/minimal die area		

Table 6 Architectural Pros/Cons

However, as can be seen in table 6, the architecture using tunable components has the capability to deliver the value required throughout the value chain on price, power and performance.

7.0 THE FUTURE OF SDR

SDR solutions offer benefits beyond that of price power and performance for today's wireless devices. SDR can impact supply chains, application sets and carrier network planning. But to do this, an architecture must be selected that delivers on those promises while continuing to meet commercial goals for price power and performance. While supersampling, subsampling and multi-transceiver architectures all can offer some degree of flexibility, none of them can offer the combination of flexibility and wide performance envelope necessary to support the ever growing set of bands and protocols that are deployed and are about to be deployed in today's market.

Many believe that the next phase in the evolution of radio is to cognitive radios which can both analyze their environment (both from a RF perspective and a network perspective) and then modify their transmission characteristics so as to most efficiently utilize the available spectrum. Truly reconfigurable architectures offer a path towards this goal. The ability for wireless devices and or networks to make choices on which bands and protocols to communicate over will lead to the next giant step forward in efficient and effective communications over the wireless spectrum.