DESIGN TRADEOFFS IN MAKING A TUNABLE TRANSCEIVER ARCHITECTURE FOR MULTI-BAND AND MULTI-MODE HANDSETS

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ABSTRACT

Wireless communications occur in a constantly evolving eco-system of licensed and unlicensed spectrum, complex end-user applications and innovation in terminal and infrastructure design. To satisfy the end-user and provide seamless connectivity, carriers and handset OEMs are developing multi-mode handsets which are capable of supporting diverse services over multiple networks. Though these handsets are increasingly complex, technology advances in material science, process technology and integration have all contributed to a steady improvement in the cost and performance they offer.

Advances in process technology generally lead to reduced power consumption and improved performance. Those advances are almost always leveraged to add new features. However the different performance required by each protocol in a multi-protocol multi-band solution, inevitably leads to compromises in cost and/or performance while the combination of technology advances and new features increases design time and complexity.

Tunable or reconfigurable transceivers have the potential to meet the performance targets of a multi-band multi-mode device while reducing cost and size. The benefits of a tunable transceiver derive from the ability of a small single transceiver to provide the same functionality as several purpose-built transceivers. These tunable devices, which are reconfigured either with software or under direct hardware control, require an architecture capable of allocating varying levels of performance across the functional blocks of the tunable transceiver. This architectural flexibility is exactly what is required in order to provide the reconfigurability required by today's devices while still achieving the expected power and performance requirements.

1.0 INTRODUCTION

Several transceiver vendors are developing multi-transceiver die in pursuit of a multi-band, multi-protocol radio. In a multi-transceiver die, each transceiver path can be uniquely optimized for the intended band and protocol. While this results in a high performance device, it increases the total die area. Designers have consequently struggled to meet the goal of increasing functionality for decreasing cost. They have evaluated many potential tradeoffs in their hunt for low-cost high performance devices. Among these tradeoffs, designers have chosen more expensive processes (RF CMOS or BiCMOS vs. Digital CMOS) to support a higher critical frequency (f_t); or designers may have implemented ADCs with higher dynamic range and thus accepted higher power consumption.

Rather than integrate several transceivers on one die in order to provide the desired multi-band functionality, designers have considered the possibility of a single broadband transceiver and transceiver channel which could support multiple bands and protocols. Until now, any attempt to integrate many protocols in one non-programmable, inflexible device using only one transceiver channel meant that each functional block within that channel needed to be designed to the most demanding performance requirement of each protocol in the application. In this "fixed function model", each design needs to account for the potential process and manufacturing variation that occurs in normal production. Designers have selected from a rapidly growing universe of IP and advanced technologies to create the architecture and implementation that best trades off power performance and cost AND meets their worst case analysis. Obsoleting this methodology requires a paradigm shift and the development of truly reconfigurable RF devices which can be configured for EACH individual protocol as well as for the RF environment that the device is operating in. A single

design can then be digitally optimized to compensate for process variation AND design corners since the inherent programmability of the transceiver allows the device to operate over a very wide range (frequency, bandwidth, noise figure etc).

The design of any multi-mode transceiver begins with an analysis of the required performance envelope (Figure 1). For each desired protocol, designers evaluate the radio characteristics such as noise figure, linearity and required rejection, etc. and combine them into a single composite performance envelope. For a reconfigurable architecture, the hard work now begins. In portable wireless devices, power is a dominant constraint to be optimized. System engineers must specify a unique configuration of the device for each desired band/protocol combination. The system engineer must analyze the possible tradeoffs and decide how to allocate such metrics such as gain though the transceiver chain as well as how to distribute filtering (analog, digital or external). In the tunable architecture considered in this paper, dynamic range, signal bandwidth and carrier frequency all can be correlated to transceiver power consumption. An analysis of the available performance and its impact on the fundamental performance targets used to assess transceivers demonstrates the value of the architecture.

Tunable architectures offer value though the complete device value chain. That value may appear as value to the end user when more applications are deployed. It may appear as value to the carrier since flexible devices enable carriers to deploy tunable devices across a fragmented spectrum map. Or it may appear as value to the handset OEM who is then able to support multiple product families with just one radio platform. In each case, reprogrammable radios will change the way radio are designed built and deployed. Reprogrammable basebands already exist in the market; the next hurdle is in the analog world. Transceivers, filters, power amplifiers and antennas must all become reconfigurable. The key to the successful implementation of tunable transceiver architectures will be their ability to deliver commercial performance with low power and low cost. Through the efforts of a broad spectrum of companies, the path to SDR and tunable architectures is already well understood. It remains for component vendors to execute on their product roadmaps and deliver tunable components to the market.

2.0 THE PERFORMANCE ENVELOPE

The successful implementation of a new tunable transceiver architecture will depend on its ability to cover the performance envelope required by a multi-band multi-mode handset. The graph in Figure 1 represents a qualitative view of the combined performance required by a radio designed to support WCDMA, GSM and 802.11g. Note that no single standard requires the highest performance for all metrics. The challenge has thus been to create a reconfigurable transceiver whose performance envelope (the grayed composite area) covers the widest possible set of applications. Analysis was performed to aggregate the worst case noise figure, IP2, IP3, bandwidth, sampling rates etc for all of the common commercial protocols deployed in the market today as well as for protocols which are being proposed for standardization. An example of that exercise is shown; the resulting composite performance envelope suggests a design target for a tunable transceiver.

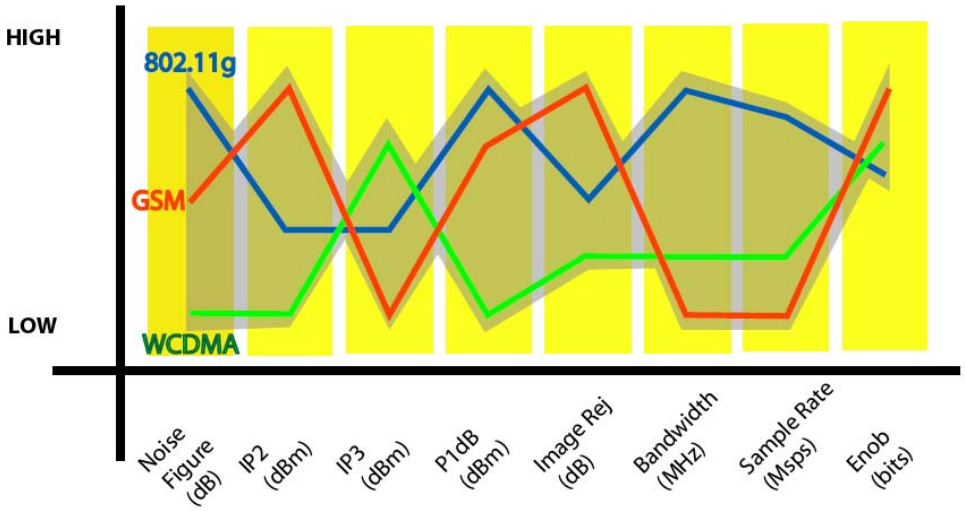


Figure 1 – Tunable Transceiver Performance Envelope

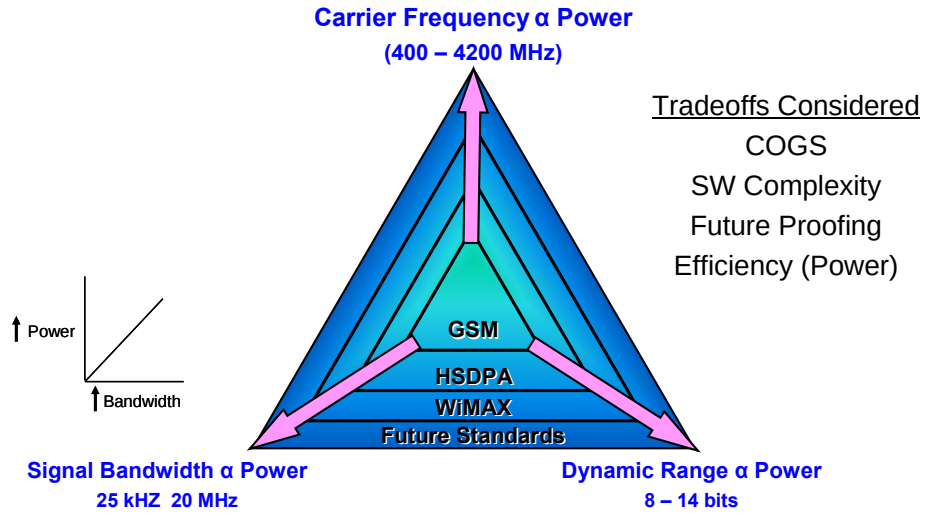


Figure 2 – Power Tradeoffs

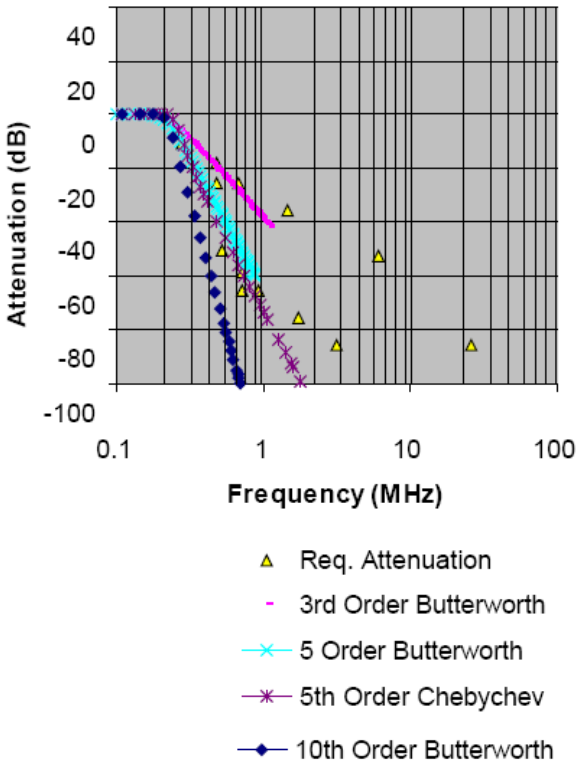
3.0 DESIGN TRADEOFFS AND CONSIDERATIONS

In creating a transceiver which meets this performance envelope, tradeoffs must be made. For portable applications, power is the critical constraint. Therefore the transceiver and its functional blocks were designed and analyzed with power consumption as the key metric. Many potential tradeoffs significant to the design of a transceiver involve power. Figure 2 illustrates the multiple dimensions in which these tradeoffs can occur. Wider bandwidth higher frequency applications drive the devices maximum power consumption.

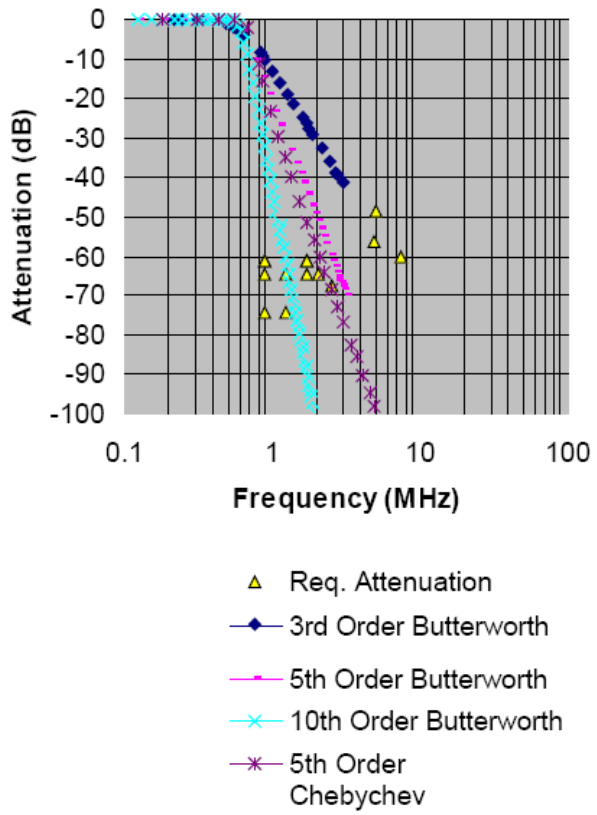
In particular, many of these tradeoffs cannot be avoided. For example, higher power consumption results from higher frequencies because of parasitic capacitance. Parasitic capacitance lowers the drive point impedance and thus it takes more current to get to the same voltage level. Supply voltage is fixed; therefore power consumption goes up.

Dynamic Range can also be traded off for power since analog to digital converters (ADCs) requires more transistors to deliver more effective bits of resolution; higher dynamic range in an ADC thus will require more power. Higher BW leads to more power consumption since more samples must be taken in order to accurately capture the information. Maintaining the same resolution at ever larger bandwidths implies higher sampling frequencies and thus more power. Additionally, more bandwidth requires the poles in amplifiers to be pushed out to 10x the operating bandwidth and this also drives an increase in power consumption.

Although these aforementioned tradeoffs allow for a broad flexibility in design and application, there is still a fundamental limit in frequency for each process node as determined by the f_t of the process. The value of reprogrammable RF has only just become comparable with fixed techniques as the f_t of currently implemented processes allows for coverage of many licensed and unlicensed bands. Typical analysis indicates you can expect useful performance up to f_t / 10. As one example, 130nm digital CMOS has a f_t of ~70 GHz and accordingly, a 130nm digital CMOS transceiver can see useful



Graph 3 – GSM Analog Filter Design



Graph 4 – CDMA 2000 Analog Filter Design

performance in a wide variety of applications up to frequencies of 7 GHz which allows a reprogrammable transceiver to cover standard licensed bands for GSM, WCDMA, WiFi, WiMAX and many others.

Tunable architectures also require one tradeoff that traditional architectures do not; tunable architectures require the addition of digital control circuitry in order to exercise the desired reconfigurability. In assessing the value of a reconfigurable transceiver, this additional digital logic affects the final cost but is of minimal impact in today's CMOS process technology.

The final analysis is made at the system level where the implementation is evaluated against the requirements of each protocol considered for the application. A tunable transceiver will contain multiple functional blocks including an LNA, mixer, analog filtering, gain blocks, an analog to digital converter and multiple stages of digital filtering. It may also include a finite state machine to independently sequence the transceiver's call control configurations. Each system level parameter (i.e. gain, noise figure, spectral mask and blocker rejection) may be implemented though a very large combination of settings. For example, when implementing various protocols, gain can be allocated to the analog, the mixed signal or the digital blocks in the circuit so as to minimize noise figure.

Blocker rejection can be accomplished though more selective analog filters or (if higher power consumption is acceptable) could be accomplished though increased dynamic range in the ADC followed by digital filtering. If we compare and contrast the blocker specs for CDMA2k and GSM, we see that:

- GSM
  - +9dB interference in adjacent channel (200 kHz)
  - +41 in 2nd adjacent (400)
  - +49 in 3rd adjacent (600)
  - +76 beyond 3 MHz
- Cdma2k
  - +71dB tone at 900 (or 1250) kHz (depending on band)
  - +57 at 7.5 MHz
  - +71 at 60 MHz (out of band)

Graphs 3 and 4 depict plots of the specifications along with the simulated performance for various analog filters. We can conclude that for GSM, the analog filter transition band doesn't have to be very narrow, but the ultimate filter rejection at alias frequency has to be high. On the other hand, for CDMA2K, the analog filter must be very sharp to knock down the 900 kHz blocker (or else the ADC must have 'dB for dB' higher dynamic range), but the ultimate in-band rejection does not have to be as high. Any gaps between the simulated analog filter performance and the performance required for blocker rejection must be covered by the digital filter.

Key tradeoffs are made in choosing the appropriate analog filter and in selecting an ADC with sufficient dynamic range to allow the digital filters to eliminate blockers. In the CDMA2000 analog filter example, the gap between the best analog filter performance shown in the graph and the 900 kHz blocker requirement clearly illustrates that a high performance digital filter is required to ensure spec compliant performance.

In table 5, a comparison of the overall analog and digital filtering requirements for multiple common protocols illustrates the wide variation in filter performance required and is an indication of the tradeoffs possible in implementing multiple protocols in a tunable transceiver.

	Analog Filters	ADC Res.	Digital Filtering	Archi-tecture
GSM/EDGE	> 90 dB rej @ sample frequency	> 75 dB	>30 dB rej @ 400 kHz	LIF
WCMDA	> 75 dB rej @ sample frequency	> 52 dB	RRC with > 40 dB rej @ 2.7 MHz	ZIF
CDMA2K	> 40 dB rej @ 900 kHz	> 60 dB	> 40 dB rej @ 900 kHz	ZIF
WiMAX	> 30 dB rej @ 2nd adj channel	> 56 dB	> 30 dB rej @ 1st adj channel	ZIF

Table 5 – Tradeoff Comparison for Wireless Protocols

4.0 APPLICATIONS AND BENEFITS

Tunable RF architectures have the potential to transform radio design. A single transceiver, configured with software to support multiple protocols has the potential to impact many aspects of the wireless value chain. End users benefit from devices which can be reconfigured to support new applications as well as legacy services currently deployed. Those services can be deployed and activated upon initial provisioning or later once fielded.

With the development of a tunable transceiver, new opportunities are created. Carriers could add new bands without having to replace all deployed terminals. Assuming a flexible baseband and wideband power amplifier and band filters, the terminals would be able to be reprogrammed to work in the newly acquired spectrum.

The tunable architecture also enables OEM benefits such as design reuse and design time reduction as well as the implementation of product families based on a tunable platform. This will support inventory reductions through the adoption of common RF platforms in a device vendor's product portfolio.

But apart from their current value, reconfigurable RF supports the vision of a radio which is capable of making decisions in real time based on the current RF environment and network usage. A radio capable of making decisions around the communications channel, also known as cognitive radio, support future goals for dynamic spectrum allocation and utilization and is one piece of the technology puzzle that will support continued improvements in the quality of our wireless communications.

5.0 CLOSING

Tunable or reconfigurable transceivers have the potential to meet the performance targets of a multi-band multi-mode device while still meeting cost, power and performance benchmarks as a commercial solution. The benefits of a tunable transceiver derive from the ability of a small single transceiver to meet the performance requirements of multiple bands and protocols. These tunable devices, which may be reconfigured with software or under direct hardware control, require an understanding of the tradeoffs necessary to allocate performance across the functional blocks of the tunable transceiver. This architectural flexibility is exactly what is required in order to provide the reconfigurability required by today's devices as well as set the stage for the adaptive radios of the future.