THE DESIGN OF FLEXIBLE FRONT END PROCESSING FOR CIREN

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ABSTRACT

This paper presents the design of a front end for CIREN which uses FRS spectrum as a secondary user. The main goal of the front end is to alleviate an unnecessary burden on a processor and to provide the flexible configuration required by the processor. The design is done on the platform of SFF-SDR. The platform is briefly introduced and a DIF design is discussed in detail. The functions of the DIF are down/up-conversion, decimation, interpolation, and channel sensing. To make a programmable feature for these functions, a DDS and a CIC filter are used. Currently, RX-path in the DIF is completed and TX-path is being designed.

1. INTRODUCTION

The Cognitively Intrepid Radio Emergency Network (CIREN) is an on-going project [1], which exploits cognitive technique for the efficiency of spectrum usage and the reliable communication. CIREN (as a secondary user) will use Family Radio Service (FRS) spectrum consisting of fourteen 25kHz-wide channels distributed across a range of frequencies between 462MHz to 467MHz in the UHF television band. Even though most of the functions such as cognition/adaptation and modulation/demodulation are performed through a software engine running on a TI DM6446, front end processing is crucial due to the limitation of the processor's speed. For that reason, the whole CIREN system consists of three types of signal processing – RF signal processing, digital intermediate frequency (DIF) signal processing, and baseband digital processing.

This paper describes the design and analysis of an RF signal and a DIF signal processing part in detail. The RF signal processing module converts an RF frequency to an IF frequency for further processing during the reception and vice versa for the transmission. We have implemented the control signals which control the various functions of the RF module from the processor. On the other hand, all the quadrature down/up-conversion, decimation and interpolation are implemented in the DIF module. So, this paper also describes the implementation strategy of the quadrature down/up-conversion, decimation, and interpolation. Currently, the DIF design for RX-path, down-conversion and decimation, is completed. For flexibility to various types of received signals and to requirement from the processor, our design supports a programmable frequency for direct digital synthesis (DDS) and programmable rates for the decimator and the interpolator which are implemented by Cascade Integrator Comb (CIC) filter with Hogenauer filter structure. We also implemented a fast channel sensing through Fast Fourier Transform (FFT). A TX-path DIF, and the interfacing between the DIF module and the baseband digital signal processing module, will be implemented soon. The interfacing and baseband signal processing will be done using video processing subsystem (VPSS) technique. The Small Form Factor (SFF)-SDR board [2] from Lyrtech Inc. is used as a hardware platform to implement all of the described functions.

The rest of the paper is organized as follows. Section 2 introduces a hardware platform which is used and Section 3 describes the design of a DIF module for flexible features. In Section 4, the verification of a design accomplished so far is presented. Finally, the future work is mentioned and conclusion is drawn in Section 5.

2. THE BRIEF OF HARDWARE PLATFORM

The overall structure of a SFF-SDR board from Lyrtech is shown in Figure 1, which is composed of an RF module, a data conversion module, and a digital processing module. The RF module covers 20 to 928 MHz in receiving and 200 to 930 MHz in transmitting. For receiving, intermediate frequency (IF) is located at 30 MHz and there are two selectable bandwidths: 5 or 20 MHz. The data conversion module includes two ADCs and one DAC. ADC output bit-width is 14-bit and its speed is up to 125 Msps [3]. DAC has a 16-bit dual-channel with 500 Msps [4]. The default

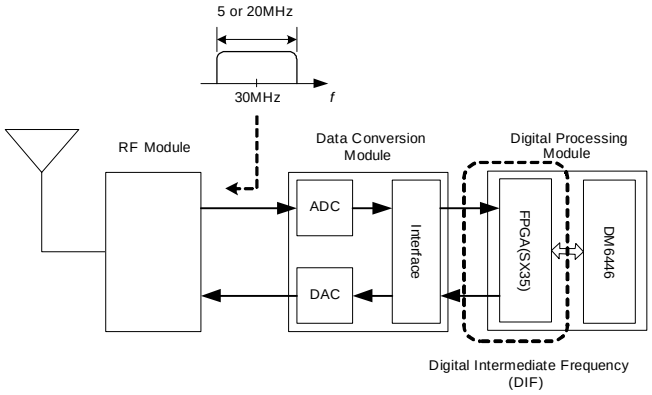


Fig. 1: The overall hardware platform (SFF-SDR).

speed of the ADC and DAC is 10 MHz, but it can be adjusted through an external clock port. For interfacing to the digital processing module, an FPGA (Virtex-4 LX25) is used. This FPGA is not configurable. The baseband module features Xilinx Virtex-4 SX35 FPGA and TI TMS320DM6446 DSP chip. Virtex-4 SX35 FPGA is configurable according to the specific application, and the TI chip contains a TMS320CC64x+ digital signal processor (DSP) core and an ARM9 general-purpose processor (GPP). This DSP supports high speed complex signal processing. The GPP performs networking and application processing.

3. FLEXIBLE DIF DESIGN

The main functions of a DIF are the quadrature down/up-conversion, decimation, and interpolation. Additionally, an FFT is implemented in RX-path, which is exploited for fast channel sensing. The configuration of the DIF is shown in Figure 2. This design is implemented on Virtex-4 SX35. For the flexible DIF, the design supports 1) a programmable frequency for down/up conversion and 2) programmable rates of decimation and interpolation.

Before we introduce the details on the design, it is worth discussing the sampling rate of ADC for this application. To use a low ADC sampling rate, we use a bandpass sampling whose sampling rate is given by [5]

$$2B \le F_S \le 4B \qquad (1)$$

when f_c/B » 1, where f_c is the center frequency in passband and B is the passband width. In the design, with the IF configuration of B=5 MHz and f_c=30 MHz, the sampling rate is set as 12 MHz. Note that this sampling down-converts IF signal to near baseband and the spectrum is flipped in 0 to $F_S/2$ range.

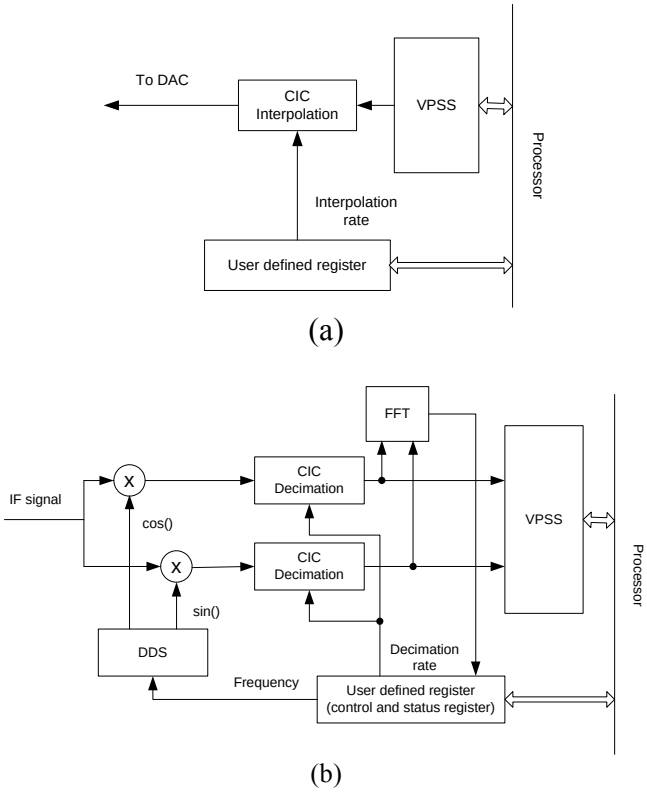


Fig. 2: The configuration of the DIF: (a) TX-path and (b) RX-path.

In the DIF, there are four components: a CIC filter for decimation and interpolation [6], Direct Digital Synthesis (DDS), a multiplier, and an FFT. The impulse response of the CIC filter is a box car or a sliding average filter. But the CIC filter has a multiply-free structure, a cascade of integrator and comb filter. This significantly reduces hardware complexity. For decimation and interpolation, the CIC filter absorbs the resampling operation, leading to a Hogenauer filter structure (a differentiator and an integrator), shown in Figure 3 [7]. Note that even though the structure is different, its impulse response is still a box car. Due to its poor filter response (13 dB attenuation), a multistage CIC is used to improve the filter performance. With the cascade of K length-M CIC filters, the frequency response is given by

$$H_K(\theta) = \left[\frac{\sin(\theta M/2)}{\sin(\theta/2)} \right]^K \qquad (2)$$

where θ is angle ranging from $-\pi/2$ to $+\pi/2$. Note that length-M corresponds to the changing rate in Hogenauer

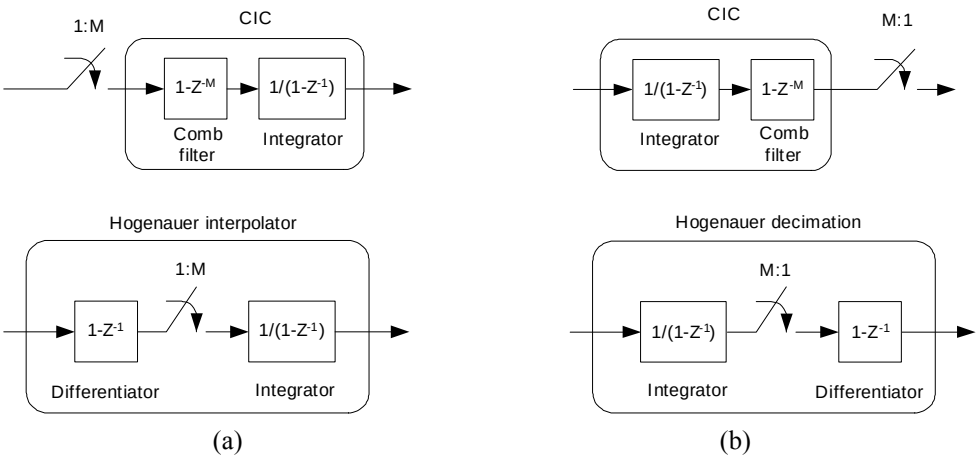


Fig. 3: The Hogenauer filter structures. (a) Interpolation and (b) Decimation.

structure as shown in Figure 3. For the correct operation, the addition in the CIC filer must use 2's complement arithmetic and the accumulator's bit width must exceed the width required by a filter output which is

$$b = b_{in} + CEIL\left[K \log_2 M\right] \qquad (3)$$

where b_{in} is the bit width of input. In our design, we use a 4-stage CIC filter, its input bit width is 16, and its final output bits are truncated to make 16 bit width output according to the changing rate of M.

To generate sinusoids for down-conversion, Direct-Digital Synthesis (DDS) is used due to its flexibility from its digital nature. The DDS is generally composed of a phase accumulator and a look-up table. The look-up table stores samples of sinusoid. The design is done by Xilinx DDS compiler v1.0 [8] and the output frequency in Hertz is defined by

$$f_{out} = \frac{f_{clk}\Delta\theta}{2^{B_\theta}}$$

where f_{clk} is the clock frequency, B_θ the bit-width of phase accumulator, and $\Delta\theta$ the phase increment. The designed DDS has the output bit-width of 6 and B_θ of 24.

A multiplier and an FFT are implemented through Xilinx multiplier v9.0 and Fast Fourier Transform v3.2 [9][10]. A 64-point FFT is used and it is designed to support streaming I/O. The channel sensing is done by threshold test with FFT and it is stored in user defined register and is read by the processor for channel sensing.

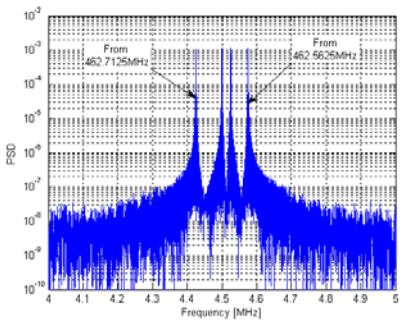
4. DESIGN VERIFICATION

At this time, the RTL design for the RX-path is completed in verilog-HDL. We simulate the design in MATLAB and verilog compiler to verify the RTL design by comparing the results. The simulation condition is:

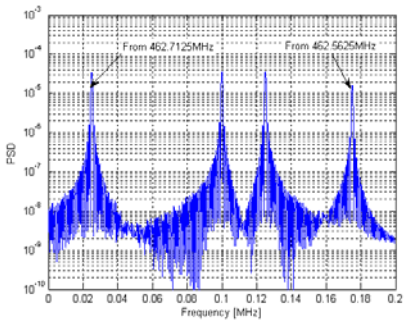
- The input vector to the design is the output of ADC, which is obtained by 12MHz-sampling on 5 tone signals at IF of 30 MHz. The frequency range of 5 tones is set to represent a low seven channel range in FRS band.
- f_{out} is 4.4 MHz (f_{clk}=12 MHz and $\Delta\theta$=hex5dddde).
- Decimation rate is 30, which leads to the decimated sampling rate of 400 kHz for upper/low 7 channels.

In the condition, $\Delta\theta$ and decimation rate are programmable. With the 64-point FFT and 400 kHz sampling rate, the frequency resolution of the FFT is 6.26 kHz. This is quite enough to distinguish 25 kHz-wide channels.

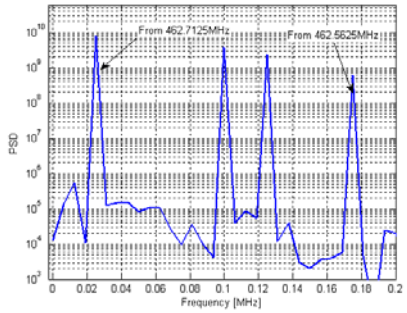
Figure 4 shows the periodograms [5] from simulations. Figure 4 (a) is the input vector to the design. The time-sequence of this is generated in MATALB and is imported at verilog-HDL RTL simulator. The downconversion/ decimation result from MATLAB is shown in Figure 4 (b) and that from RTL simulation in Figure 4 (c). They are almost same, which verifies the RX-path RTL design. Note that in RTL simulation result, the signal strength decreases as frequency increases since the passband frequency response of the 4-stage CIC still looks like a sinc-function. But this attenuation can be compensated by the processor because the response is known.



(a)



(b)



(c)

Fig. 4: The periodograms from simulations. (a) Input to the design (RX-path), (b) Decimated signal in MATLAB simulation, and (c) Decimated signal in verilog-HDL simulation.

5. FUTURE WORK

This paper presents the design work on a flexible front end for CIREN. The RX-path is accomplished so far and the current design features the programmable downconversion frequency and decimation rate. In addition, a 64-point FFT is implemented to support a fast channel sensing. The FFT result can be directly used for the sensing through the threshold test on its magnitude. It can also be exploited for the other sensing methods such as spectrum correlation.

For future work, the TX-path design is going to be finished soon. After that, we will do a test with the SFF-SDR Platform having the whole complete design. In the test, programmable features will be controlled dynamically and the sensing performance will be evaluated.

6. REFERENCES

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