SYNTHESIZING FPGA CORES FOR SOFTWARE DEFINE RADIO

John Huie (General Dynamics Decision Systems, Scottsdale, Arizona, john.huie@gdds.com); Price D'Antonio (General Dynamics Decision Systems, Scottsdale, Arizona, price.d'antonio@gdds.com); Robert Pelt (Altera Corporation, San Jose, California, rpelt@altera.com); Brian Jentz (Altera Corporation, San Jose, California, bjentz@altera.com)

ABSTRACT

The paper describes the integration of two separate waveforms (FM and Spread Spectrum) in a new prototype development of a software define radio.

The FM modulator and demodulator were integrated into one signal processing core capable of performing the modulation and demodulation of a 5Khz audio signal.

Waveform processing for the Spread Spectrum Waveform (SSW) proved to be a challenge due to the wide bandwidth of the waveform, and due to the high signal processing requirements for high data rates greater than 10Mbps. Since the waveform is going through evolutionary change during its development cycle, the prototype design meets both current waveform requirements and maintains sufficient flexibility to accommodate additional processing and evolution of the waveform.

1. BACKGROUND

The concept of a Software Defined Radio (SDR) has been around for more than 10 years. The ability to perform field upgrades and reconfiguration of waveforms has a large benefit to the military community. But, only recently has semiconductor technology evolved to make SDR possible. Typical architectures implement waveforms in the digital domain using Microprocessors, FPGAs, and DSP Processors. This paper focuses on implementation using a single FPGA. FPGAs have specific features that enable high performance SDR implementation while retaining cost effectiveness. These include: high-bandwidth memories, embedded DSP Blocks, phase-locked loops (PLL), general purpose processors (GPP) and high-speed interfaces. In addition, soft core processors plus FPGA co-processors enable reconfiguration of the digital waveforms.

2. DIGITAL RADIO ARCHITECTURE

Figure 1 shows a figure of a common FM radio architecture. In traditional radio architectures, all of the FM modulation and demodulation is performed in the analog domain. The processing power of digital components can now easily perform these operations. The first step in a digital radio architecture is to perform the exact analog functions in the digital domain. This can be done in three ways: 1) perform the signal processing as software on a soft core general purpose processor (GPP) or on a soft core digital signal processor (DSP), 2) perform the signal processing as hardware implemented as firmware in the FPGA, or 3) perform the signal processing as a micro-sequenced co-processor supporting specialized instructions for the DSP.

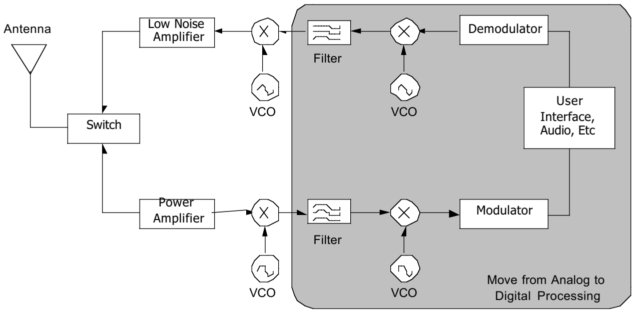


Figure 1: FM Radio Architecture

The customary signal processing implementation is to use a microprocessor (or DSP) to perform the radio functions. This allows the waveform developer to use a standard software language, and remain hardware independent. However, a DSP has limitations in performance that restrict DSP solutions to relatively narrowband waveforms. AN FPGA based solution allows flexibility to achieve a high degree of parallelism in signal processing, whether using multiple soft core processors or using firmware based coprocessors to substantially outperform DSP based implementations of waveforms.

3. PROCESSOR BASED DEMODULATION

Figure 2 shows a typical radio system using a microprocessor (or DSP) as the baseband processor. In this case the processing is performed by a 'soft core' microprocessor. Soft Core processors are built using the generally available resources in an FPGA. Typically these processors can provide 100 – 150 Dhrystone MIPS (DMIPS). This is enough processing power to perform modulation and demodulation for low bandwidth signals. Furthermore, currently available FPGAs can support from 2 to 50 soft core processors depending on the size of the FPGA selected. The System on Programmable Configuration (SOPC) Builder allows the user to build custom instructions for the soft core processors, improving the performance of the processors to meet future growth of waveforms for the software defined radio.

When the processing power needed exceeds that of the soft core approach, co-processing elements can be added. DSP Builder tool is tightly coupled with Matlab Simulink, which provides system level behavior that generates HDL code targeted to a specific family of FPGA devices. Figure 3 shows an example of the same FM radio that uses a CORDIC (COordinate Rotation DIgital Computer) co-processor. The CORDIC co-processor implements a vector rotation engine that can be used to calculate trigonometric functions [1]. In the case of FM, the CORDIC provides the arctangent function needed to demodulate FM waveforms. Table 1 shows typical performance of soft core processors and CORDIC co-processors.

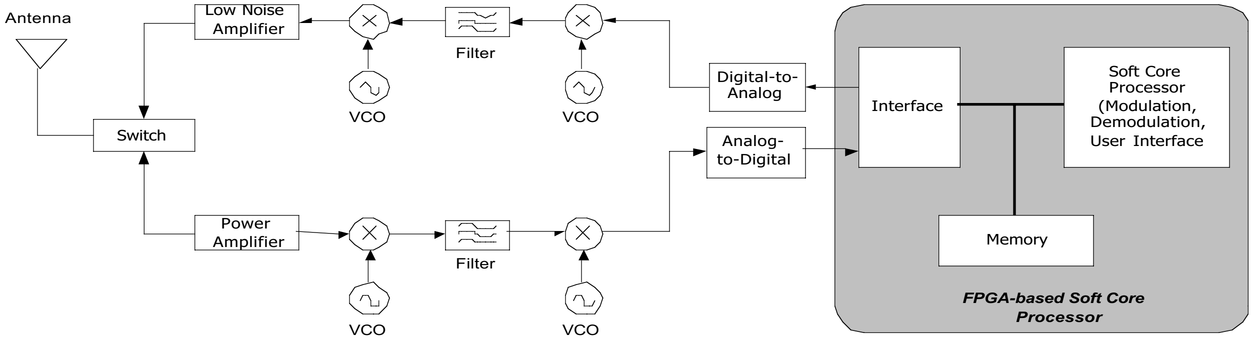


Figure 2: Processor Based FM Radio

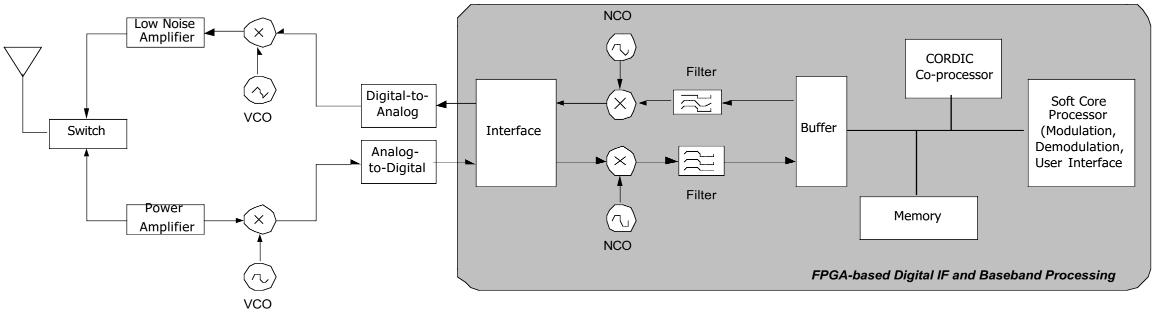


Figure 3: FM Radio with Digital IF

Table 1: FM Radio Components

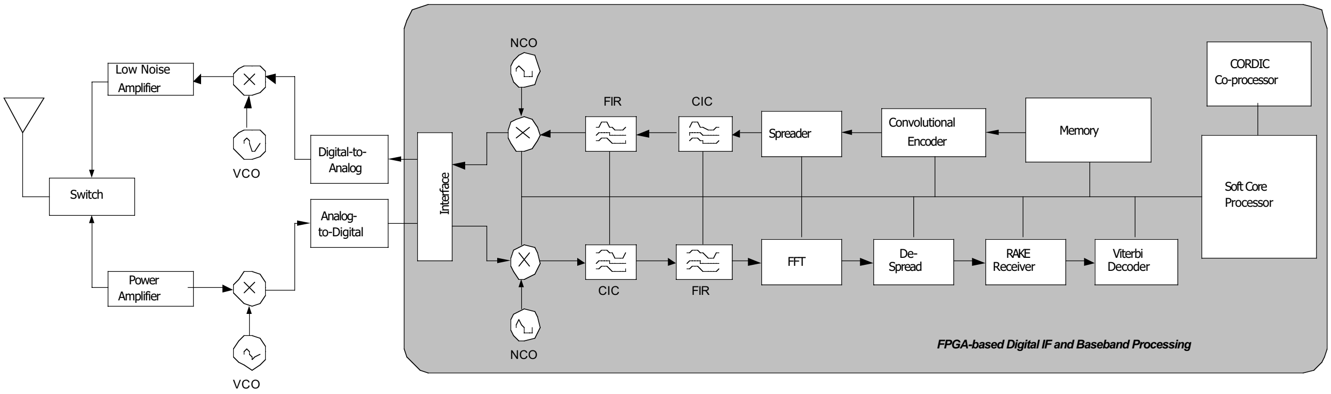
Function	Speed	Resources
Soft Core (Altera NIOS)	100 MHz	1500 LE
CORDIC	219 MHz	966 LE

4. DIGITAL IF PROCESSING

FPGAs are capable of more than baseband modulation and demodulation. Today's advanced FPGAs have the capability to provide IF (Intermediate Frequency) processing as well as baseband processing. Figure 2 shows the FM radio architecture with IF processing. In this implementation the VCO (Voltage Controlled Oscillator) is replaced with an NCO (Numerically Controlled Oscillator). The analog filtering functions are now replaced by digital FIR (Finite Impulse Response) filters. The Soft Core processor (along with the CORDIC co-processor) still performs the baseband processing functions. The Soft Core processor can also support adaptive changes of the IF performance. For example, the Soft Core processor can update the output frequency of the NCO, or change the coefficients of the FIR Filter.

Today's FPGAs are capable of supporting IF sampling rates up to 150 MHz.

Table 2 shows some utilization and clock rates for the IF processing functions.
Utilizations based on Altera's Stratix FPGA Family are:



- LE: Logic Element, basic element of an FPGA
- Mult: The number of 18x18 Multipliers used
- M4K: Embedded 4 Kbit memories
- MSPS: Million Samples Per Second
- Note: Resources based on [2], [3]

Figure 4: SSW Implementation

Table 2: Digital IF Components

Function	Speed	Resources (LE/Mult/M4K)
Parallel FIR (48 taps, 14-bit)	244.26 MSPS*	1375 / 0 / 30
Serial FIR (48 taps, 14-bit)	19.33 MSPS*	360 / 0 / 6
NCO (24-bit)	278.78 MHz	67 / 8 / 12
CIC (6th order, 14-bit)	200 MHz	1138 / 0 / 0

diagram of the SSW implementation in an FPGA. In this implementation, most of the waveform processing is performed by co-processing components. Each of the co-processing components are generated by DSP Builder through Matlab Simulink. A high level model of the co-processing components are simulated in Matlab Simulink. In Simulink, the co-processing components have their own built-in compiler to generate a RTL (Register Transfer Level) model for simulation in Modelsim with its associate test bench stimulus. The Simulink models of the co-processing components are FPGA centric such that it takes advantage of the hardware architecture for a given family of FPGA devices. But, as in the FM case, the Soft Core processor performs the initialization, parameterization, tracking loops and adaptivity management for the co-processors. Notice that the CORDIC coprocessor is still available to perform FM waveform processing.

Table 3: SSW Components

Function	Speed	Resources (LE/Mult/M4K)
FFT* (128 ppt)	1.03 _sec	4838 / 9 / 19
FFT* (2048 ppt)	8.38 _sec	7952 / 18 / 44
FFT* (8192 ppt)	38.73 _sec	8388 / 18 / 176
Viterbi Decoder	11 Mbps	1801 / 0 / 0

* Two Radix 4 Engines, 16-bit operation

** Constraint length = 7, number ACS = 8

Note: Resources based on [4], [5]

5. IMPLEMENTING SPREAD SPECTRUM WAVEFORM (SSW)

The concept of 'co-processing' can be extended to support more computationally intensive waveforms, like the SSW waveform. Table 3 shows that the waveform requires processing rates that are far beyond the reach of traditional microprocessors. Co-processing components increases performance requirements and provides additional computational resources when needed to alleviate software overhead and minimize event cycles in order to reduce power consumption.

6. SYSTEM IMPLEMENTATION

The software defined radio (SDR) form factor drives power requirements for the design. The SDR system comprises of two modules, the digital baseband module and the RF module. The antenna and Human Machine Interface (HMI) are part of the chassis frame that enclose the RF and Digital module. Through the advancements in package technologies the RF and Digital components on the module can fit into two separate IC packages. Using mixed signal technologies the RF and Digital circuitry can fit into one substrate by minimizing interference between the analog and digital systems. Furthermore, digital signal processing techniques can compensate for some of the limitations in semiconductor and passive components such as capacitors and inductors to meet stringent RF requirements.

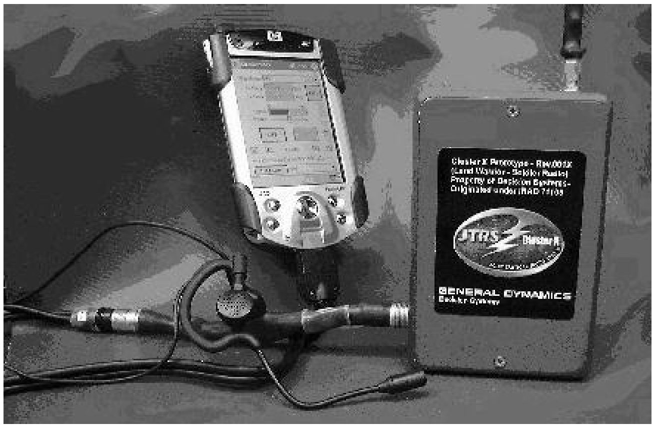


Figure 5: Small Form Factor Prototype

A small form factor prototype baseband module has been built. The circuit card measures 5 square inches, using 14 layers, .062 inch thick. Three power planes, three supply ground planes, two signal ground planes (analog and digital), and six signal layers provides the necessary isolation to minimize coupling between the RF and digital circuits. Minimizing the pin count connectivity for the HMI interface and the RF module further reduces the board size.

High speed signals around the FPGA are integrated into the inner layers to reduce EMI coupling throughout the digital board. Matched length signal traces for high speed signals ensure the impedance of the signal traces is 50 ohms. The six signal layers are interleaved between the supply planes. Static and control signals with low clock edge rates are routed on the top and bottom layer of the digital board. SMPS (Switch Mode Power Supply) provides 1.5V, 3.3V, and 5V for the digital board. A 7.2V to 12V DC input voltage provides the main input voltage for the digital board. The efficiency of the power supply design is 90%.

A simple discrete reset circuit is used to initialize the FPGA, Flash, UART transceivers, HMI interface, and RF interface. In addition, a soft rollback is provided through the RF module interface to prevent continuous transmission at the 5 watt level greater than 1 minute. The incoming I and Q data from the data converter of the RF module is processed through the FPGA (modem) and then sent through the transceiver interface into a handheld personal assistant, similar to the HP IPAQ model 5550. Based on the overall throughput rate and latency in the system, WLAN should support streaming audio on demand. The handheld personal assistant is the HMI for the prototype SDR. Outgoing data from the handheld personal assistant is sent through the transceiver interface and the FPGA (modem) prepares the data for transmission then sends the I and Q data to the data converters of the RF module.

The flash on the SDR prototype baseband module holds the configuration bit stream for the FPGA and the integrated compiled code for the soft core processors. During power-up a small CPLD bootloads the stored flash data into the FPGA. To initially load the data into the flash, the CPLD is jumper selectable during power-up to either read or verify blank/erase/program the flash. The SDR prototype baseband module can also load configuration data for the FPGA through the JTAG port.

7. SUMMARY

Software Defined Radio has become a reality for defense applications. Using the latest FPGA technology, implementation of SDR is now practical. FPGAs provide a design environment that allows for true architectural trade-offs to optimize power, and to tradeoff between firmware and software implementation of signal processing. Soft core processors provide new architectural approaches to parallelizing all signal processing within a single IC allowing high bandwidth implementations of adaptivity, and flexibility to accommodate waveform evolution throughout the product life, and to support product evolution beyond the product lifetime of ASIC based approaches. Cost trade-off between ASIC and FPGA shows initial cost of entry for ASIC are costly due to tools and resources. However, FPGA entry level cost is minimal in tool cost and the learning curve is short compared to the ASIC design approach. As a result very few designs achieve the production volume required to justify the expense of an ASIC, before the semiconductor industry overtakes the technology with new technology. However, in our architecture, we readily track the latest semiconductor technology, and thereby retain ultimate cost effectiveness.

8. REFERENCES

[1] Ray Andraka, "A Survey of CORDIC Algorithms for FPGA Based Computers," FPGA '98, Proceedings of the 1998 ACM/SIGDA Sixth International Symposium on Field Programmable Gate Arrays, Feb. 22-24, 1998, Monterey, CA. pp191-200

[2] Altera Corporation, "FIR Compiler User Guide v2.7.0", www.altera.com

[3] Altera Corporation, "NCO Compiler User Guide v2.0.5", www.altera.com

[4] Altera Corporation, "FFT Compiler User Guide v2.0.0", www.altera.com

[5] Altera Corporation, "Viterbi Compiler User Guide v4.0.0", www.altera.com