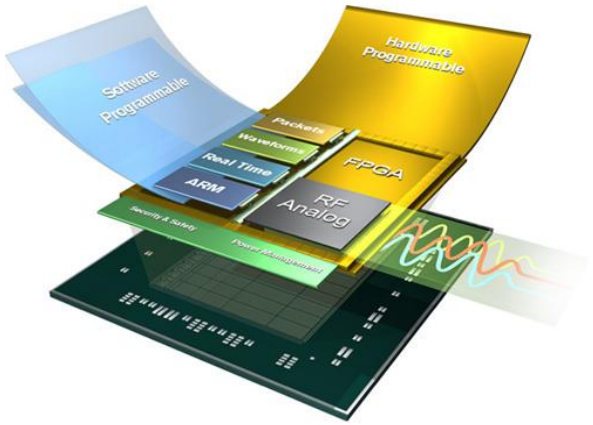
PENTEK

Strategies for Deploying RFSoC Technology for SIGINT, DRFM and Radar Applications

Rodger Hosking
Pentek, Inc.

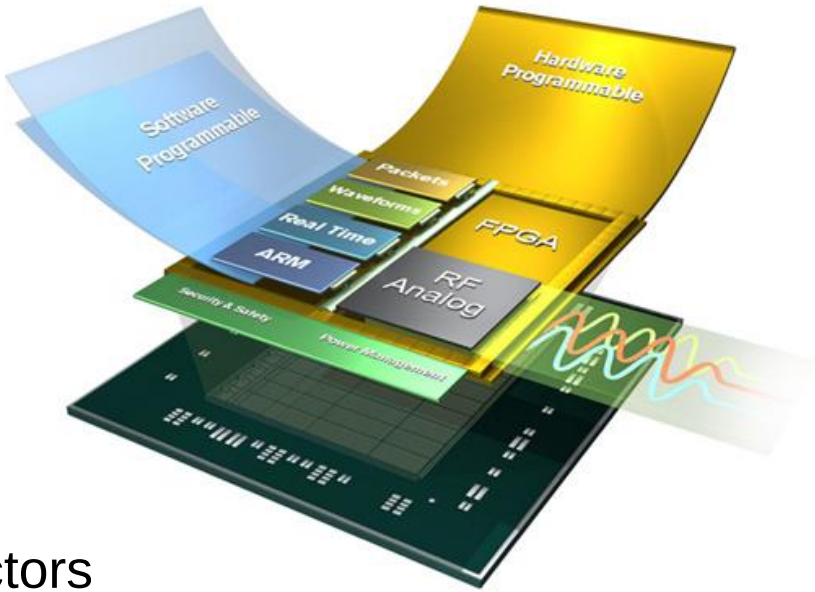


WInnForum Webinar
November 8, 2018

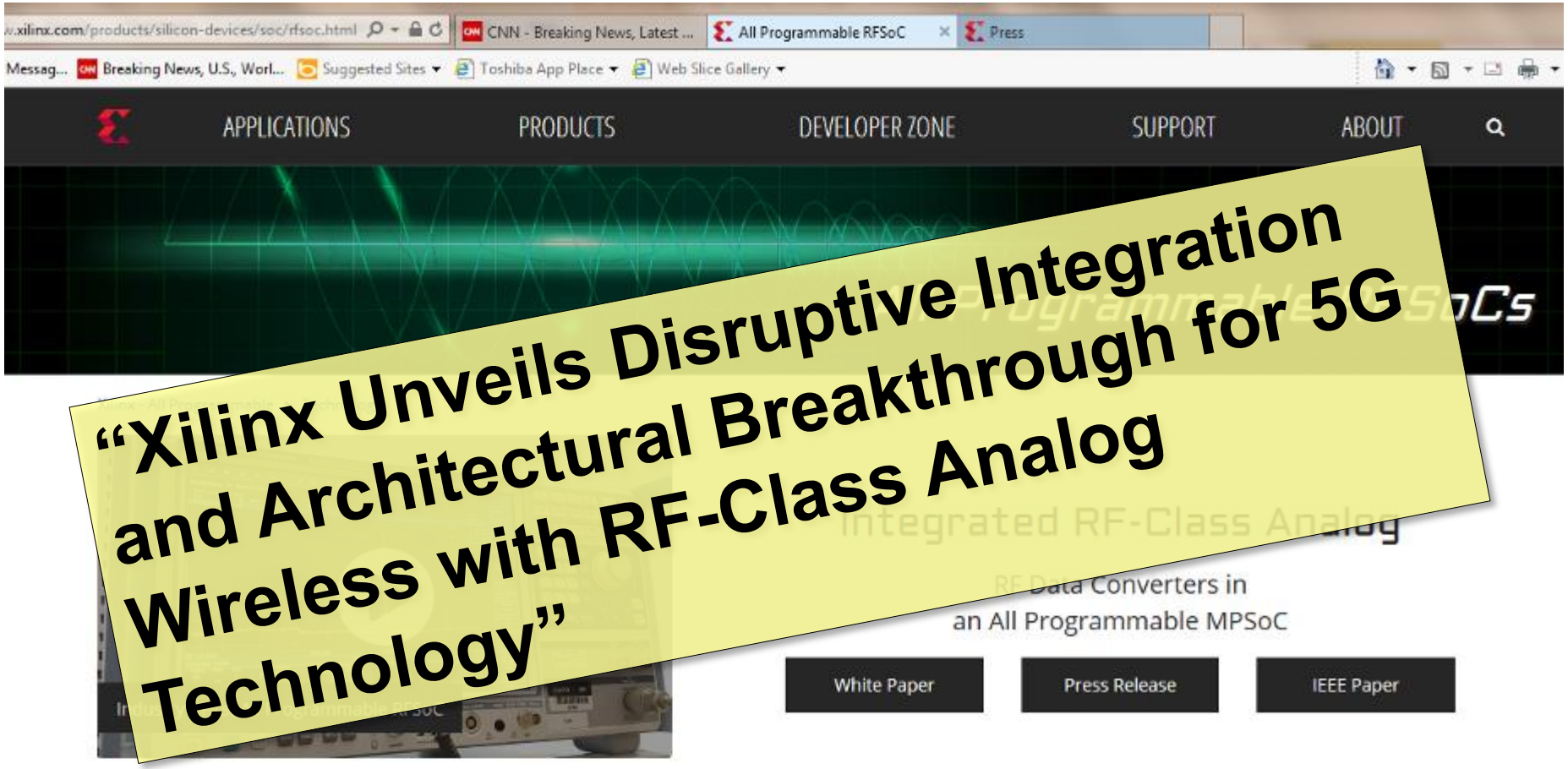
30 YEARS

Topics

- Xilinx RFSoC Overview
- Impact of Latency on Applications
- RFSoC Market Opportunities
- RFSoC Design Challenges
- RFSoC Module Concept: QuartzXM
- Development Platforms for QuartzXM
- QuartzXM Migrates to Other Form Factors
- FPGA IP Development Strategies
- ARM Software Development Strategies
- Summary



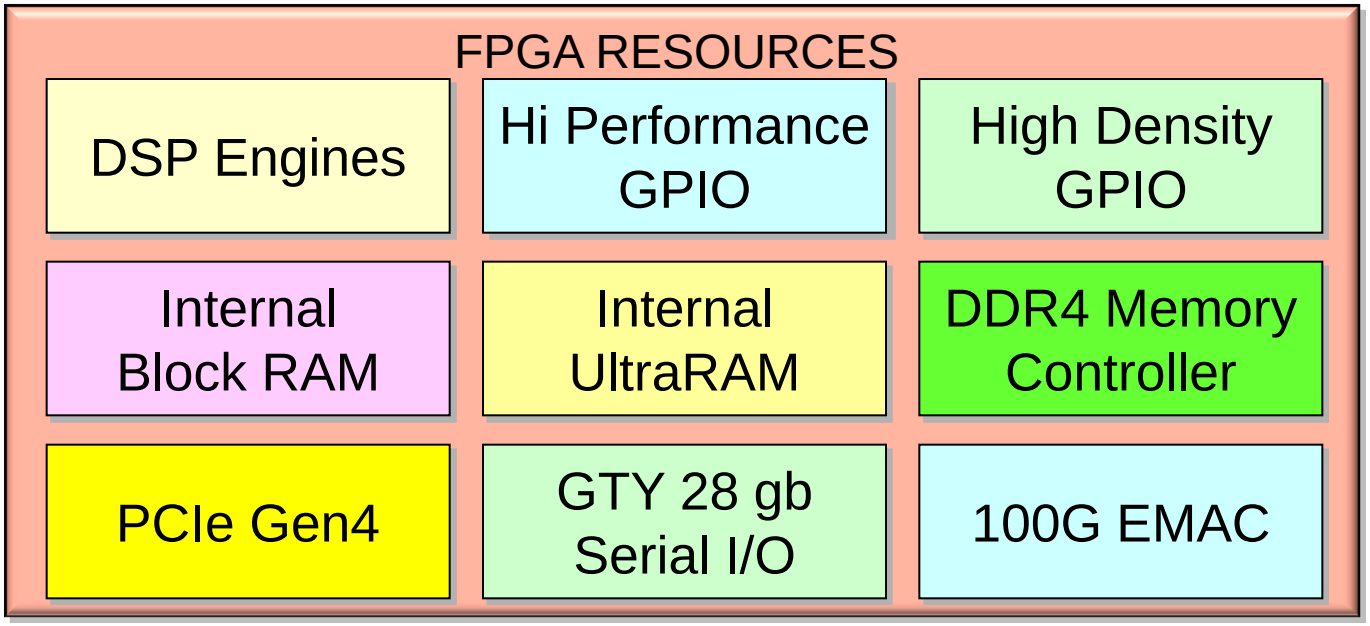
February 2017: Xilinx Announced RFSoC



"Xilinx Unveils Disruptive Integration and Architectural Breakthrough for 5G Wireless with RF-Class Analog Technology"

Xilinx UltraScale+ FPGA Resources

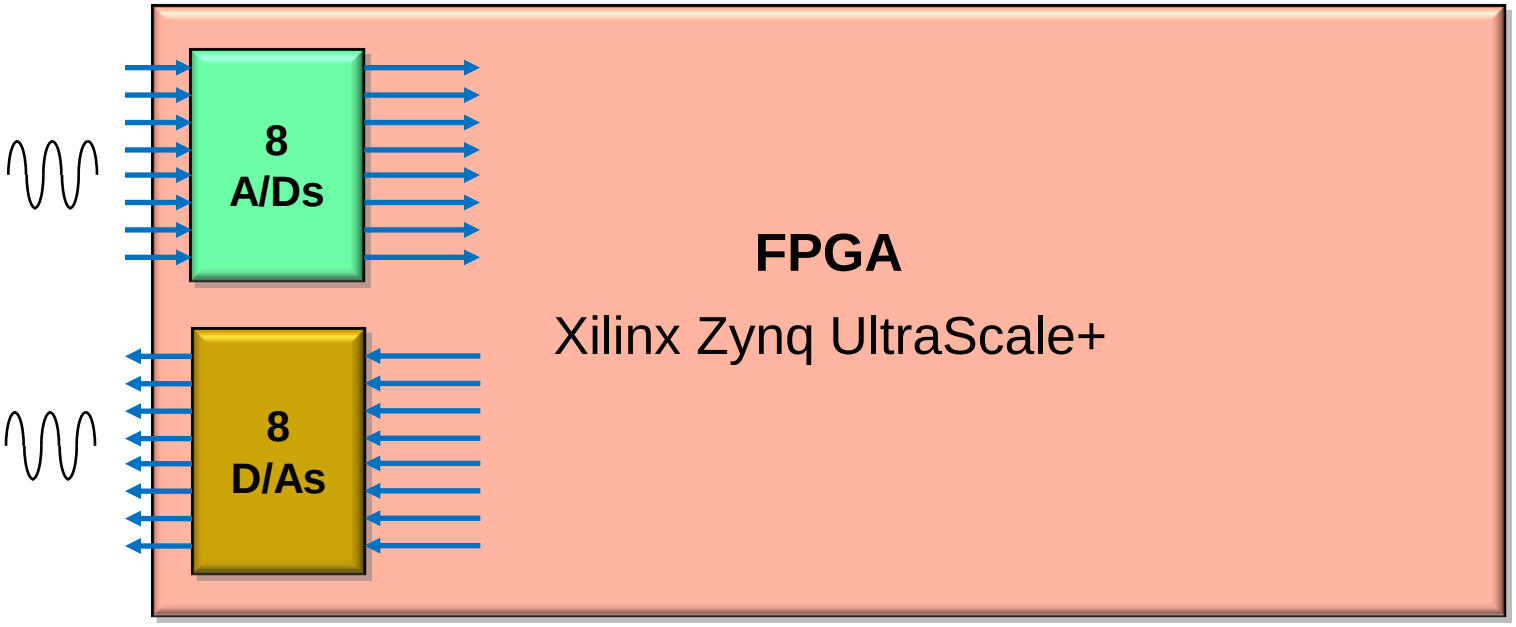
- 16 nm FPGA Fabric – Logic Cells, DSP Engines, Block RAM, etc.
- Advanced Real-Time Digital Signal Processing Engines
- Extensive General Purpose I/O for Peripherals



- Fast Internal Memory and Controller for External DDR4
- PCIe Gen4 System Interface
- Enhanced 28 gb GTY Serial I/O and MAC for 100 GbE

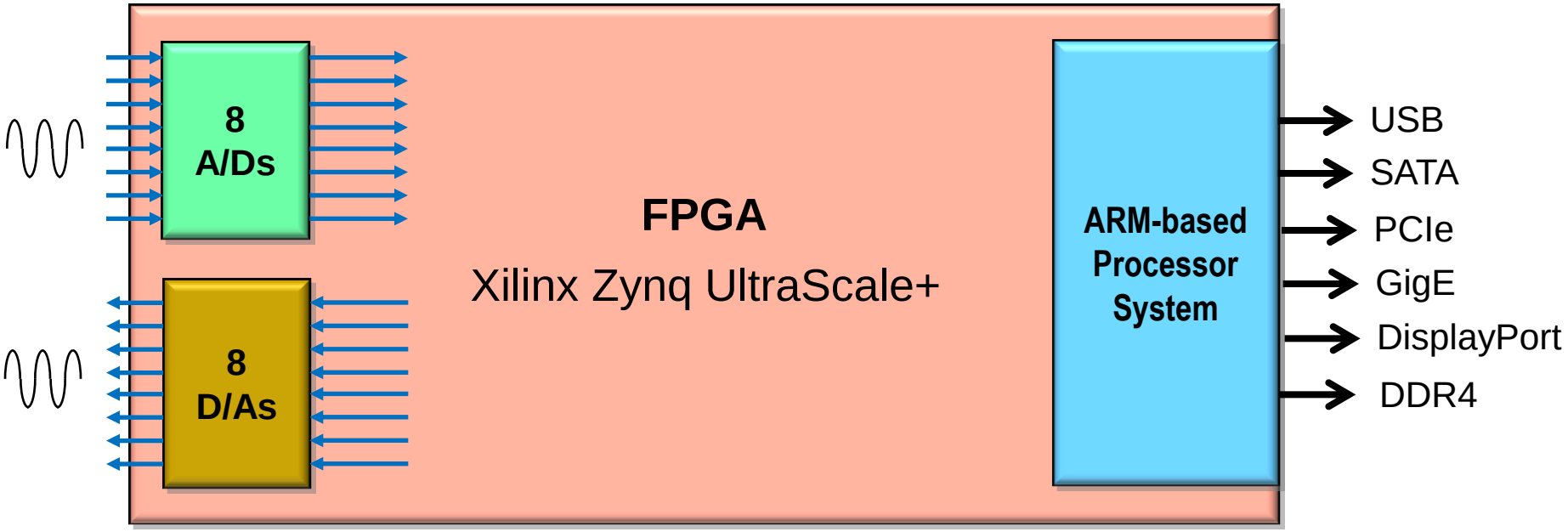
Integrated Data Converters in the FPGA

- A/Ds and D/As are connected directly to FPGA fabric
- Lowest latency parallel interfaces



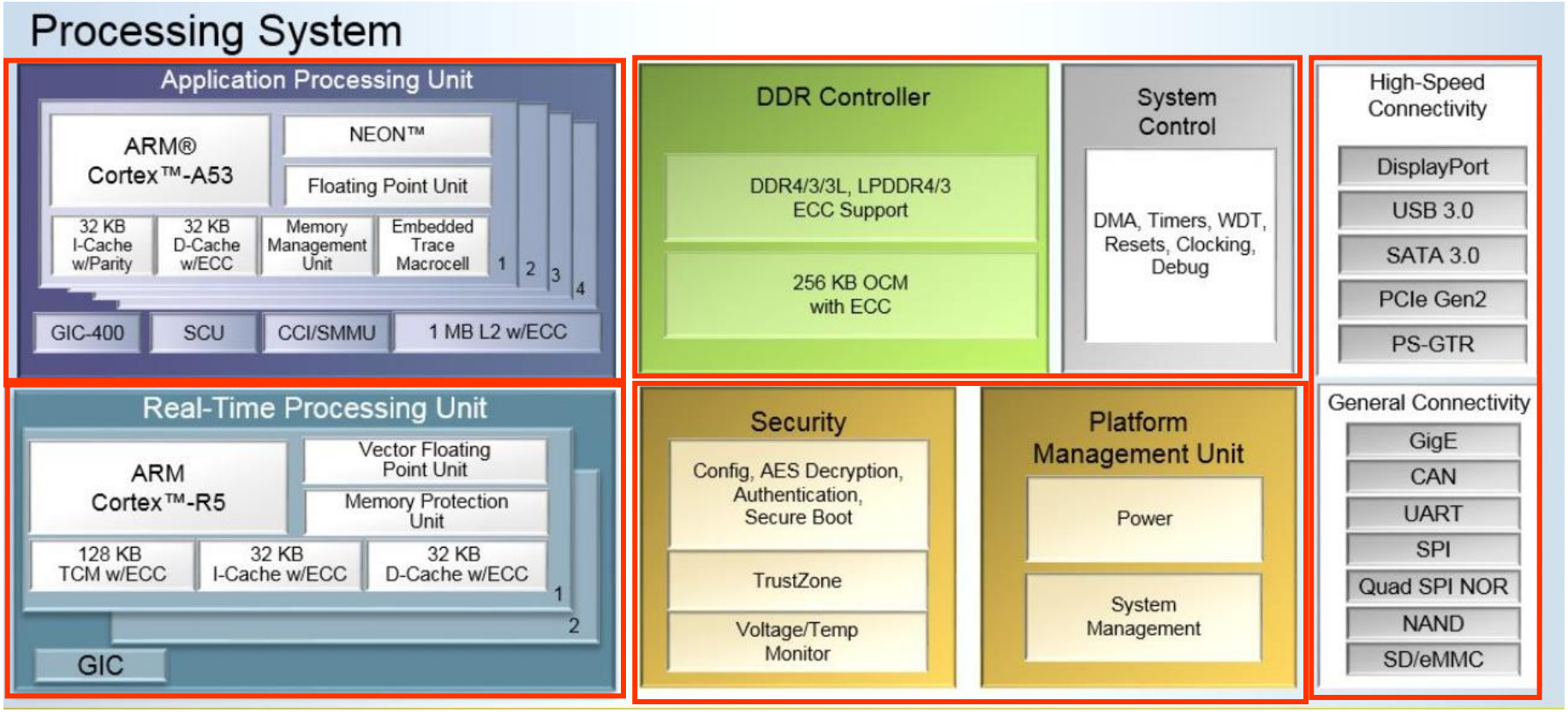
- 8 A/Ds: 12-bit, 4 GHz with integrated Digital Downconverters
- 8 D/As: 14-bit, 6.4 GHz with integrated Digital Upconverters

ARM Processor Resources



ARM Based Processor System

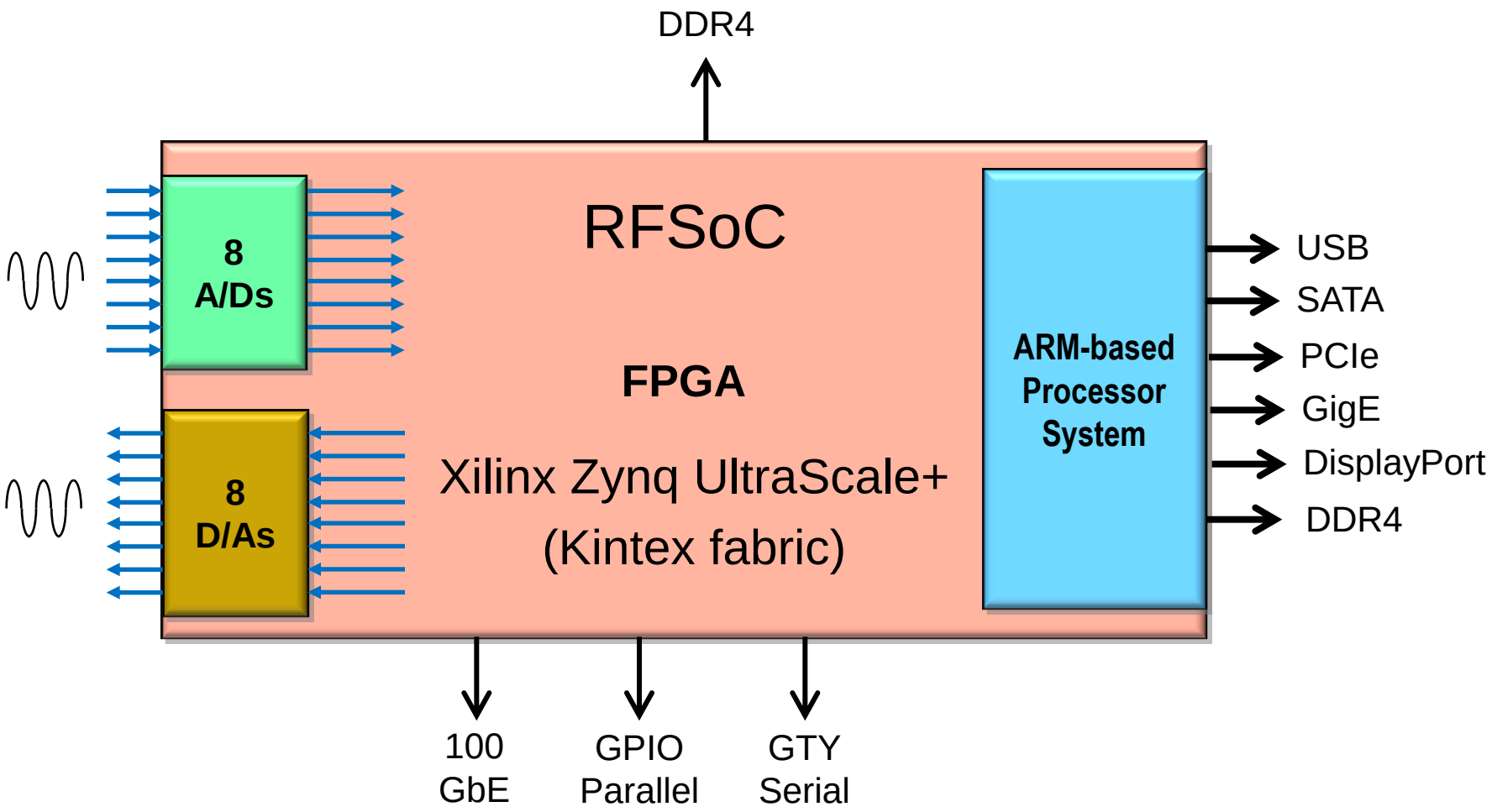
- Application Processor: Four 64-bit ARM Cortex-A53 cores
- Real-Time Processor: Two ARM Cortex-R5 real time cores



- DDR4 Memory Controller and System Controller
- Security Manager and Platform Management Unit
- High-Speed Connectivity and Processor I/O

RFSoC – Complete RF System on Chip

- Complete sub-system on a single monolithic chip!



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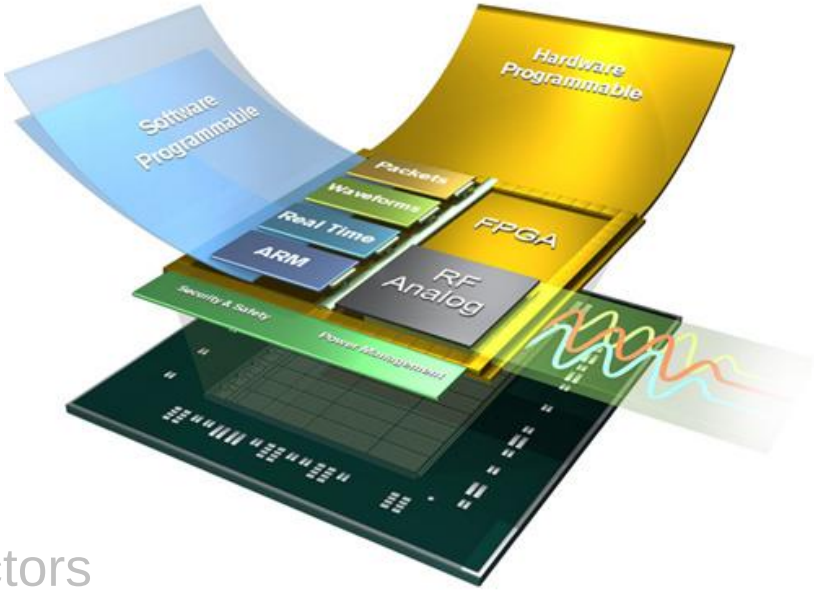
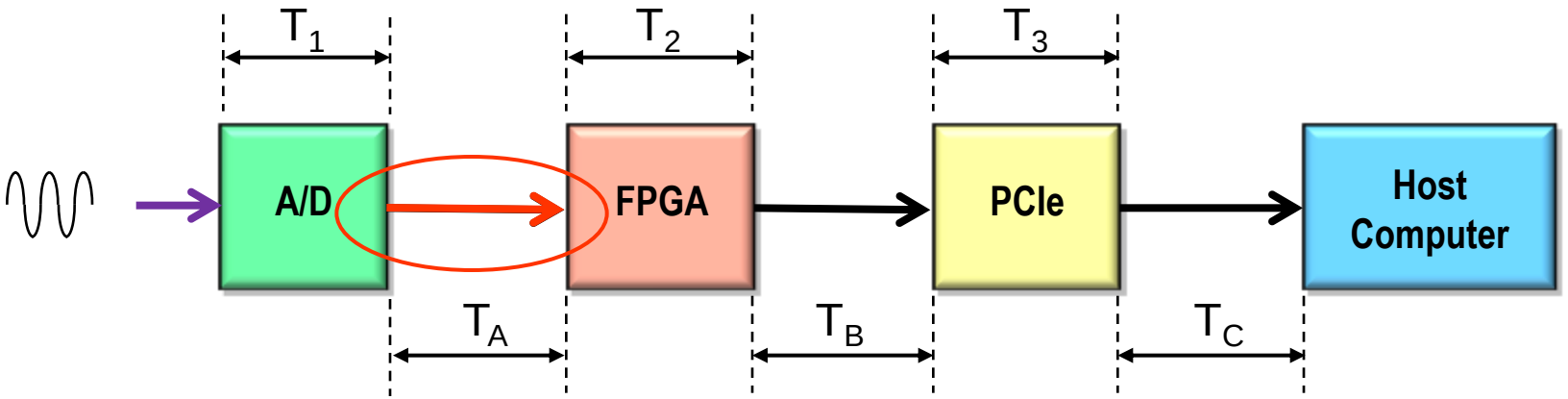
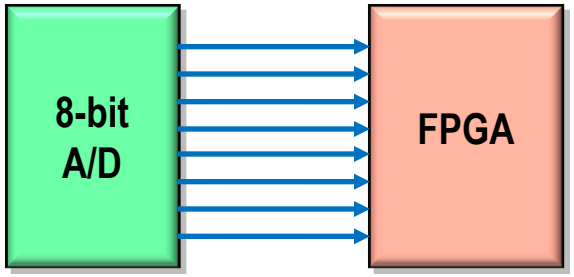


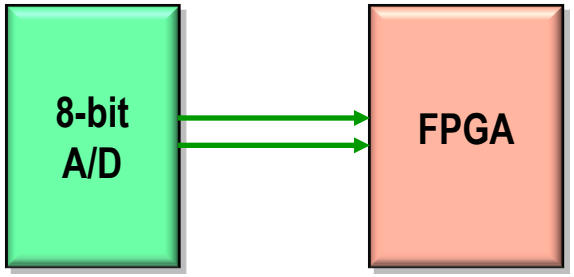
What Is Latency?

- Time delay through the system from input to output
- Includes delays within each element
- Includes delays in the links between each element
- Data converter links are becoming a critical limiting factor!



Parallel vs. Serial Converter Interfaces





Parallel connection (LVDS)

Pro
- Simple
- Low latency

Con
- Limited speed
- Many lines to route on PCB

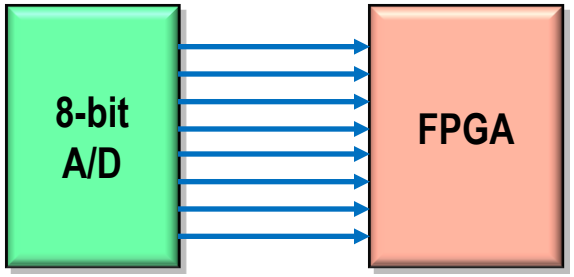
Serial connection (JESD204B)

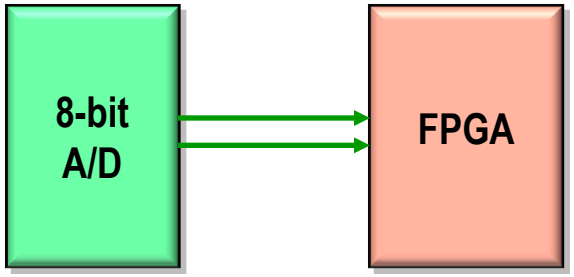
Pro
- Can handle high speed A/Ds
- Fewer lines to route on PCB

Con
- Serial protocol introduces latency
- Complex to implement

- The latest and fastest discrete data converters use JESD204B

RFSoC – The Best of Both





Parallel connection (LVDS)

Pro

- Simple
- Low latency

Con

- ~~Limited speed~~
- ~~Many lines to route on PCB~~

Serial connection (JESD204B)

Pro

- Can handle high speed A/Ds
- Fewer lines to route on PCB

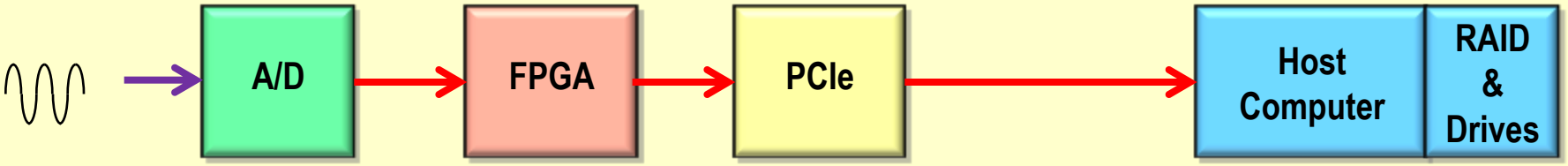
Con

- ~~Complex to implement~~
- ~~Serial protocol introduces latency~~

- RFSoc Uses Internal Parallel Data Converter Interfaces
  - Simplest Interface and Low Latency
  - Internal connections handle high data rates
  - Internal connections reduce PCB trace count
- Eliminates All the Cons!

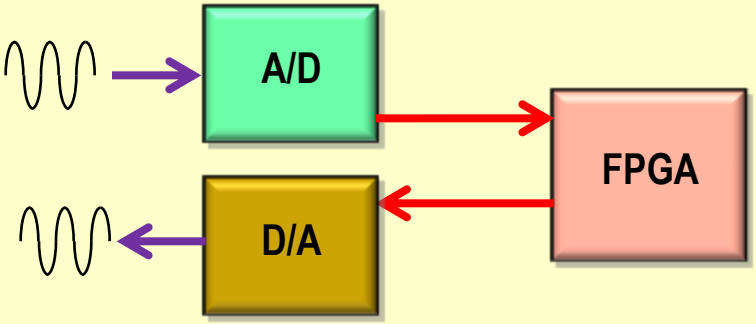
Applications and Data Transfer Latency

Application not affected by latency - Recording



Latency introduced by JESD204B not a problem

Application affected by latency – Countermeasures



Latency introduced by JESD204B is a big problem!

- RFSoC Covers Applications for ALL Latency Requirements!

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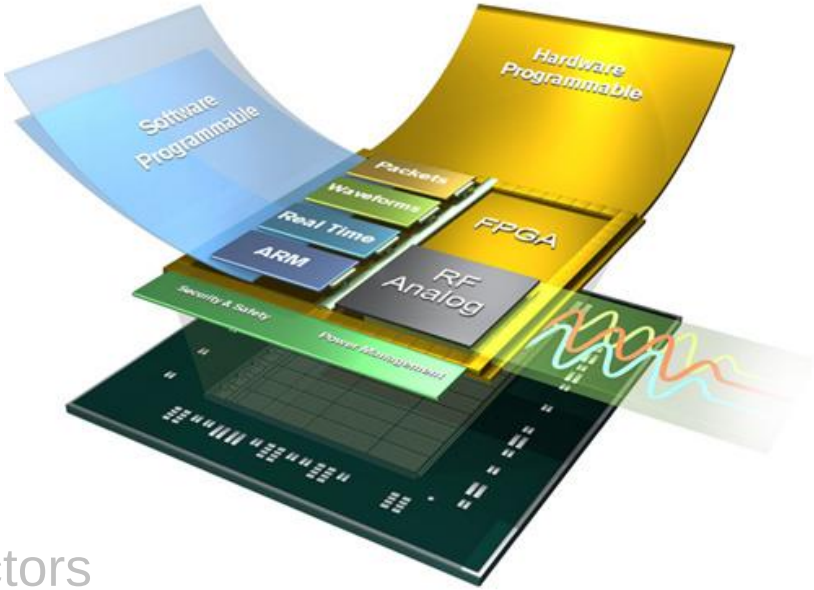
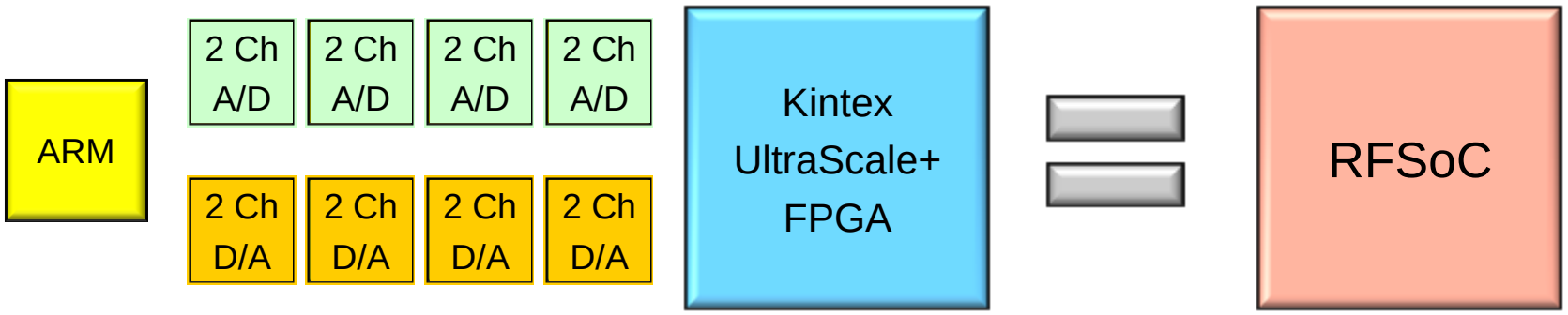


RFSoC Market Opportunities

- Radar
  - Multi-function Phased Array Radar (MPAR) initiative combines U.S. weather and radar networks
  - Common Module beamformer for DARPA Arrays Commercial Time Scales (ACT) program
- EW and Countermeasures
  - Low latency DRFM applications
- Communications
  - SATCOM and Military / Airborne Radios
- SIGINT
  - Monitoring, Interception, and Analysis
- 5G Wireless & Cable Remote PHY
  - Remote radio head for Massive-MIMO, wireless backhaul, and fixed wireless access
  - Implements DOCSIS 3.x PHY Spectral Efficiency requirements for distributed broadband digital networks

How Does RFSoC Change the Market?

- Reduced size and footprint
  - About 50% less compared with discrete data converters, FPGA & processor
- Reduced power
  - About 30-40% total power savings
- Reduced cost
  - About 40-60% total cost savings
- Reduced latency
  - About 80-90% less delay than JESD204 data converters



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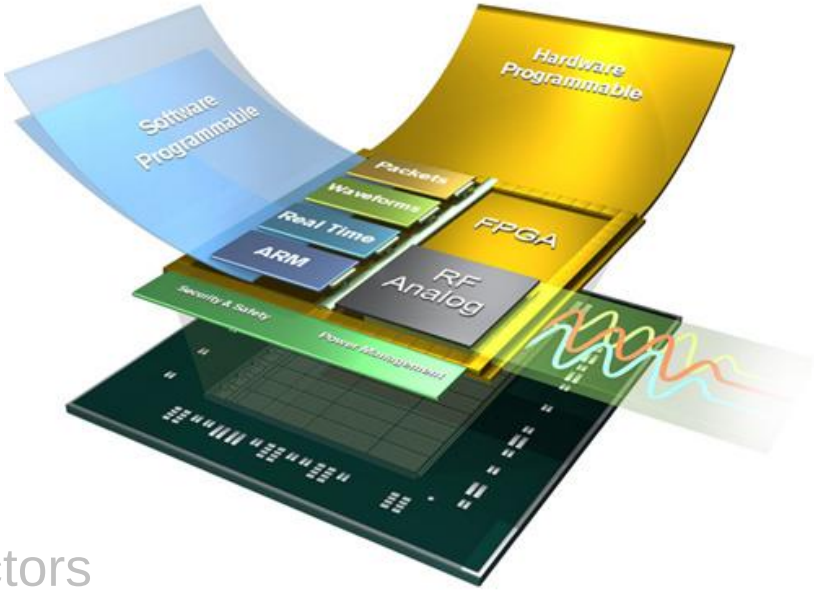
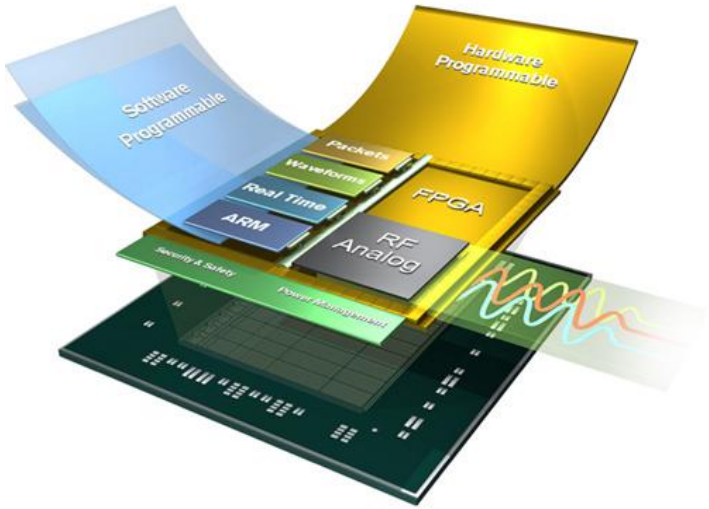


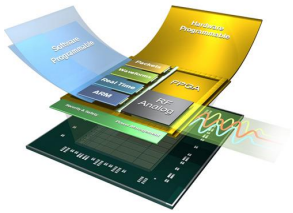
RFSoC: Board Level Design Issues

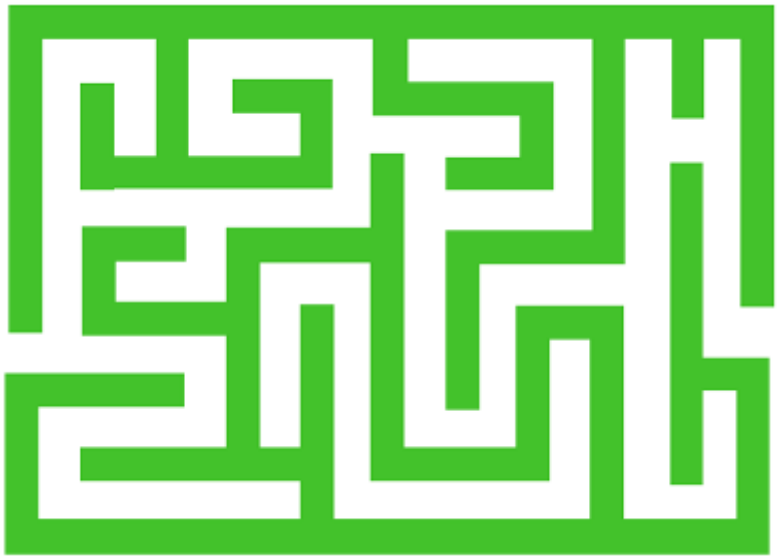
- RF Signal Integrity
  - 16 Analog RF Signals with GHz Bandwidths
  - Spurious digital signal pickup
  - Crosstalk between analog channels
  - Signal path integrity and impedance
- Gigabit Serial Links – 28 Gbit GTY
  - Signal path integrity and impedance
  - Bit error rate considerations
- Clock Management
  - Data Converter Sample Clocks
  - FPGA Fabric and Gigabit Serial Links
- Power Supply Requirements
  - RFSoC chip requires 13 different power supplies
  - Analog supplies must be extremely clean
- Thermal Management
  - Air- or conduction-cooling provisions



Design Strategies for RFSoC

- What the shortest path from RFSoC chip to Deployed Product?
  - Hardware Strategies
  - FPGA Design Strategies
  - ARM Processor Software Development
- How can I get a running start?





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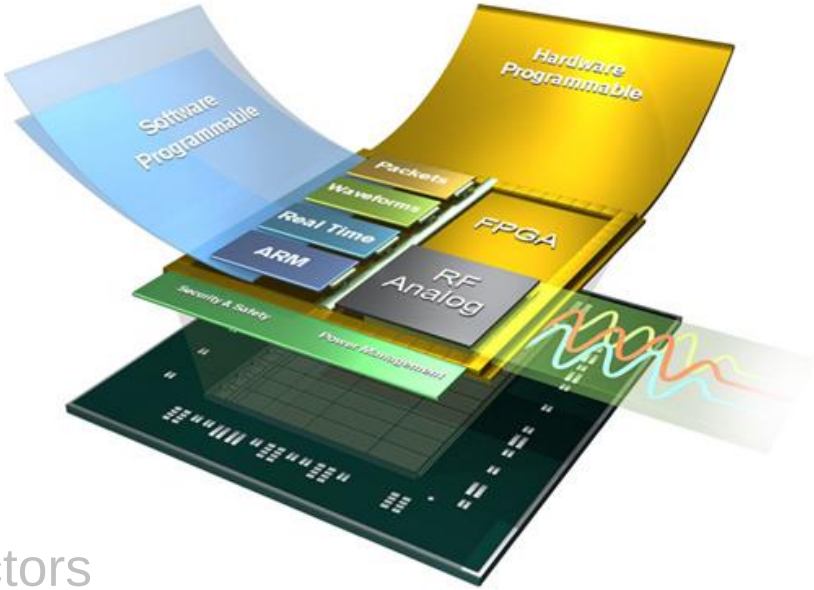
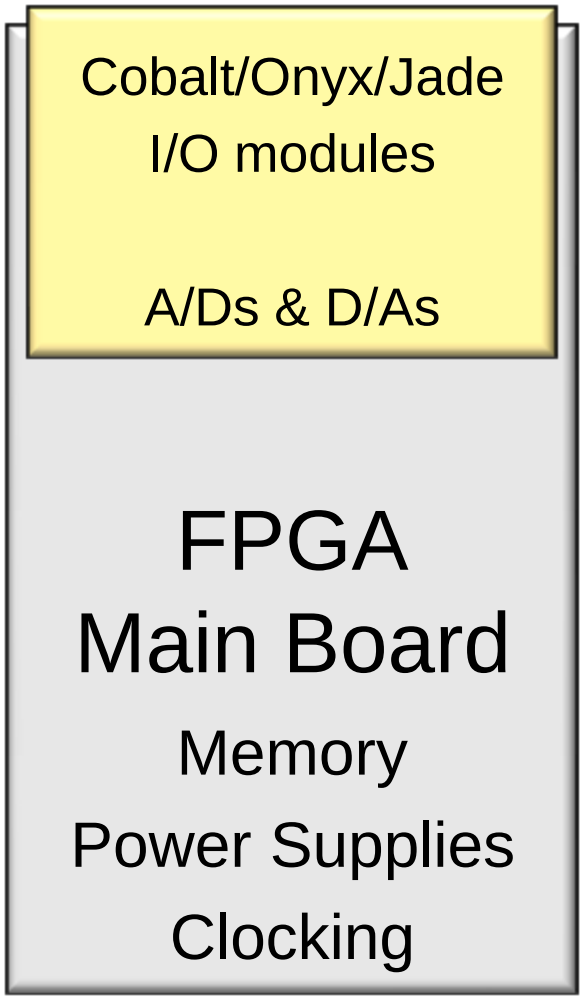
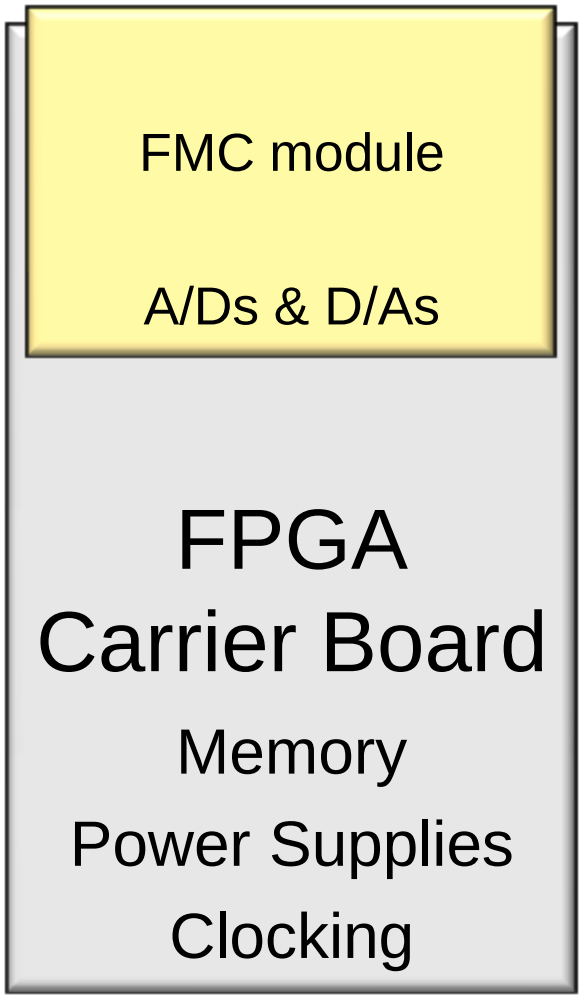


Traditional Modular Designs

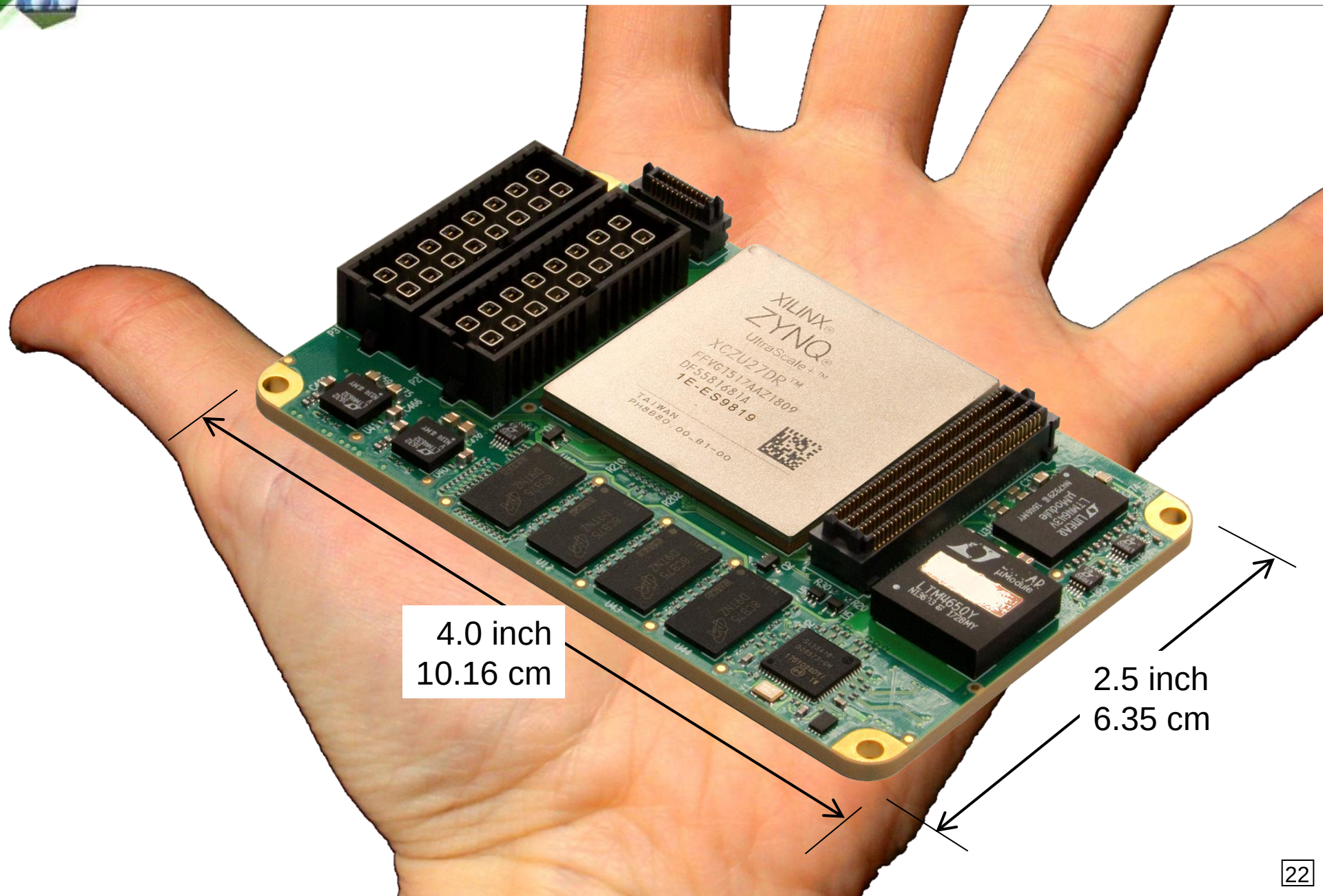


XMC Products



FMC Products

QuartzXM: RFSoC e**X**press **M**odule



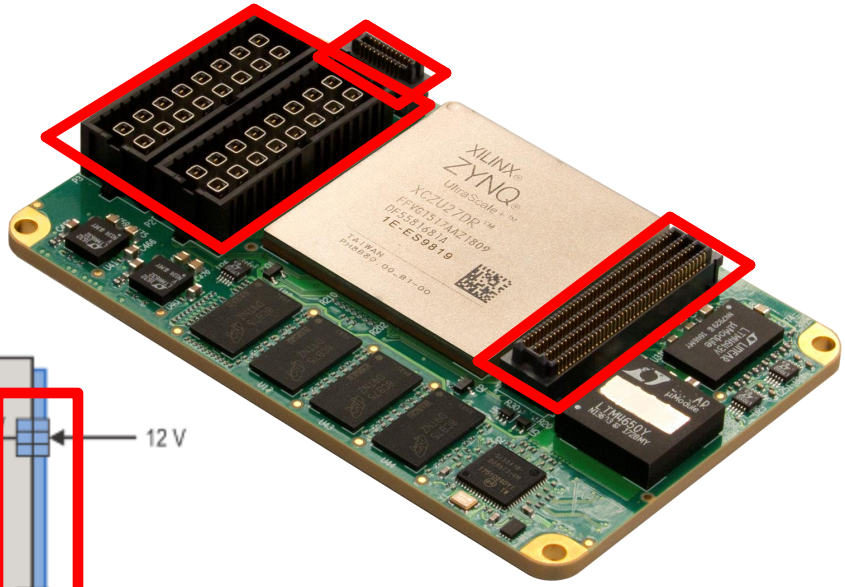
Benefits of the QuartzXM eXpress Module

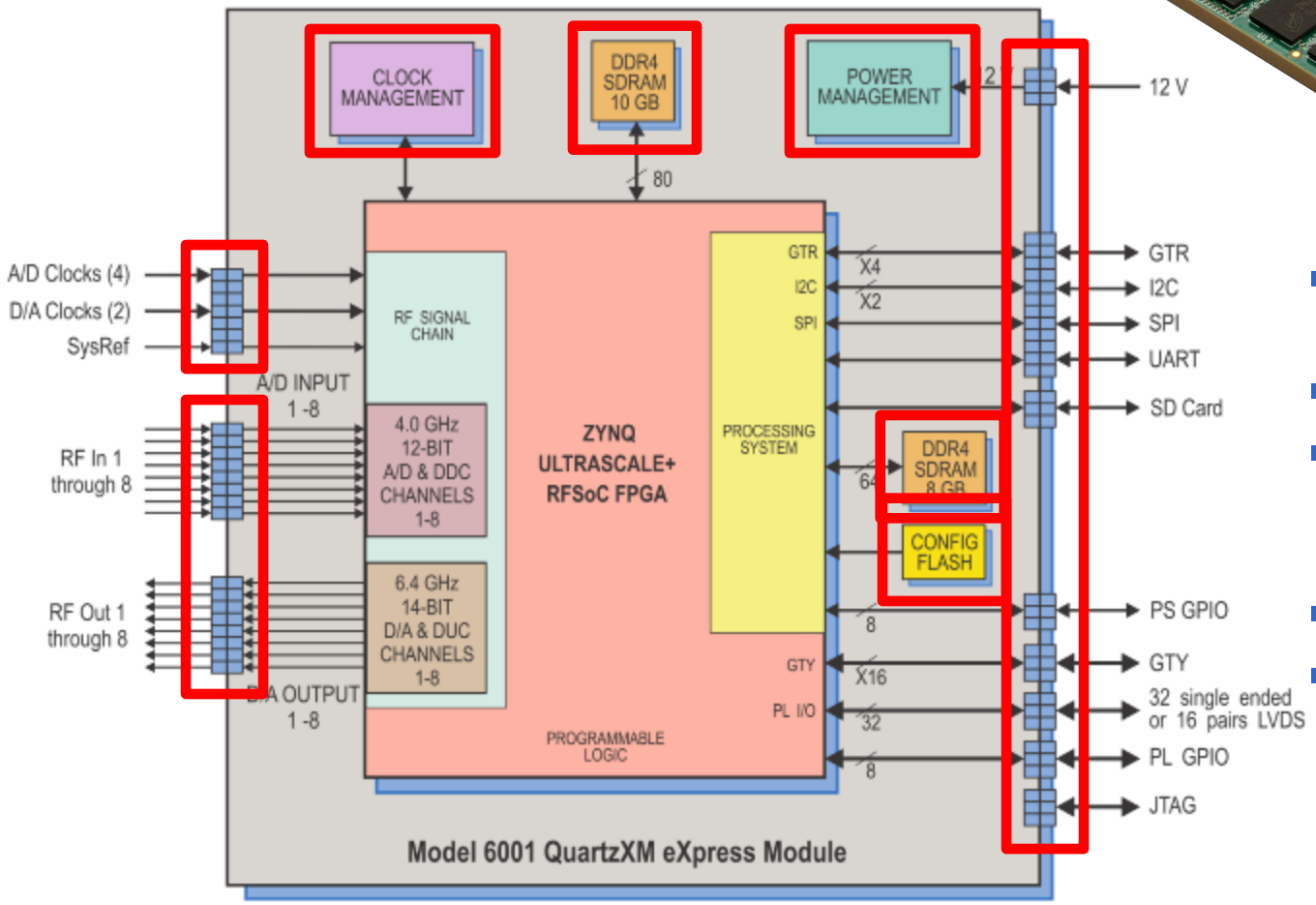
- Mezzanine module simplifies and speeds RFSoC product designs
- Connectorizes & preserves integrity of RF and gigabit serial signals
- Generates all 13 RFSoC power supplies from a single +12V input
- Includes FLASH and DDR4 memories for FPGA & ARM processor
- Maintains PCB constraints for bypassing, filtering, & geometries
- Includes clock management and health monitoring facilities
- Excellent path for addressing SWaP requirements

- Some technical details:
  - 28 layer PCB
  - Over 4000 drilled holes
  - Uses advanced PCB fabrication techniques including: *sequential lamination, backdrilling, blind and buried vias, etc.*
  - Supports 28Gbps GTY serial interfaces

Model 6001 – QuartzXM eXpress Module

- Contains all the infrastructure circuitry to support the RFSoC





- Power supplies and power management
- Clock management
- DDR4 SDRAM for both the FPGA fabric and processors
- Configuration FLASH
- Connectors for bringing ALL RFSoC signals to a carrier board

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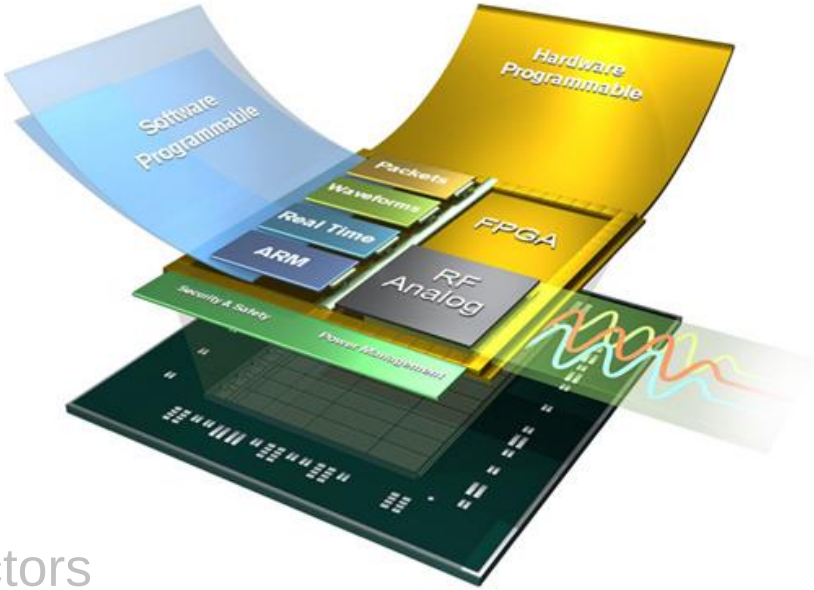


VPX Standards for Embedded Systems

- VITA 66.x Optical Backplane I/O
  - Several full- and half- width blind-mate optical connector types
  - Provides high bandwidth data paths between boards and chassis

Photo: Elma

- VITA 67.x Coax Backplane I/O
  - Several multi-position connector types – up to 12 coax signals
  - RF signal band-widths to 40 GHz
  - Eliminates front panel signal cables

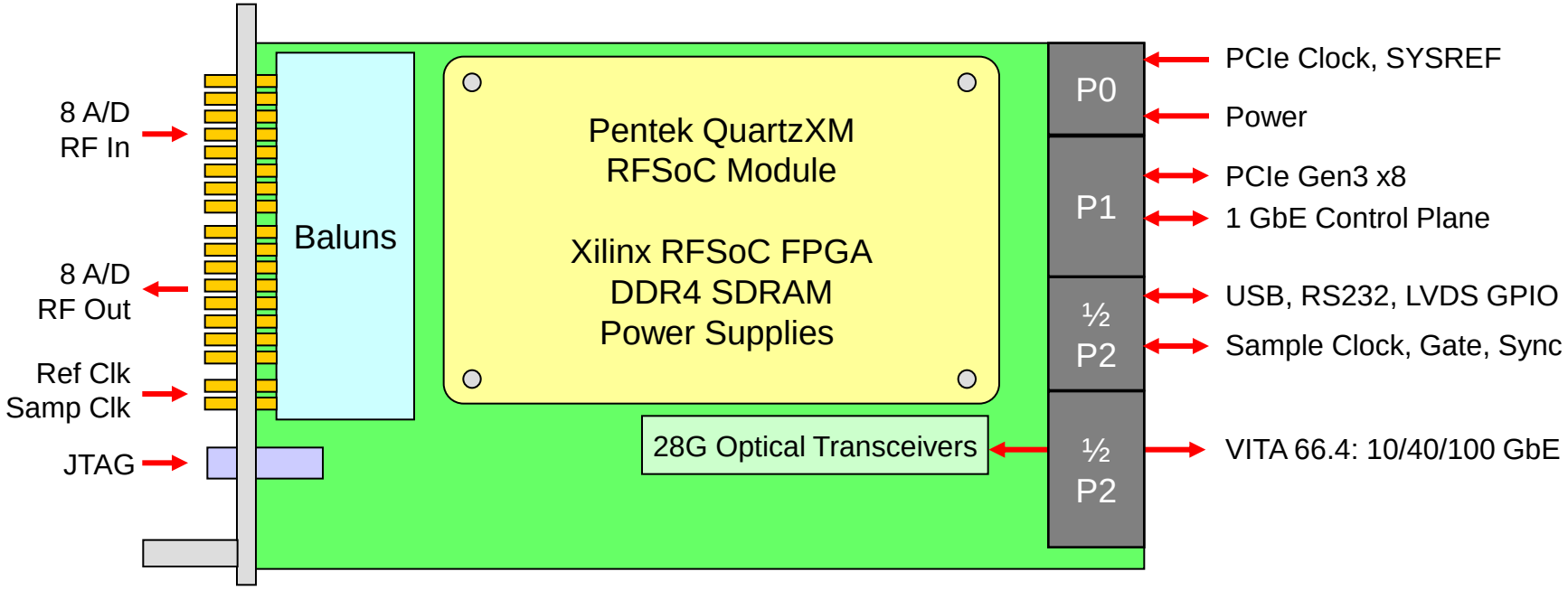
Photo: SV Microwave

- VITA 65.0 & 65.1 OpenVPX - 2017
  - Most popular MIL-AERO standard for deployed systems
  - Major enhancements reflect widespread use and adoption of OpenVPX
  - New Card, Slot and Backplane Profiles
  - Radial Backplane Clock distribution ensures precision timing and synchronization across boards
  - Provision for a 100 MHz reference clock
  - New definitions of combinations of VITA 66.x optical and VITA 67.x coaxial backplane I/O

Photo: TE Connectivity

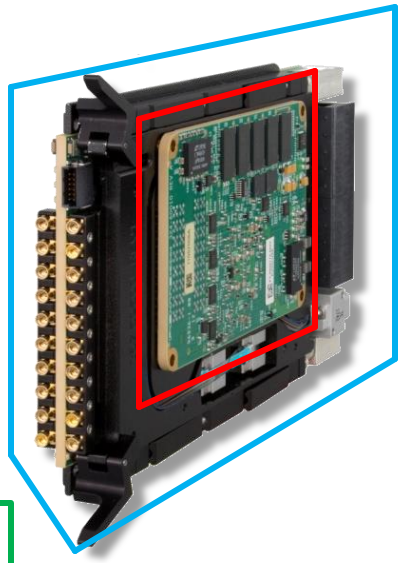
QuartzXM on 3U VPX – Front Analog I/O

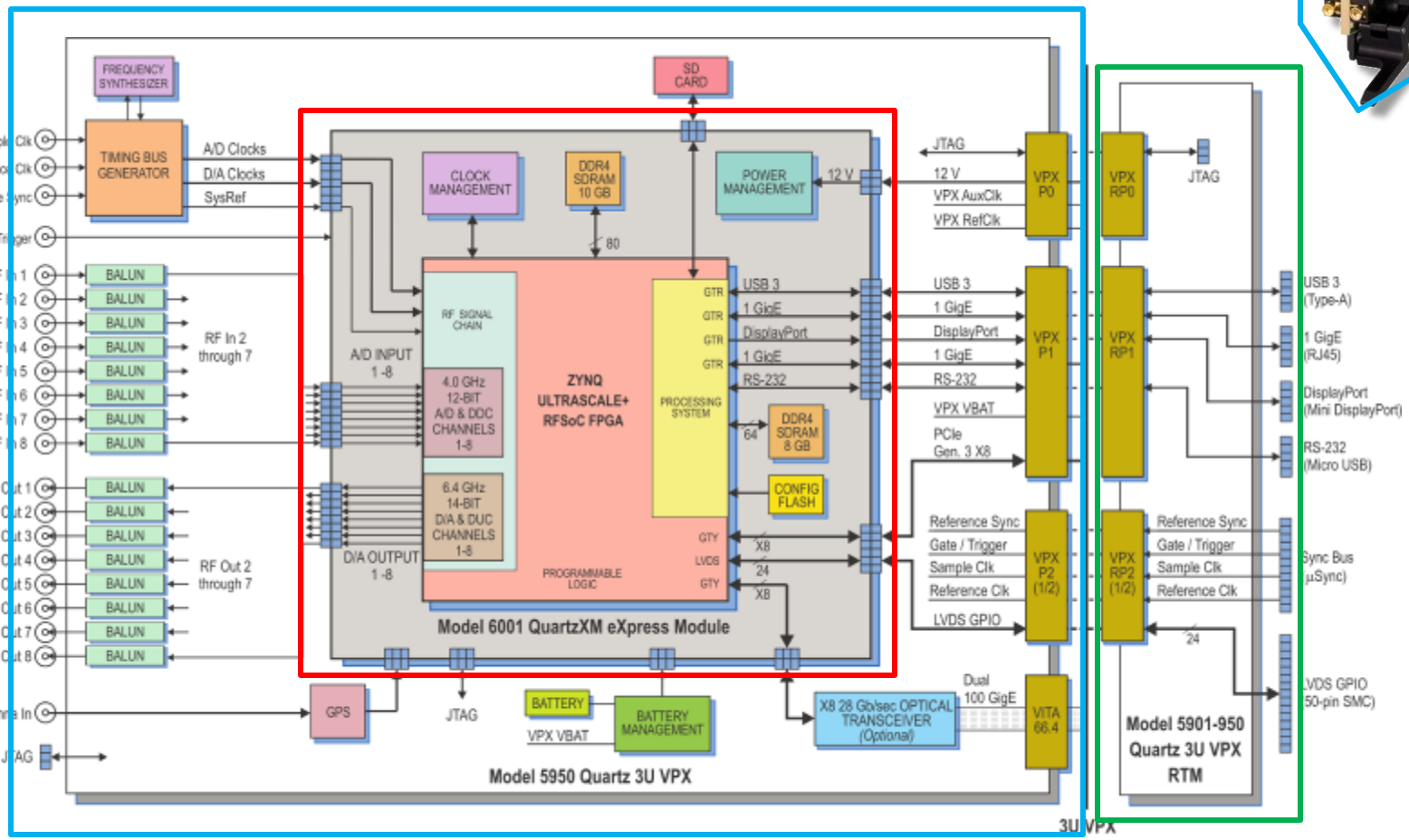
- Model 5950 3U VPX Carrier for QuartzXM
- Open Architecture Form Factor Supporting Industry Standards
  - VITA 65.1 OpenVPX
  - VITA 66.4 Optical Serial Backplane I/O
- Complete functional sub-system on one 3U VPX module
- Scales easily to support high-channel count systems
- Synchronization across multiple modules

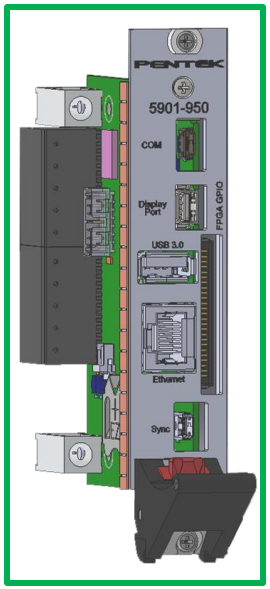


Model 5950 Quartz 3U VPX

- 3U VPX Carrier provides Coaxial RF Front Panel I/O
- Rear Transition Module provides ARM processor I/O
- Air- and Conduction-cooled Versions

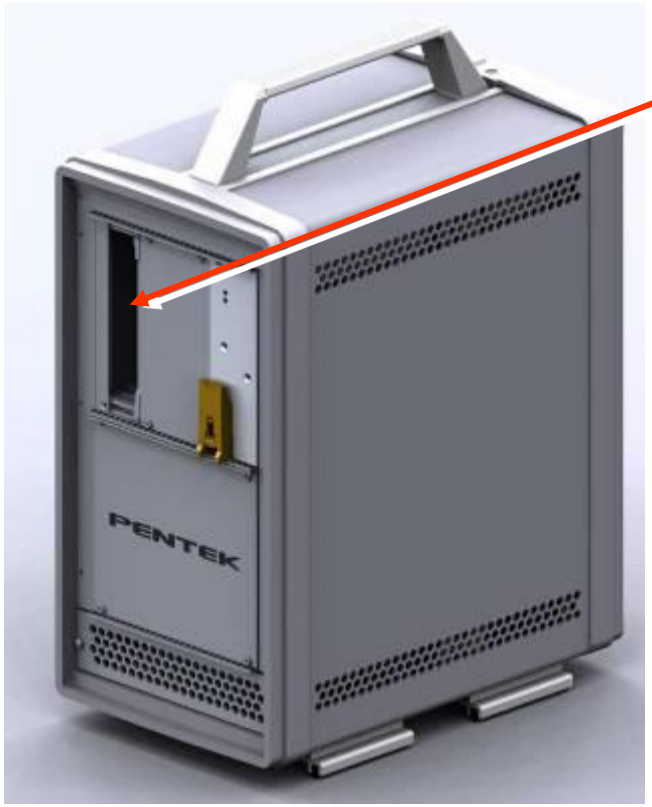






3U VPX Single Slot Development Chassis

- Low-cost chassis includes backplane, power supply, & cooling
- Model 5950 3U VPX RFSoC installed & tested
- Model 5901 Rear-Transition Module installed & tested
- Optional MTP Optical connector for dual 100GbE

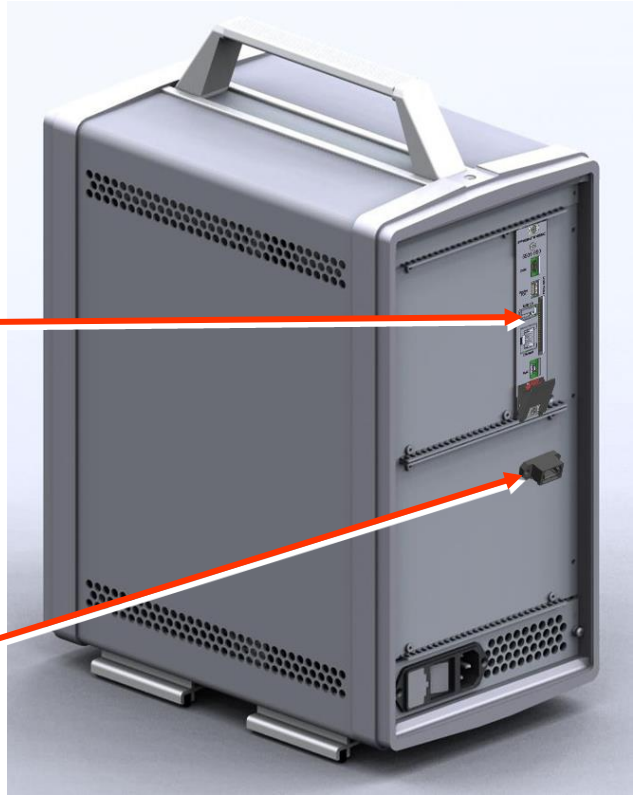


Front

Model 5950 3U VPX Front Panel (RF I/O, clocks, timing, etc.)

Model 5901 Rear Transition Module (ARM Processor I/O, FPGA LVDS I/O)

MTP Optical I/O (Dual 100 GbE)



Rear

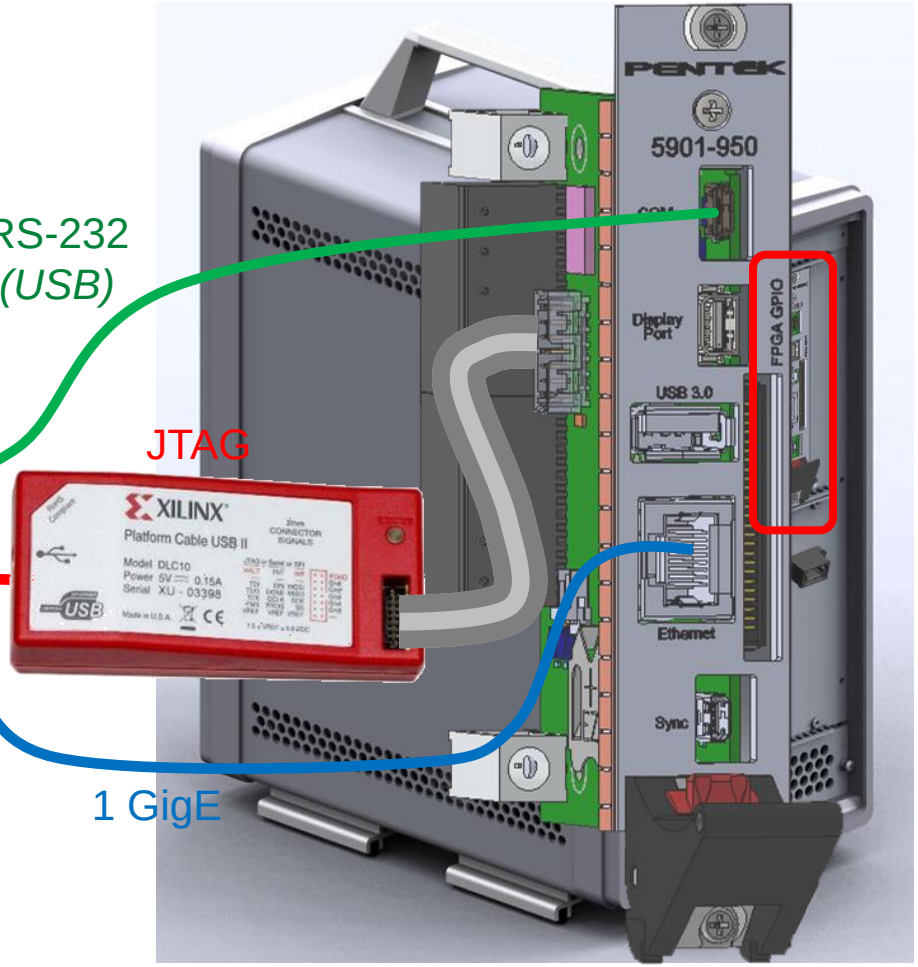
Single Slot Development Chassis Strategies

Customer's PC

RS-232
(USB)

JTAG

1 GigE



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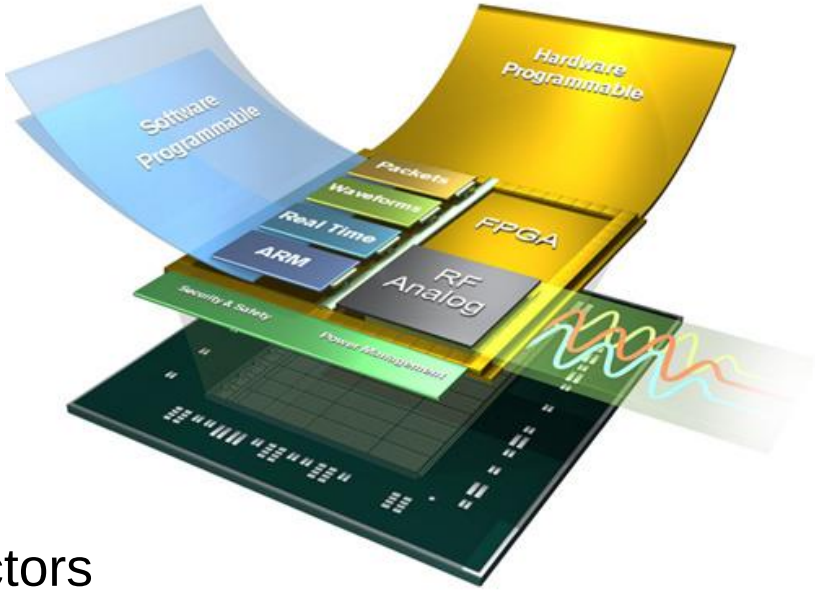
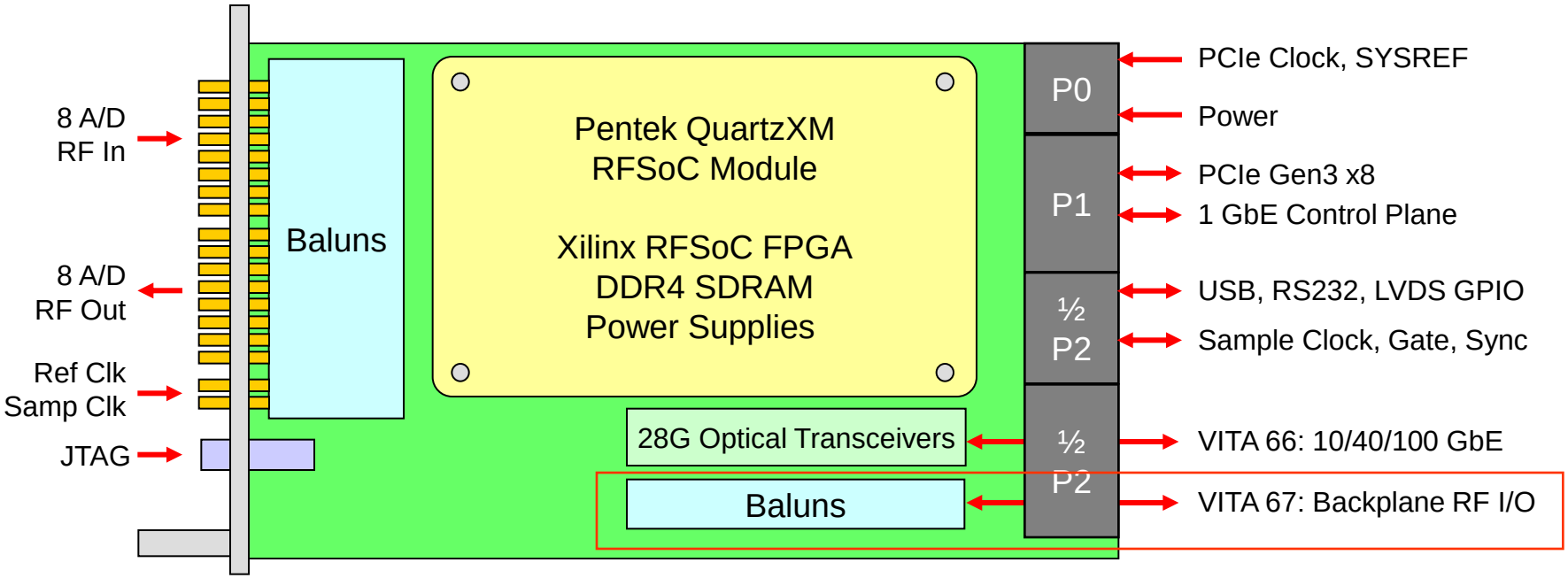


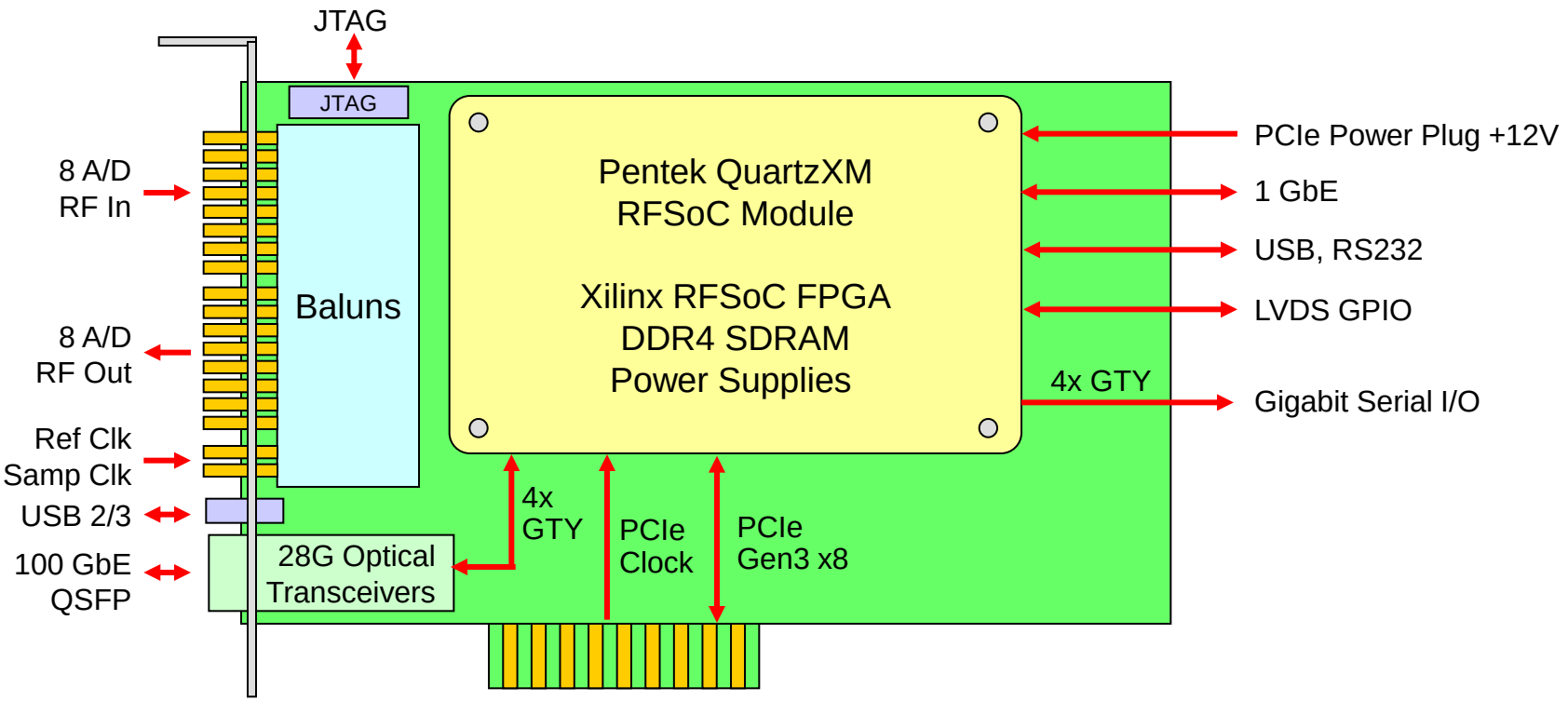
QuartzXM for 3U VPX – Backplane RF I/O

- Similar to Model 5950 except analog RF I/O connects through backplane
- VITA 67 defines several possible RF backplane connector formats
- Simplifies system integration and maintenance tasks
- Improves reliability by eliminating cables



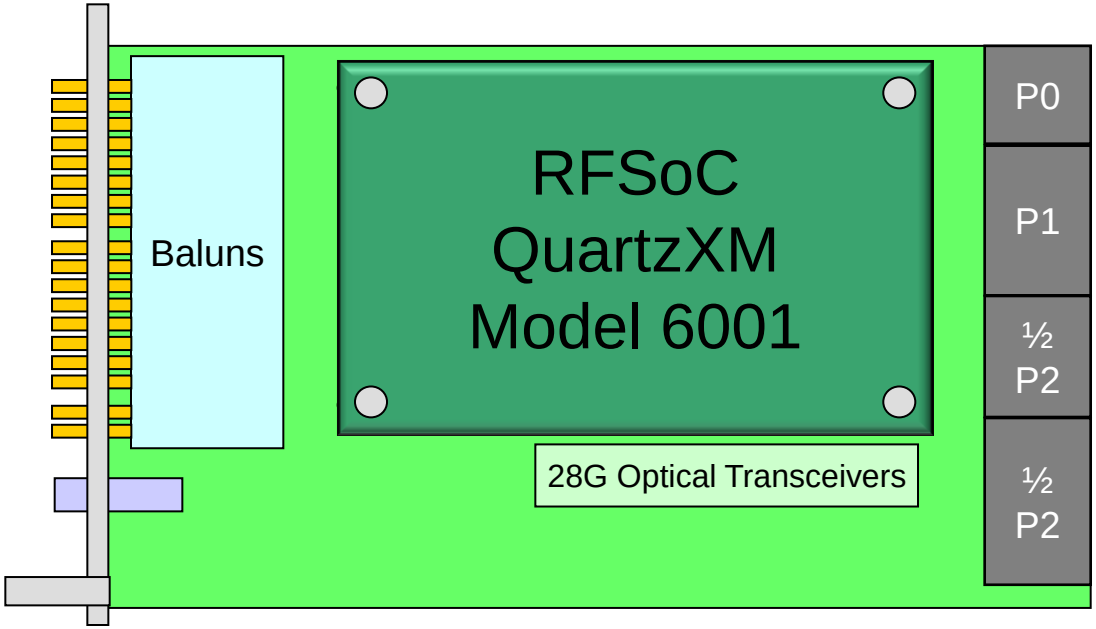
QuartzXM on PCIe Carrier for PC Platform

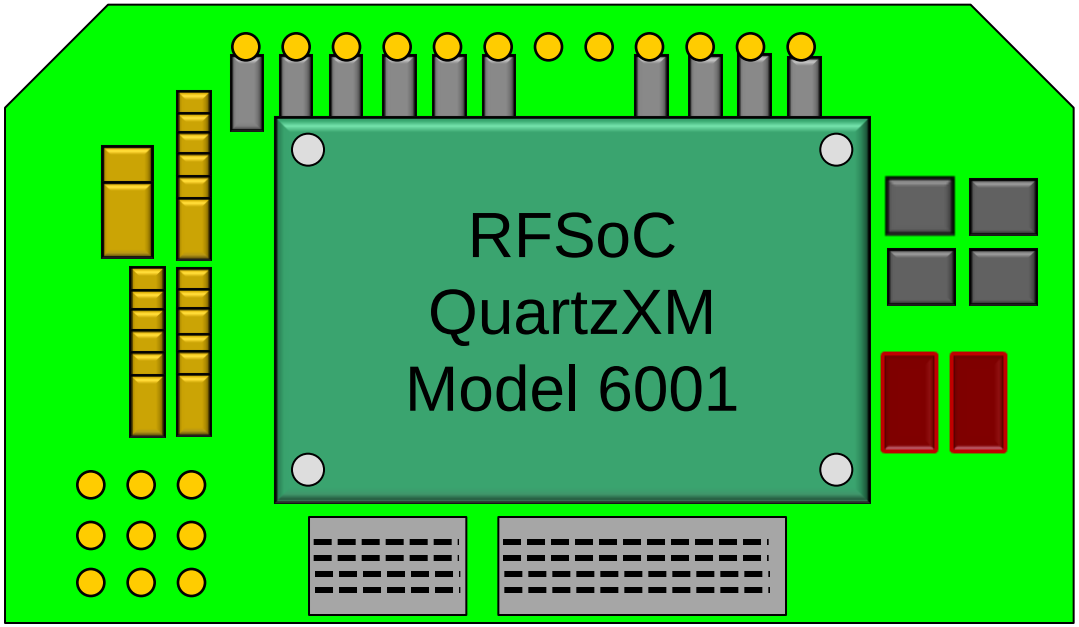
- Allows RFSoC development tasks in a low cost PC platform
- Perfect for software and FGPA development seats
- Perfect for continuation engineering and support
- Supports deployed applications for benign environments



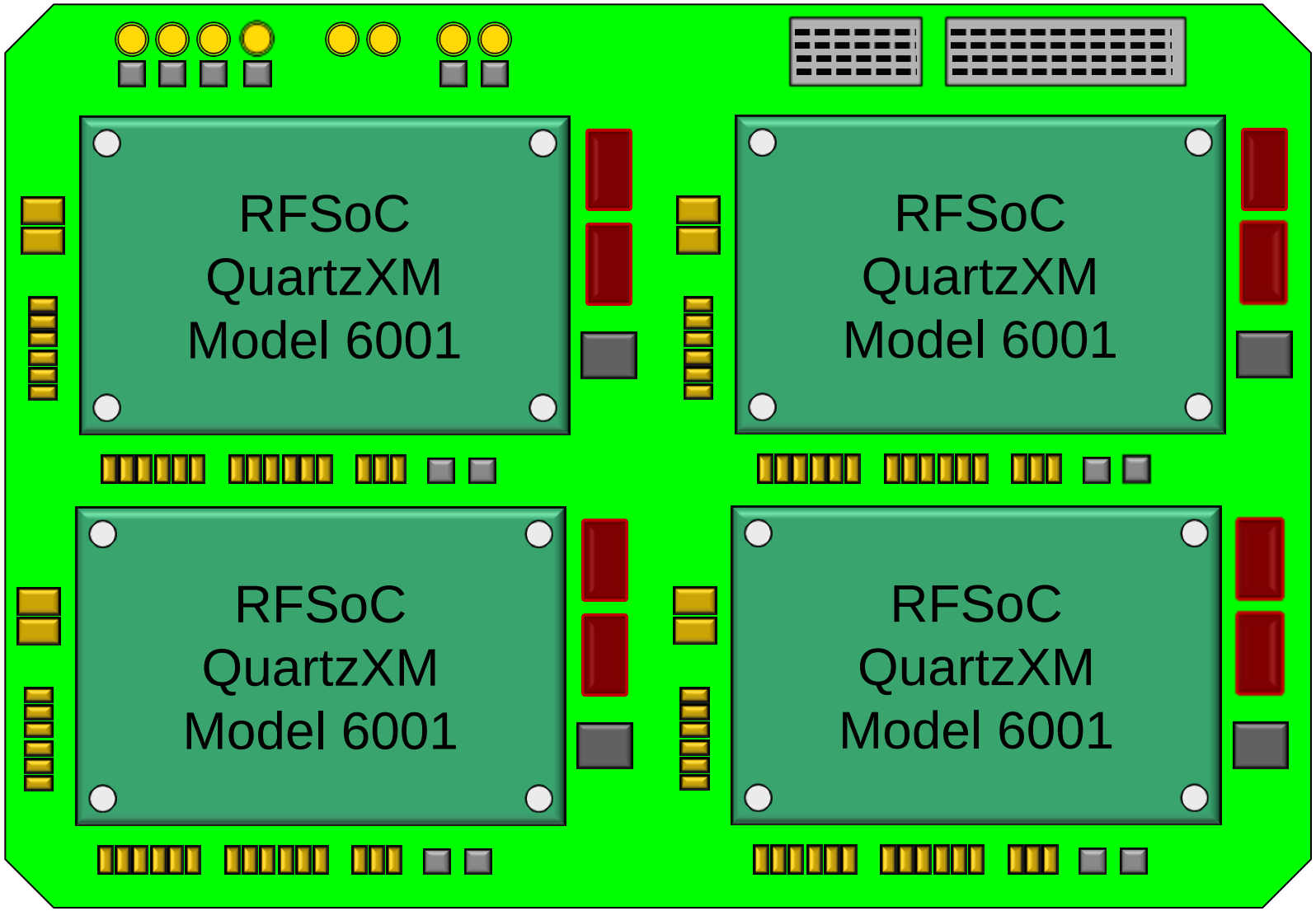
Migrating QuartzXM to Custom Platforms

- Development Strategy
  - Start with standard open-architecture product like 5950
  - Develop software and IP for custom form factor application
- Custom Carrier
  - Use Pentek Quartz Carrier Design Package
  - Pin definition, design rules, layout guidance and design review
  - Attach QuartzXM Module
  - Keep 5950 as a development platform

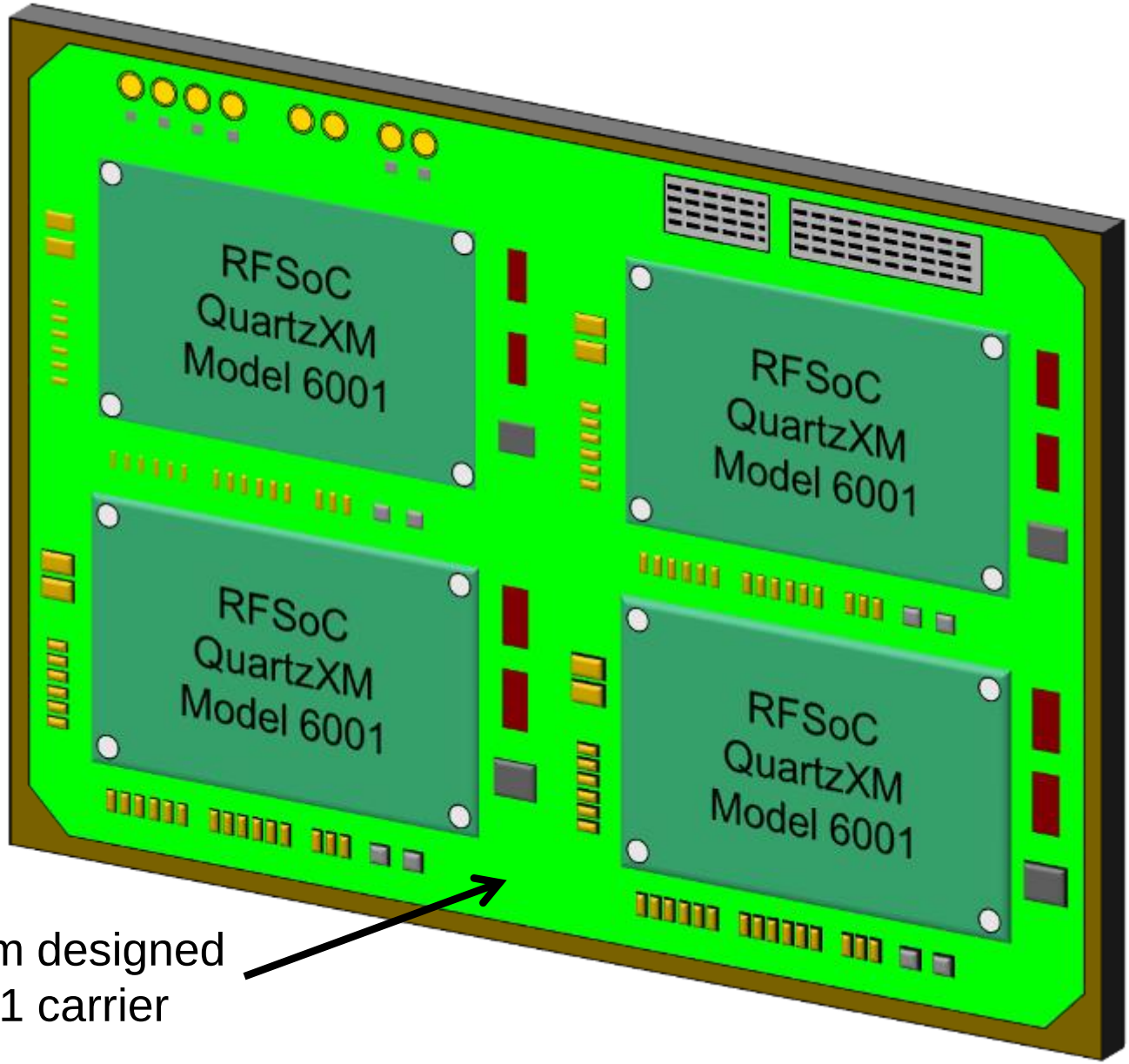




Custom RFSoC SoM Solutions



Custom RFSoC SoM Solutions

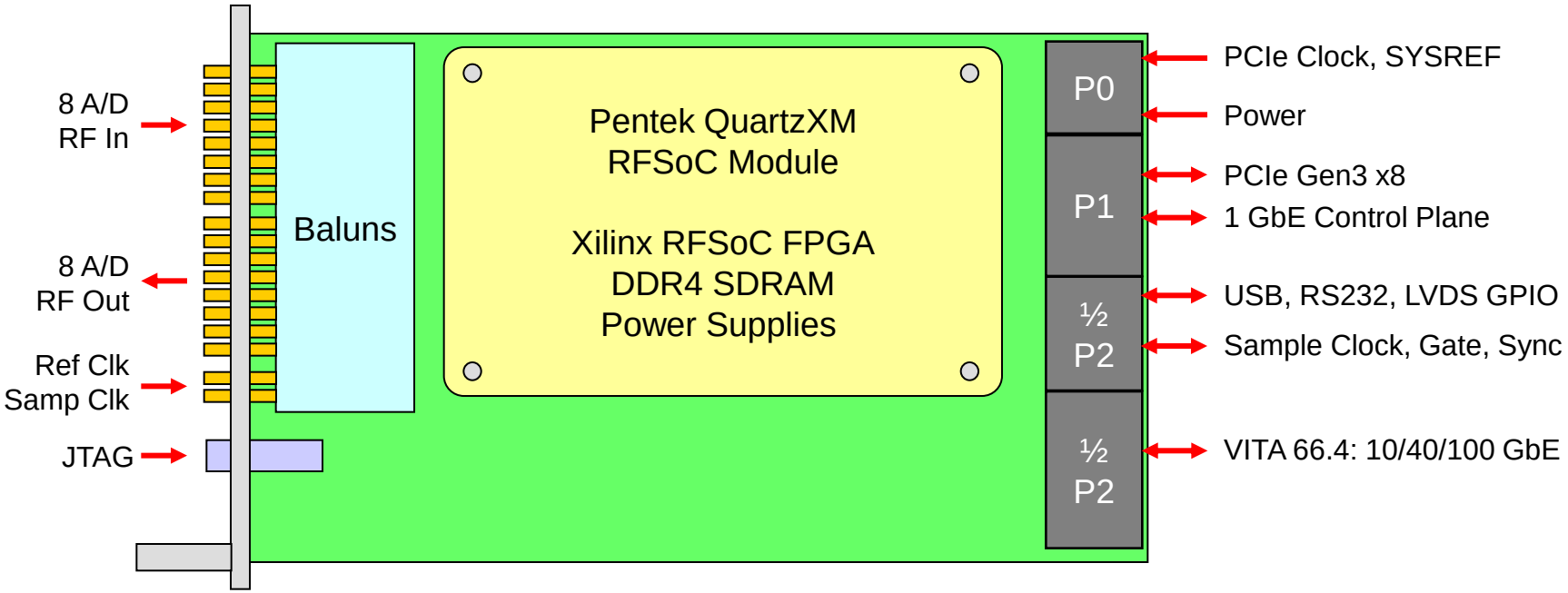


Customer's
8 x 4 antenna
array

Custom designed
6001 carrier

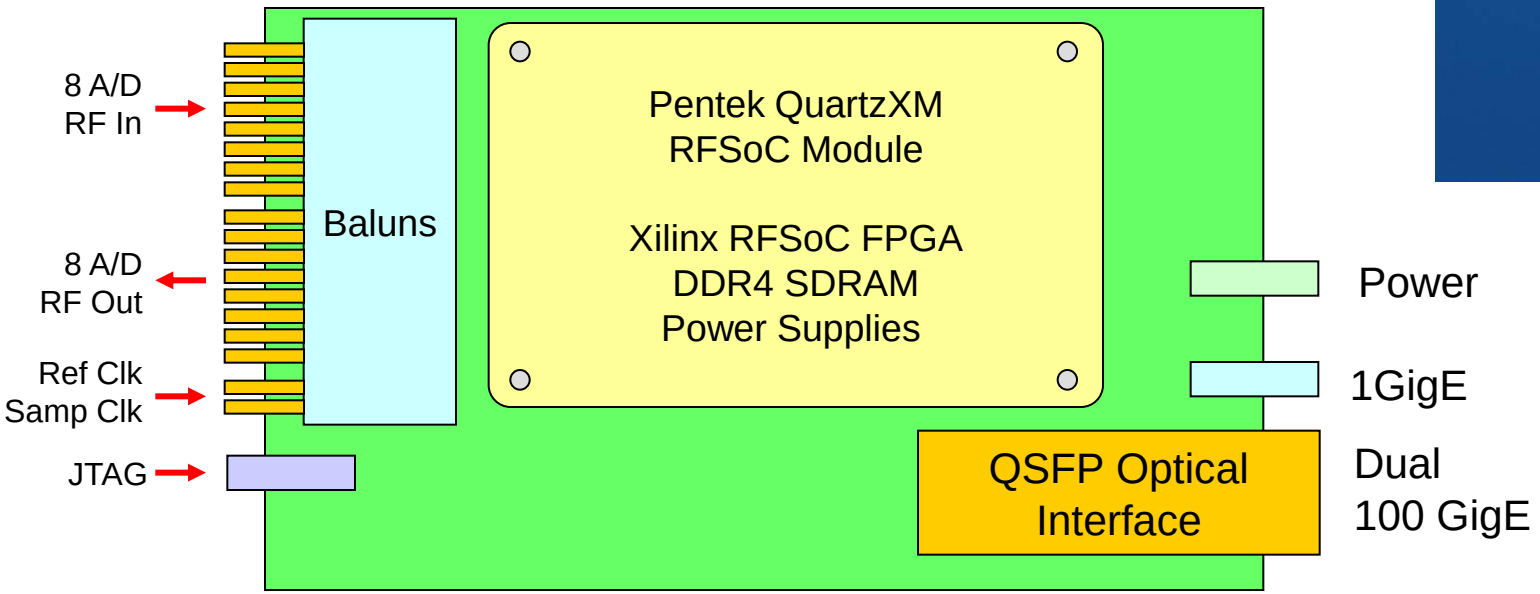
Small Form Factor Remote Box

- Create or adapt a carrier for the QuartzXM module
- For example, start with the Model 5950 3U VPX board
- Modify the board to remove VPX connectors & hardware



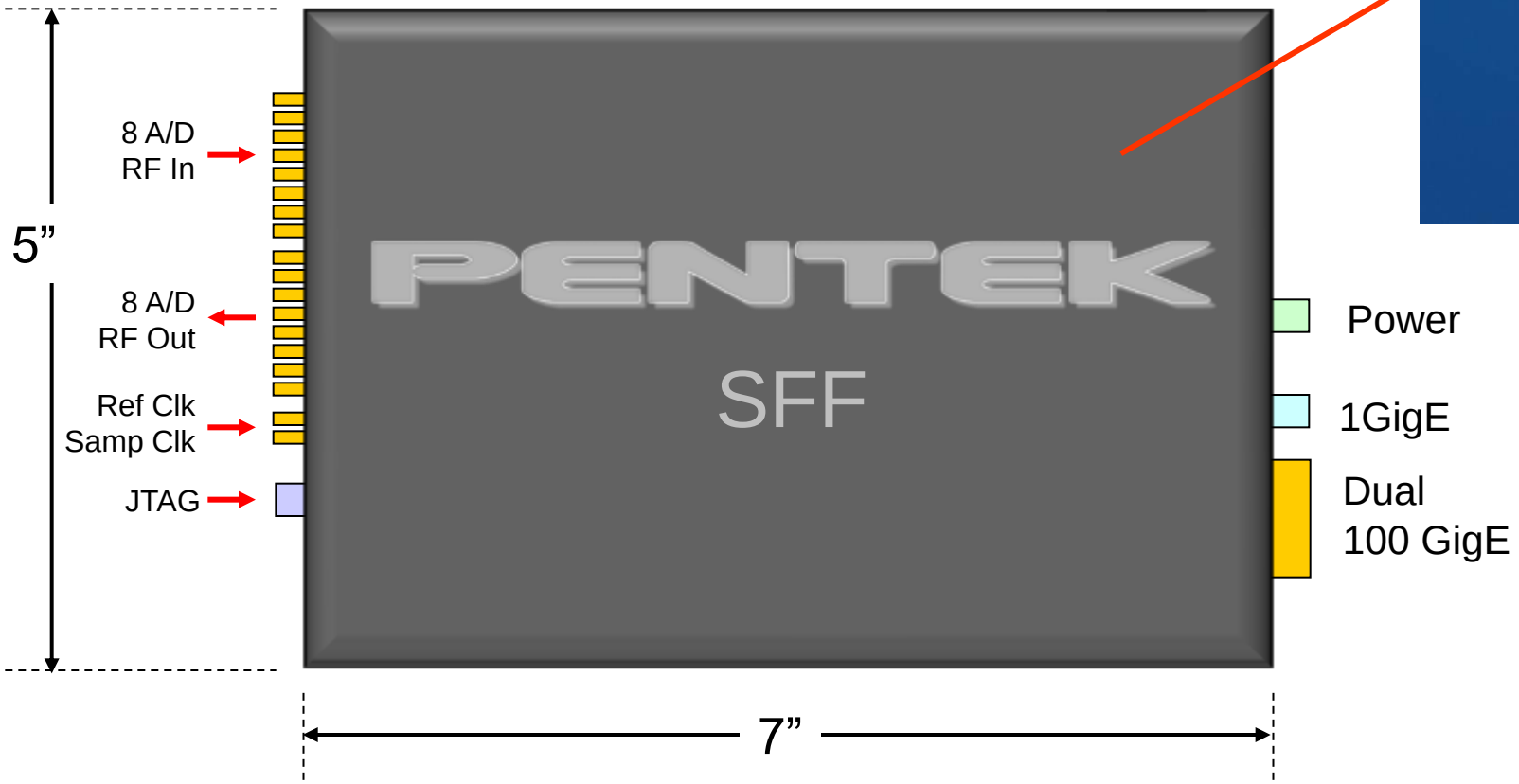
Small Form Factor Remote Box

- Add connectors appropriate for the application



Small Form Factor Remote Box

- Install it within a suitable SFF sealed enclosure
- Mount the unit on a mast near the antenna
- Complete 8-channel RF transceiver sub-system



Model 4801 Carrier Design Package

- Documentation needed for a customer to design his own carrier
  - Pin definitions and electrical specifications of all signals on the QuartzXM
  - 3D mechanical models
  - Thermal profiles of the module and components
  - Carrier reference design schematics
  - PCB stack-up recommendations
  - PCB design guidelines and routing rules
  - Operating system and bootstrap guidelines
  - Additional electrical and mechanical engineering guidance

- Carrier Design Package purchase requires an NDA

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- FPGA IP Development Strategies
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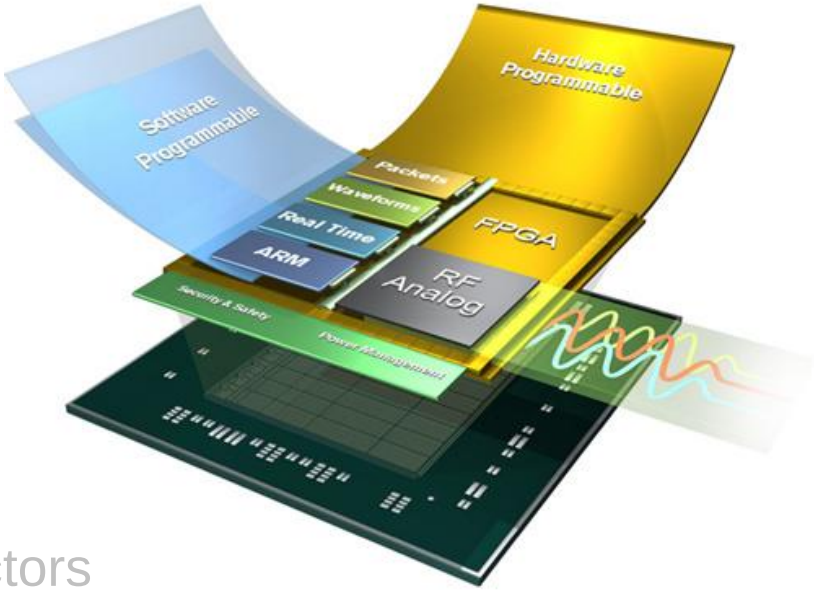


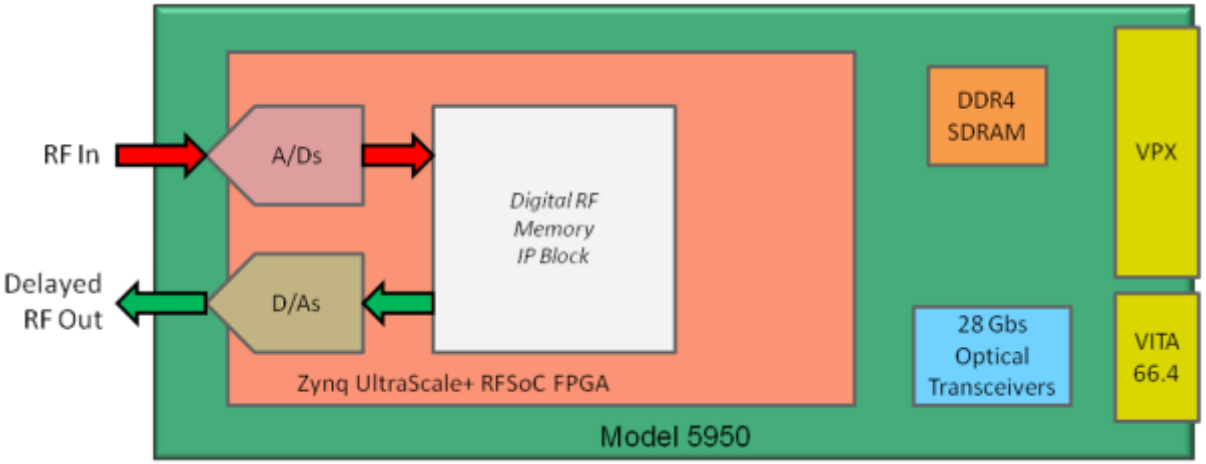
FPGA Design Strategies for RFSoC

- Xilinx Vivado Tool Suite
  - Vivado IP Integrator
    - Graphical Design Entry Tool
  - Vivado AXI-4 IP Library Modules
    - Standardized for compatibility
  - Vivado High-Level Synthesis
    - Generates RTL from C & C++
  - Vivado Simulator
    - Design Verification
  - TCL Tool Command Language
    - Scripting language

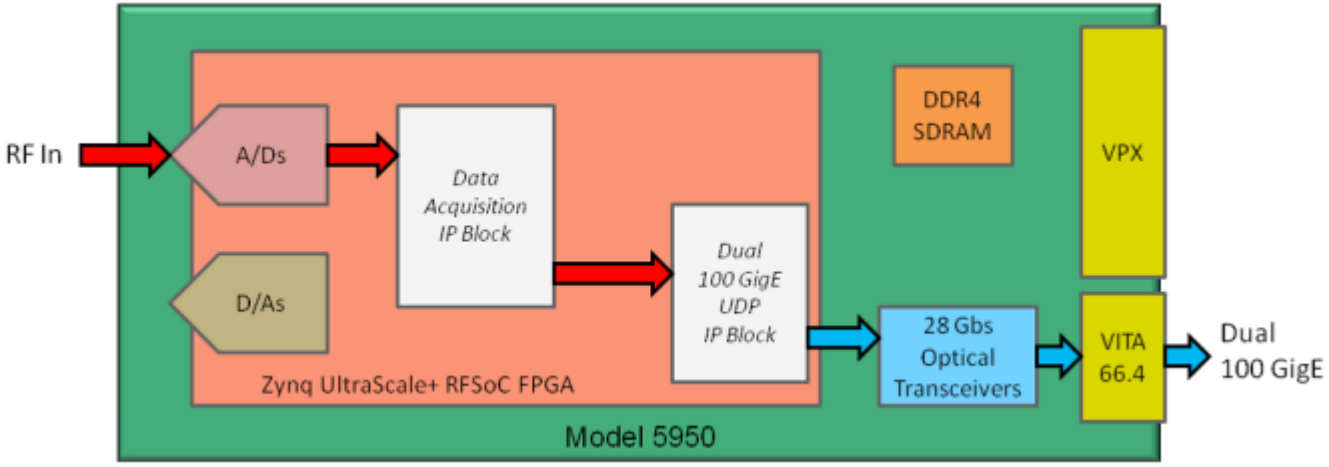
- Pentek Navigator FDK for RFSoC
  - Complete Vivado Project Folder
    - All files included ready for development
  - Full AXI-4 Compliant IP Library
    - Full IP Source code included
  - Pentek FPGA Resource Modules
    - DMA controllers, triggering & gating
    - Timing & synchronization
    - 100 GbE engines
  - Factory Installed RFSoC Applications
    - Radar & Data Acquisition
    - Waveform Generation

Included RFSoC Starter Applications

Digital RF Memory with Programmable Delay

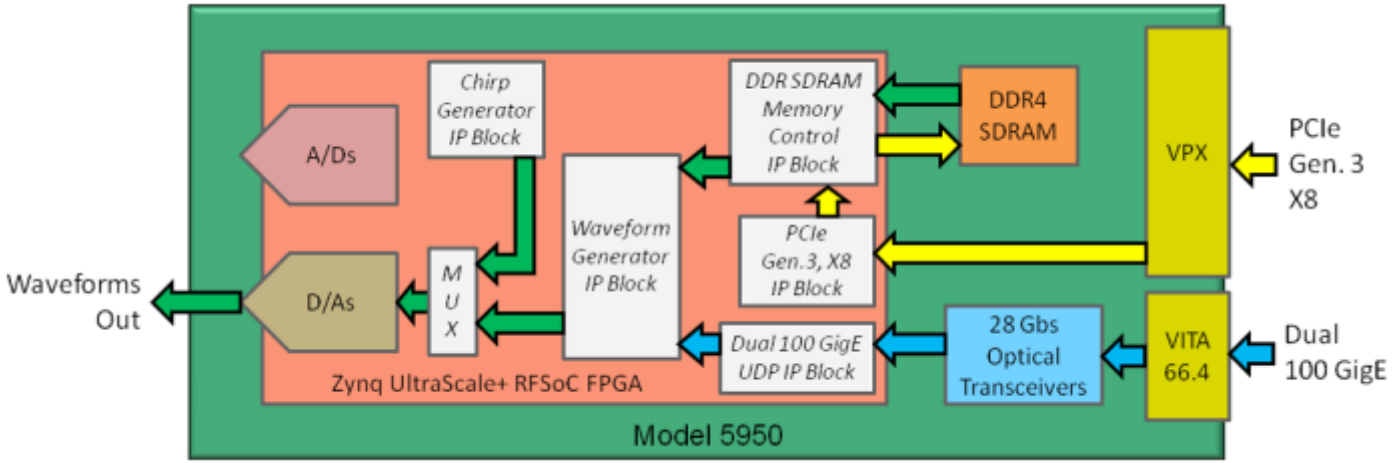


A/D Acquisition Engine to 100 GbE Optical Streaming

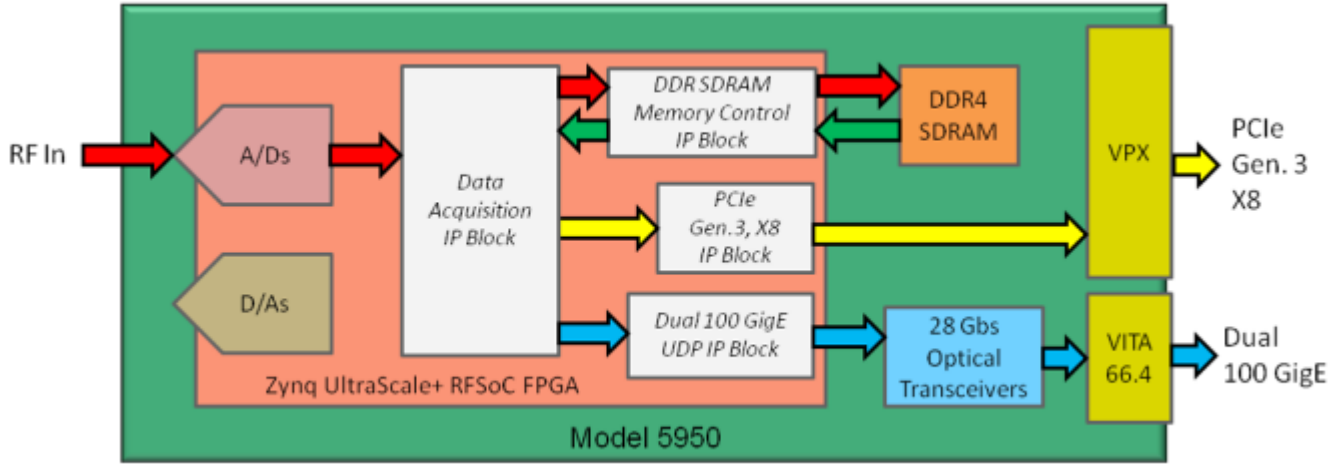


Included RFSoC Starter Applications

Waveform Generator from Memory, PCIe, or 100 GbE



Multi-mode Acquisition to Delay Memory, PCIe, or 100 GbE



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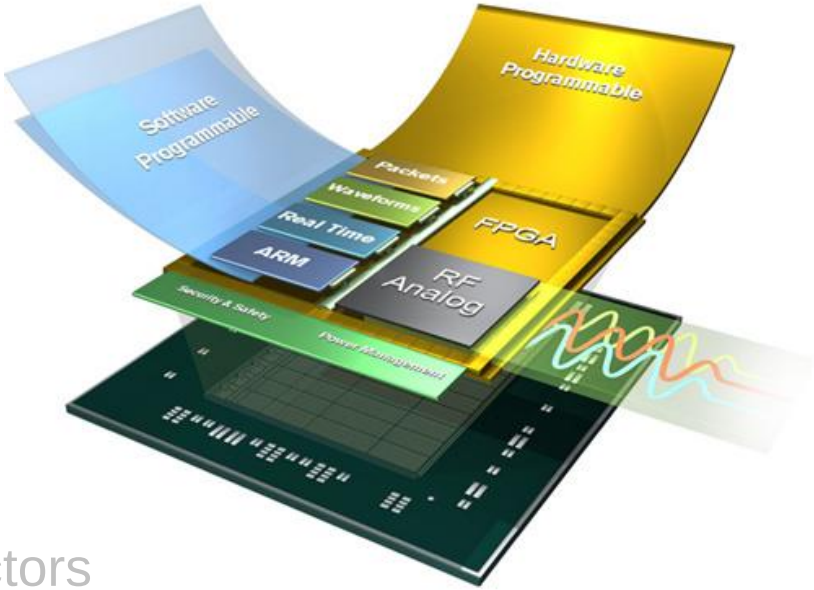


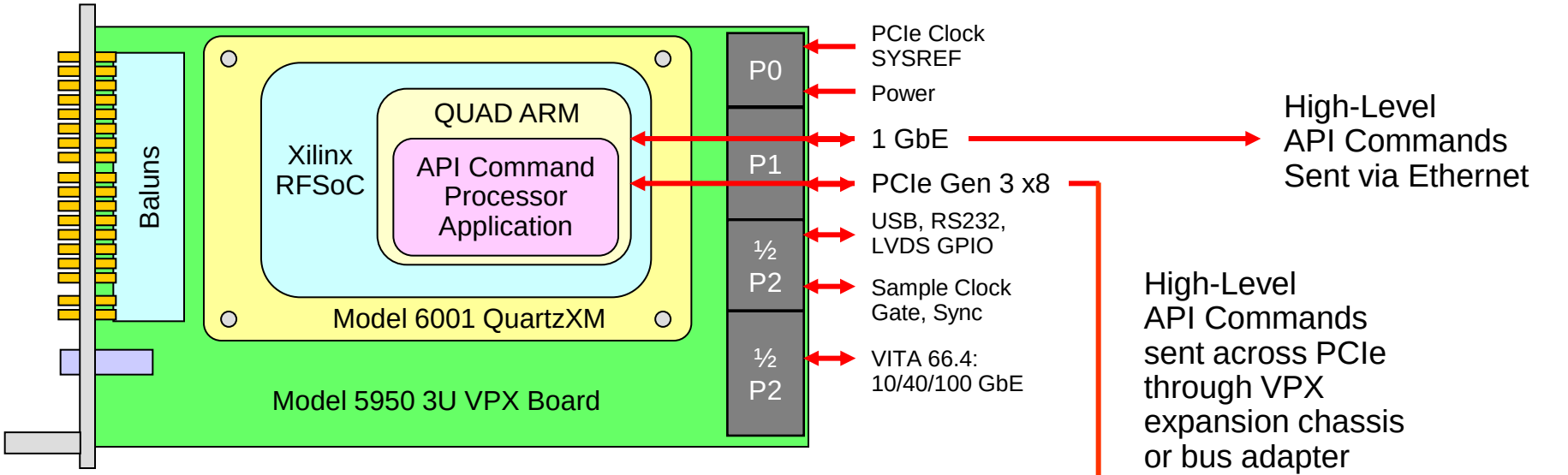
FPGA Design Strategies for RFSoC

XILINX ALL PROGRAMMABLE™ VIVADO™

NAVIGATOR Board Support Package

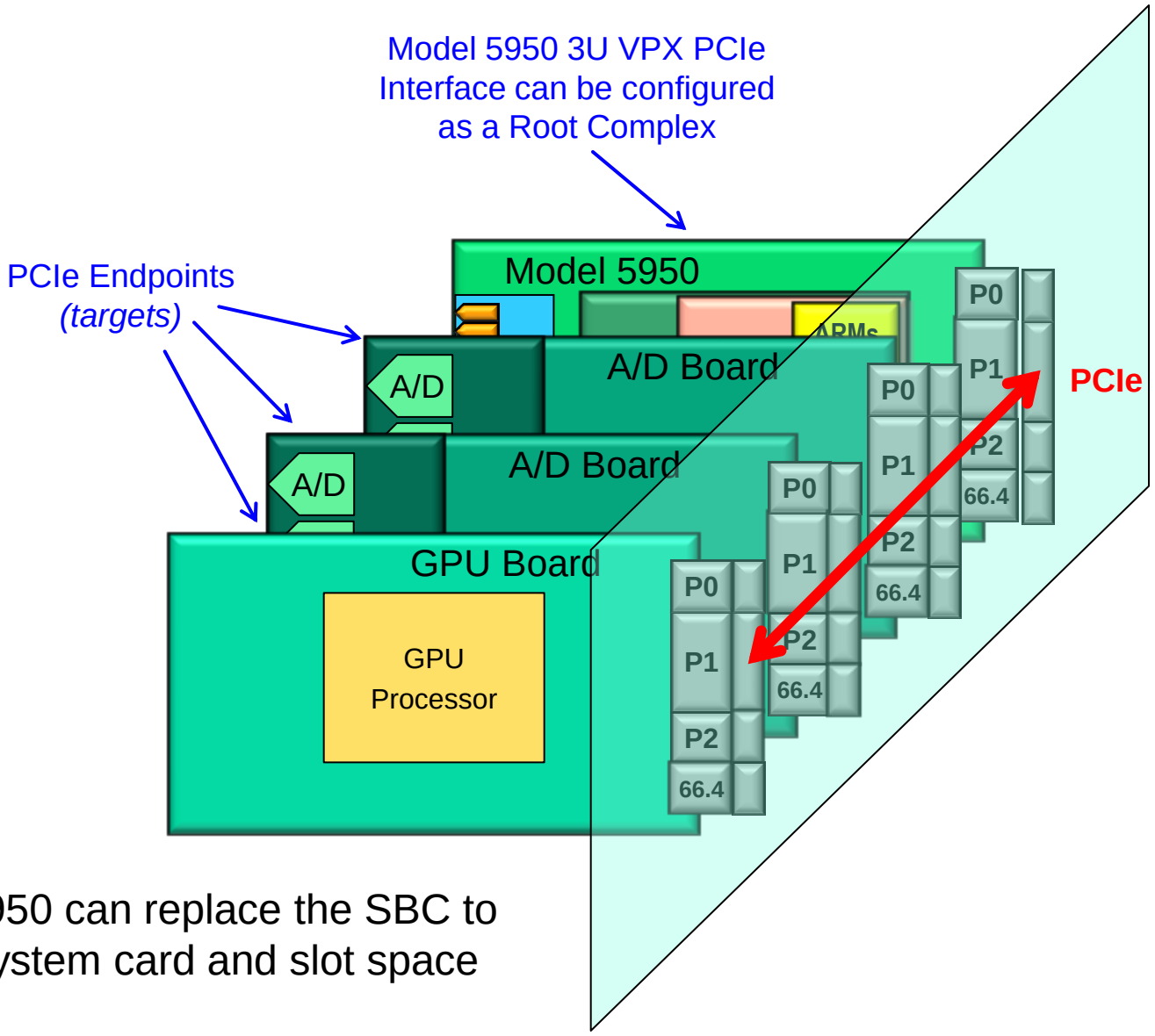
- Xilinx Vivado Tools for RFSoC
  - Xilinx RFSoC ARM SDK
    - Complete Integrated Design Environment (IDE) interfaces to Vivado FPGA tools
    - Multi-processor hardware/software co-debug capabilities
    - Editor, compilers, build tools, flash memory management
    - Libraries and device drivers
    - Xilinx Software Command Line Tool (XSCT) for scripting
  - Xilinx PetaLinux
    - Linux OS for ARM Processor
    - Linux Tools and Utilities
- Pentek Navigator BSP for RFSoC
  - Navigator command processor
    - RFSoC ARM command processor application executes high-level API commands from PCIe or Ethernet
  - Powerful Tool Suite
    - Initialization and control of all FPGA IP
    - Delivery of all operational parameters
    - High-Level C-Language Libraries
    - Full C Source Code Provided
    - Numerous Program Code Examples
    - Device Drivers for Windows & Linux
  - Signal Viewer Utility
    - Displays acquired signals on virtual spectrum analyzer and oscilloscope

Flexible API Command Processing



- ARM Processor on QuartzXM runs the Pentek Navigator QuartzXM API Command Processor
- Accepts API commands across Ethernet
- Accepts API commands across PCIe bus
- Flexible options for different system architectures

Multiboard 3U VPX System Architectures



- Model 5950 can replace the SBC to save a system card and slot space

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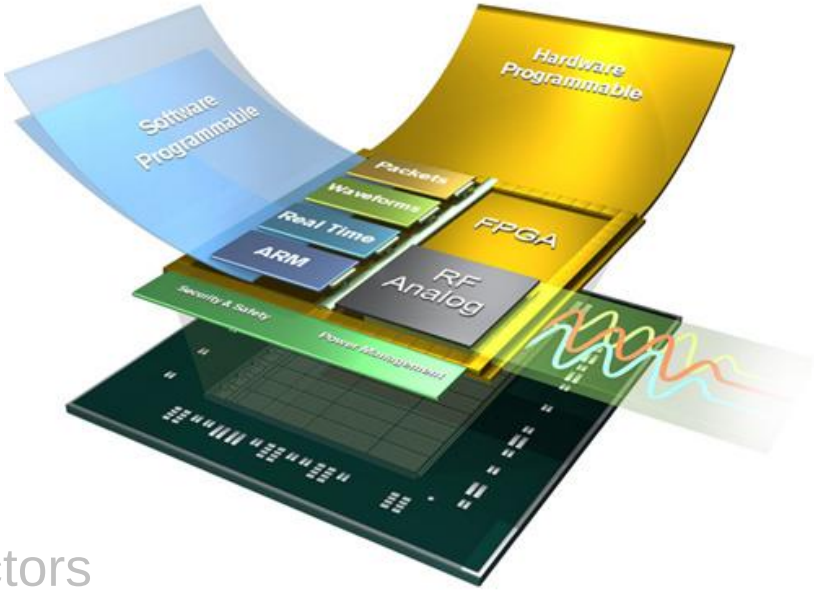
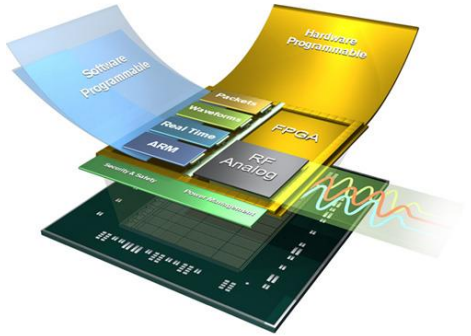
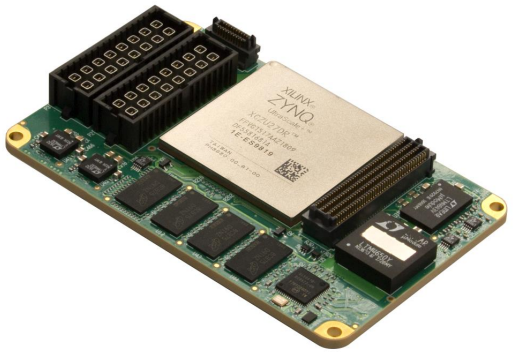


RFSoC Deployment Strategies

- Xilinx RFSoC Offers Extreme Integration
  - A/D, D/A, FPGA, ARM Processor, Flexible I/O
  - Low Latency for wideband RF signals
- Pentek QuartzXM Simplifies System Design
  - Small footprint for high density applications
  - Complete RFSoC infrastructure with DDR4, clock management, & power supplies
  - High performance RF and digital connectors
- Xilinx Vivado Tools
  - FPGA development tools
  - ARM processor OS and development tools
- Pentek Navigator FDK and BSP Tools
  - API command processor for ARM
  - Factory installed FPGA IP modules for timing, DMA controllers, PCIe, memory controllers
  - FPGA IP AXI-4 library functions
  - Four starter application examples installed
- Speeds development cycles, saves costs





Thank you! For More Information……

- Visit www.pentek.com/RFSoC
- Data Sheets
  - Model 5950 3U VPX RFSoC Board
  - Model 6001 RFSoM Module
- Whitepaper
  - Xilinx's Zynq UltraScale+ RFSoC
- Pentek Pipeline Summer 2018
  - Strategies for Deploying RFSoC
- Live Signal Acquisition Video
  - Shows A/D acquisition using ARM-based API Command Processor

Live Signal Acquisition: Quartz Model 5950 and Model 6001 RFSoC boards