SDR OFDM Waveform design for a UGV/UAV communication scenario

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Christian Blümm
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Introduction

Goal:

Robust and *flexible* wireless communication for UAVs (Unmanned Air Vehicles) and UGVs (Unmanned Ground Vehicles) in civil use

Application Examples:

- Detection and monitoring of hazardous substances
- Search and rescue
- Security services
- Environmental mapping and –monitoring
- Surveillance of major sport events
- …

Introduction

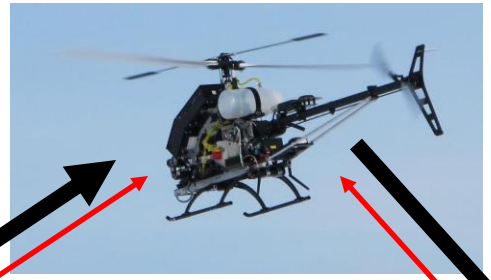
Goal:

Robust and *flexible* wireless communication for UAVs (Unmanned Air Vehicles) and UGVs (Unmanned Ground Vehicles) in civil use

Approach:

- OFDM (Orthogonal Frequency Division Multiplexing) based waveform
- Highest parameter flexibility for maximum throughput in heterogenous environments with varying demands (e.g. fast changing channels, high speed)
- Two independent logical links for control data and video data (OFDMA)
- TDMA (Time Division Multiple Access) on MAC layer
- Self designed hybrid SDR platform with FPGA (Virtex 5) and GPP (Intel Atom)

Scenario



UAV
relay

Radio link
UGV-UAV
0,5-1 km
LOS

Radio link UAV-
Base station
5-10 km
LOS

UGV
sensor carrier

NLOS

Base station

narrowband, high-available
control-data link, bidirectional
about 115 kbit/s (TCP/IP)

broadband mission-data link
unidirectional, about 10-20 Mbit/s
(UDP/IP)

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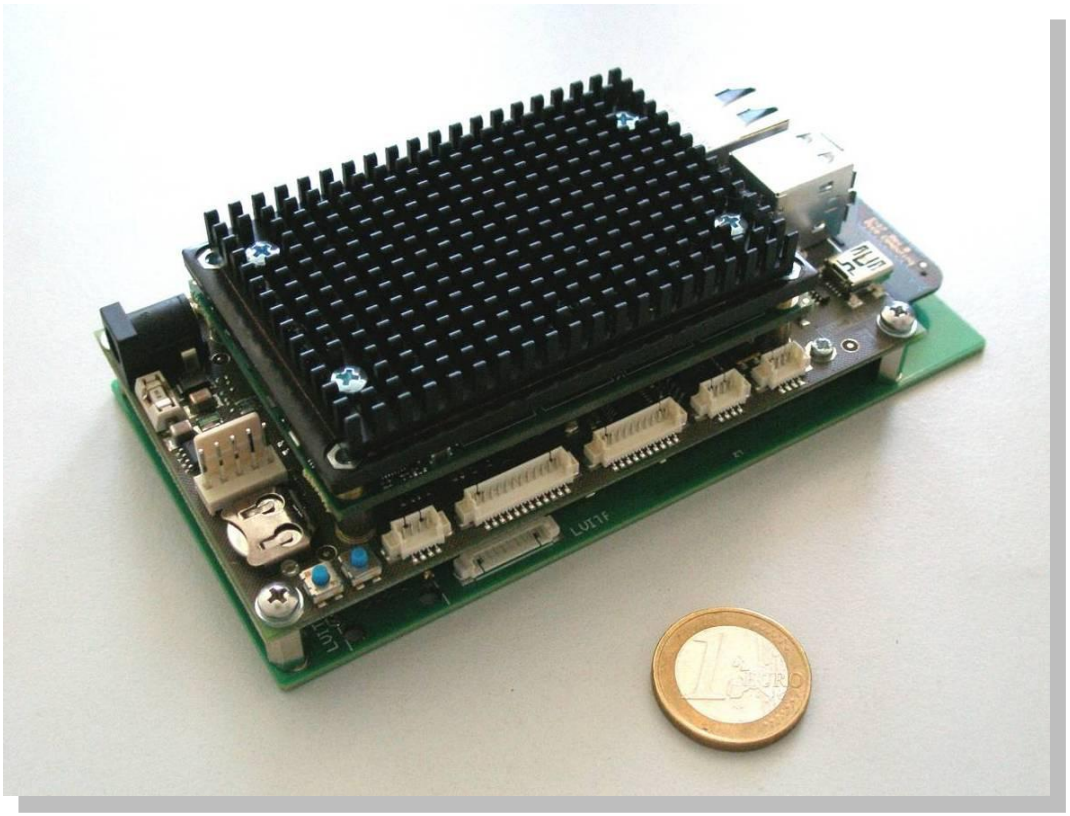
Hardware Platform



Platform Setup:

- COTS microprocessor board
- COTS FPGA board
- customized interface board

Characteristics:

- high performance
- small form factor
- universal system interfaces

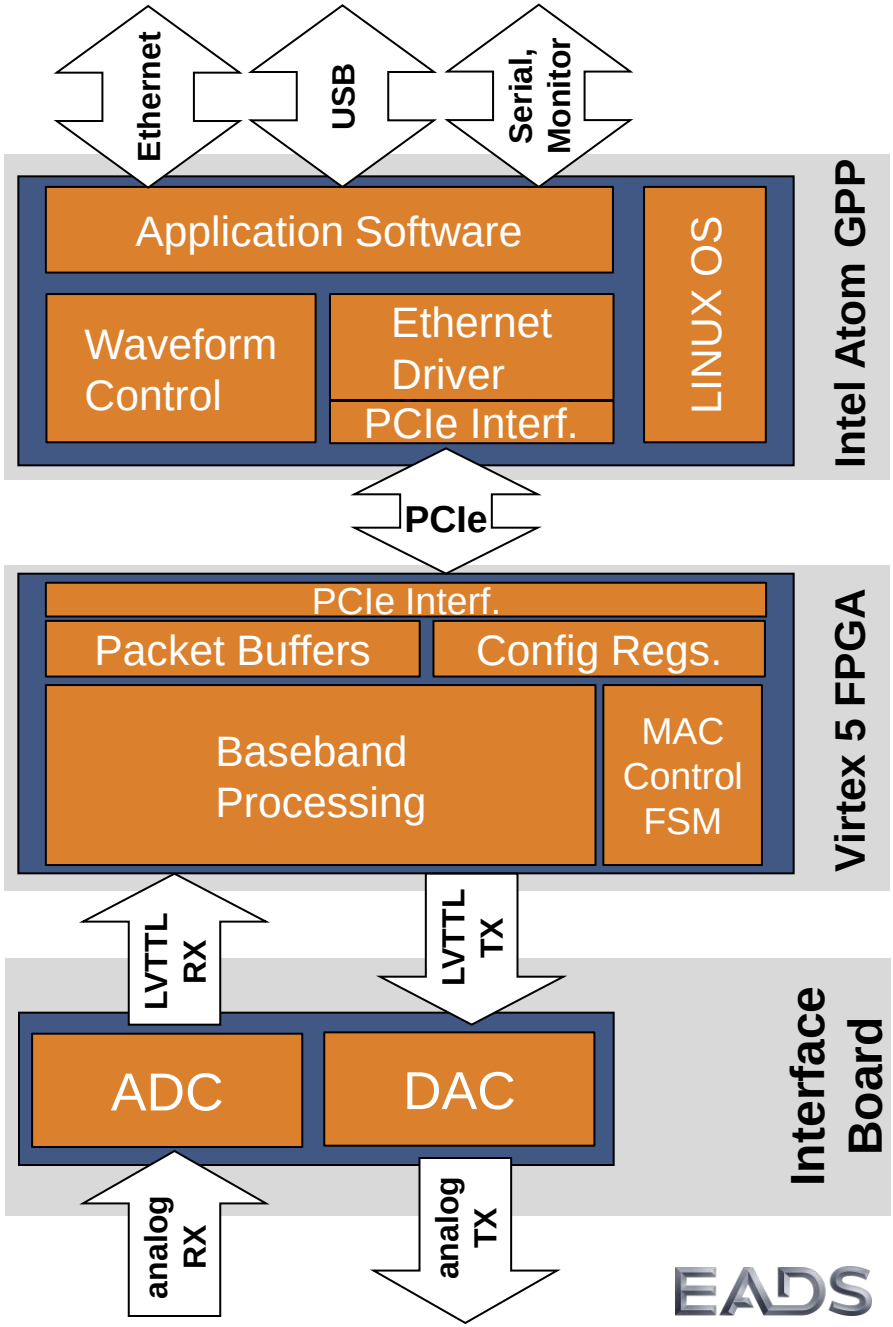
Hardware Platform

COTS Microprocessor Board
- Intel ATOM processor 1.6 GHz
- 1 GB RAM, 4 GB Flash Memory
- 1 Gbit Ethernet, USB 2.0, monitor IF,…
- compatible with standard Linux kernel

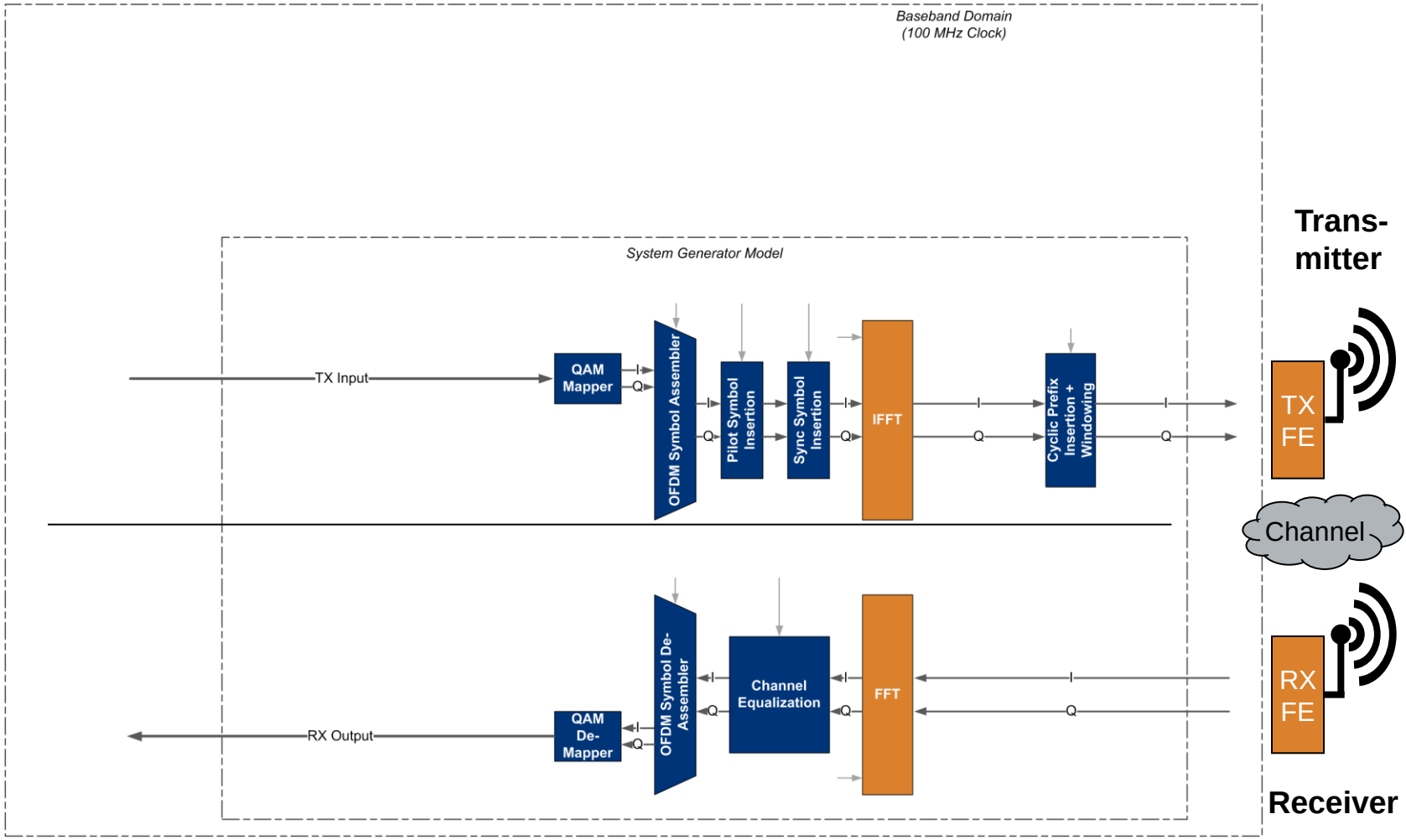
COTS FPGA Board
Xilinx Virtex 5 FPGA
Flash for FPGA configuration
32 LVDS I/Os or 64 LVTTL
2 RocketIO GTP with up to 3.75 Gbit/s

Self-designed Interface Board
- 16 Bit ADC
- 16 Bit DAC

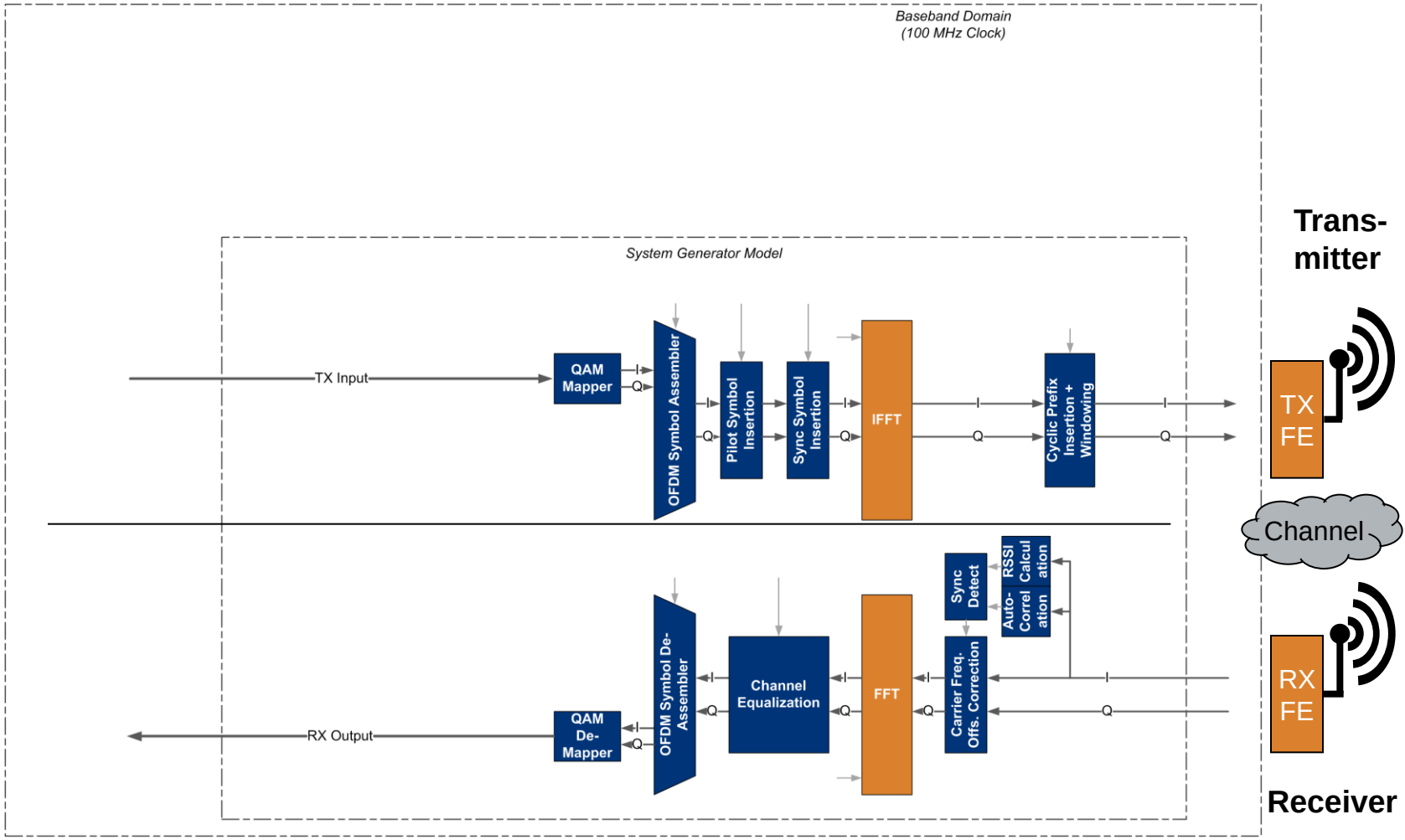
Hardware Platform



Waveform


Baseband Domain
(100 MHz Clock)
System Generator Model
TX Input
QAM Mapper
OFDM Symbol Assembler
Pilot Symbol Insertion
Sync Symbol Insertion
IFFT
Cyclic Prefix Insertion + Windowing
Trans-mitter
TX FE
Channel
RX FE
Receiver
RX Output
QAM De-Mapper
OFDM Symbol De-Assembler
Channel Equalization
FFT

Waveform


Baseband Domain
(100 MHz Clock)
System Generator Model
TX Input
QAM Mapper
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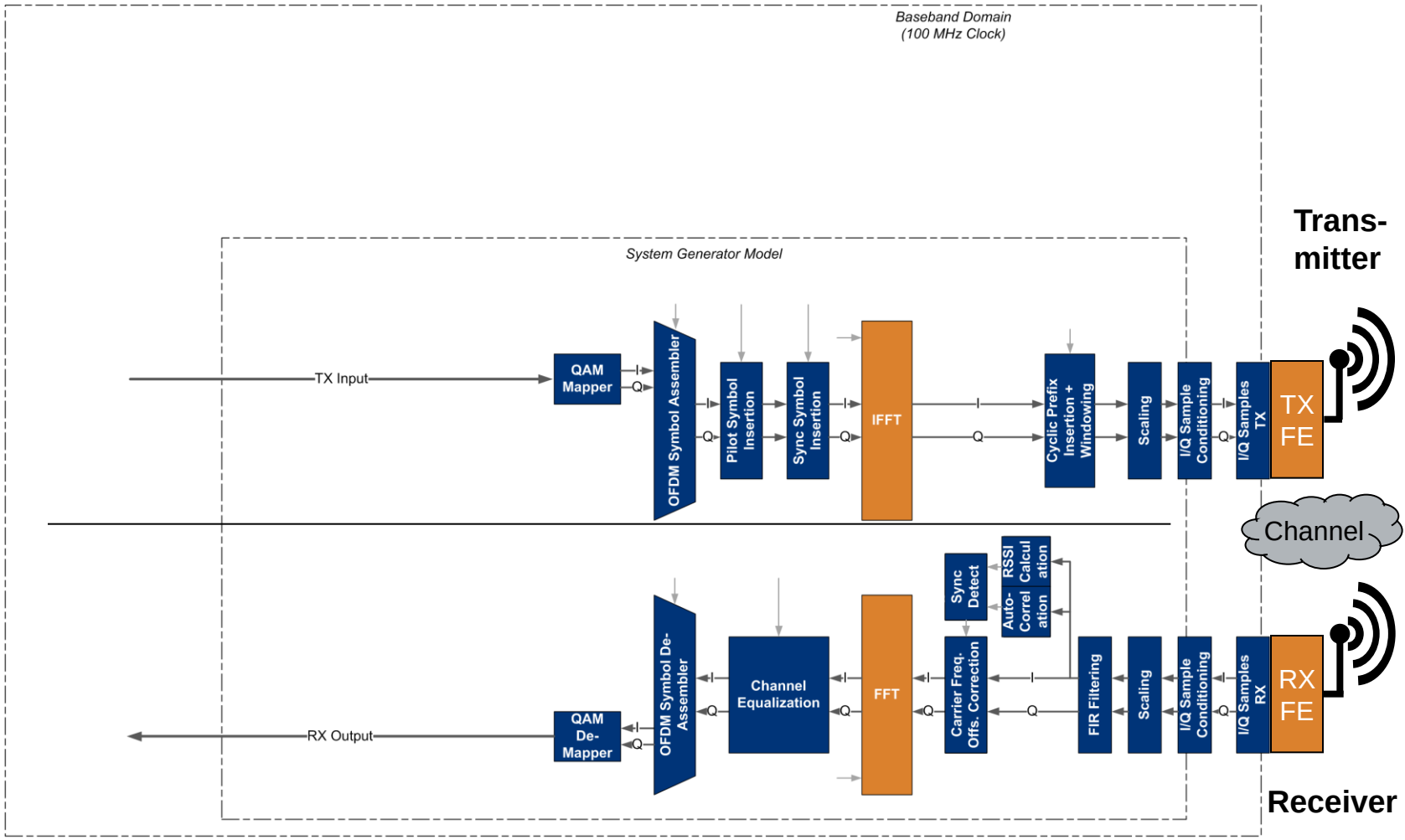
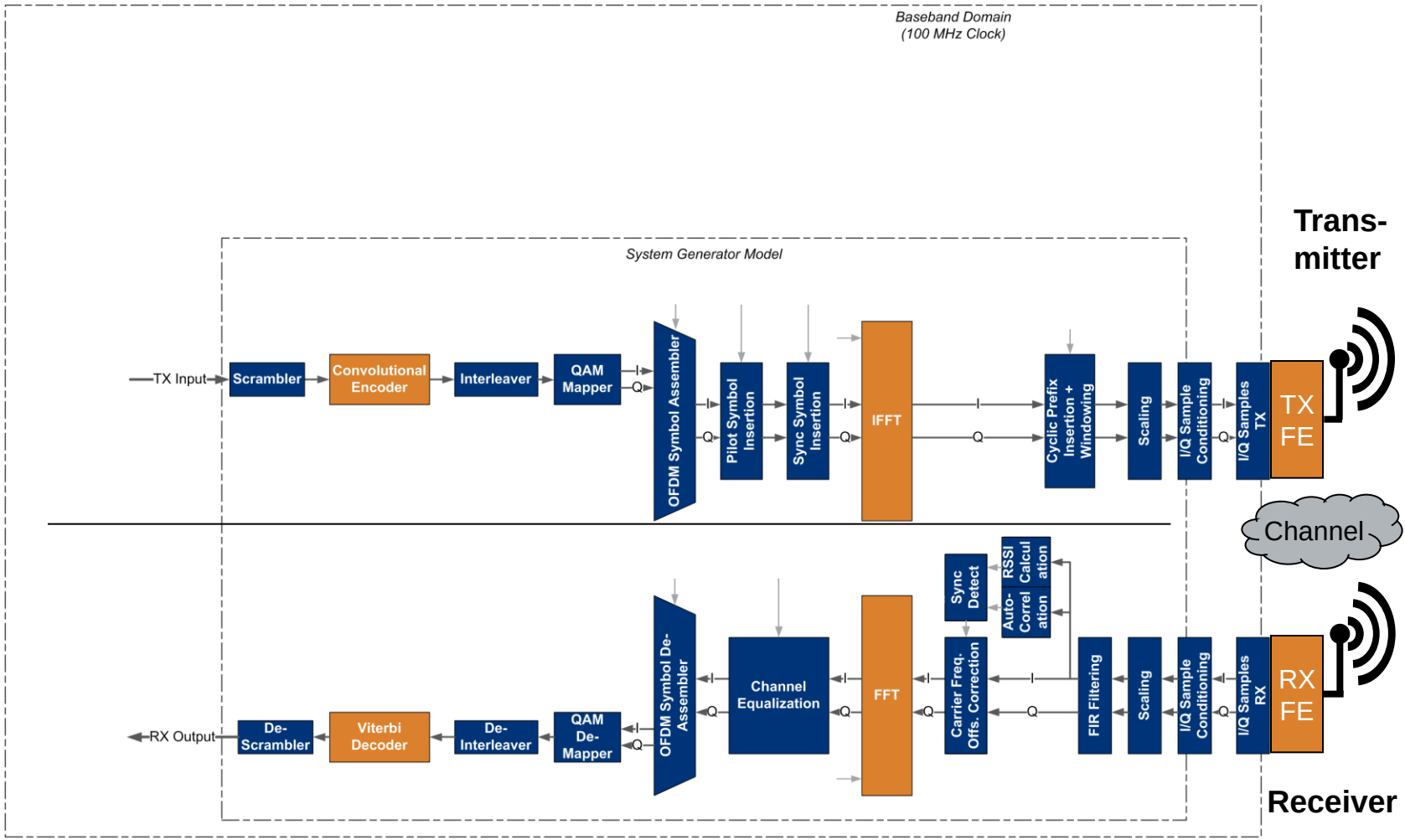
Pilot Symbol Insertion
Sync Symbol Insertion
IFFT
Cyclic Prefix Insertion + Windowing
Trans-mitter
TX FE
Channel
RX FE
Receiver
RX Output
QAM De-Mapper
OFDM Symbol De-Assembler
Channel Equalization
FFT
Carrier Freq. Offs. Correction
Sync Detect
Auto-Correl ation
RSSI Calcul ation

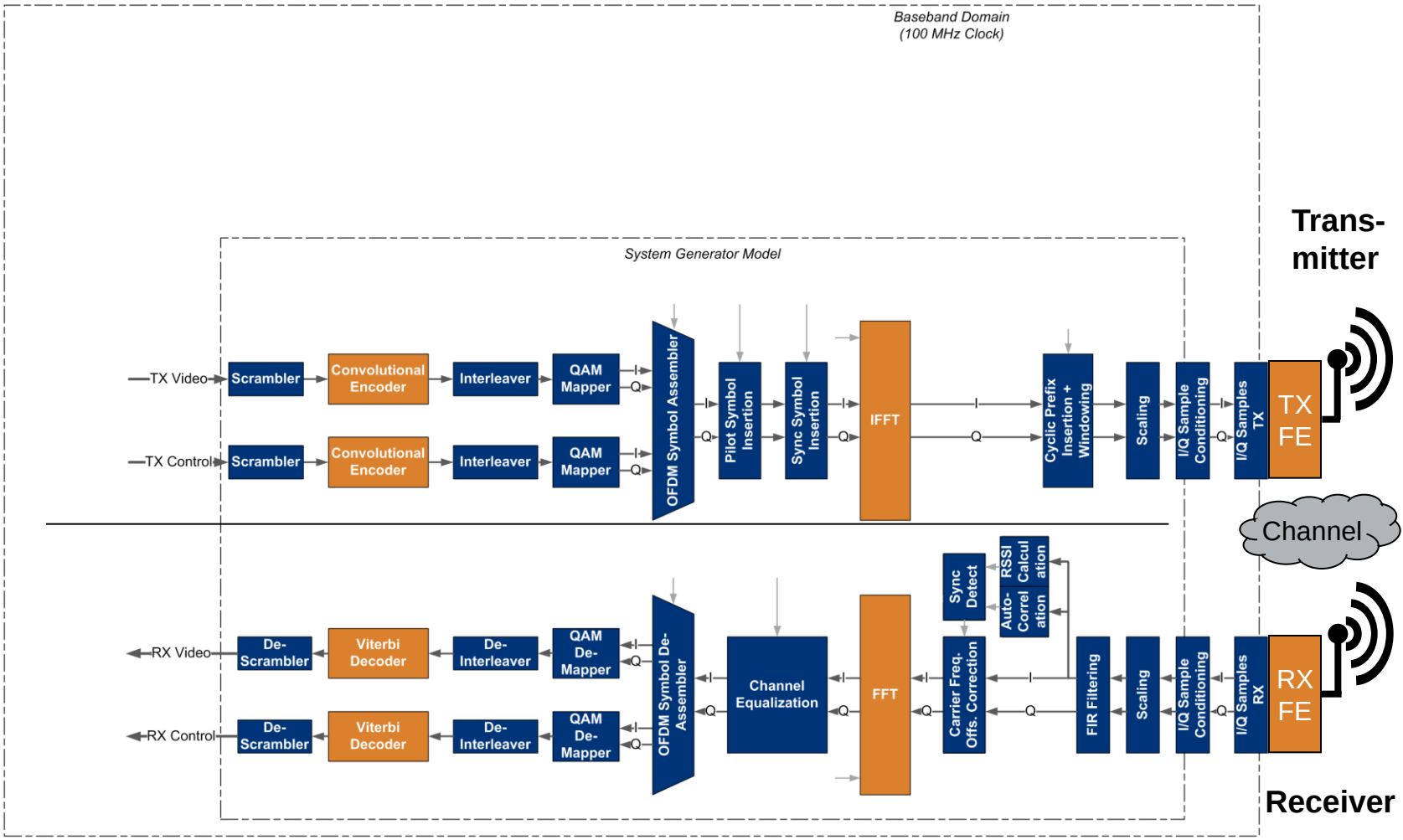
Waveform


Baseband Domain
(100 MHz Clock)
System Generator Model
TX Input
QAM Mapper
OFDM Symbol Assembler
Pilot Symbol Insertion
Sync Symbol Insertion
IFFT
Cyclic Prefix Insertion + Windowing
Scaling
I/Q Sample Conditioning
I/Q Samples TX
TX FE
Trans-mitter
Channel
RX FE
I/Q Samples RX
I/Q Sample Conditioning
Scaling
FIR Filtering
Carrier Freq. Offs. Correction
Sync Detect
Auto-Correl ation
RSSI Calcul ation
FFT
Channel Equalization
OFDM Symbol De-Assembler
QAM De-Mapper
RX Output
Receiver

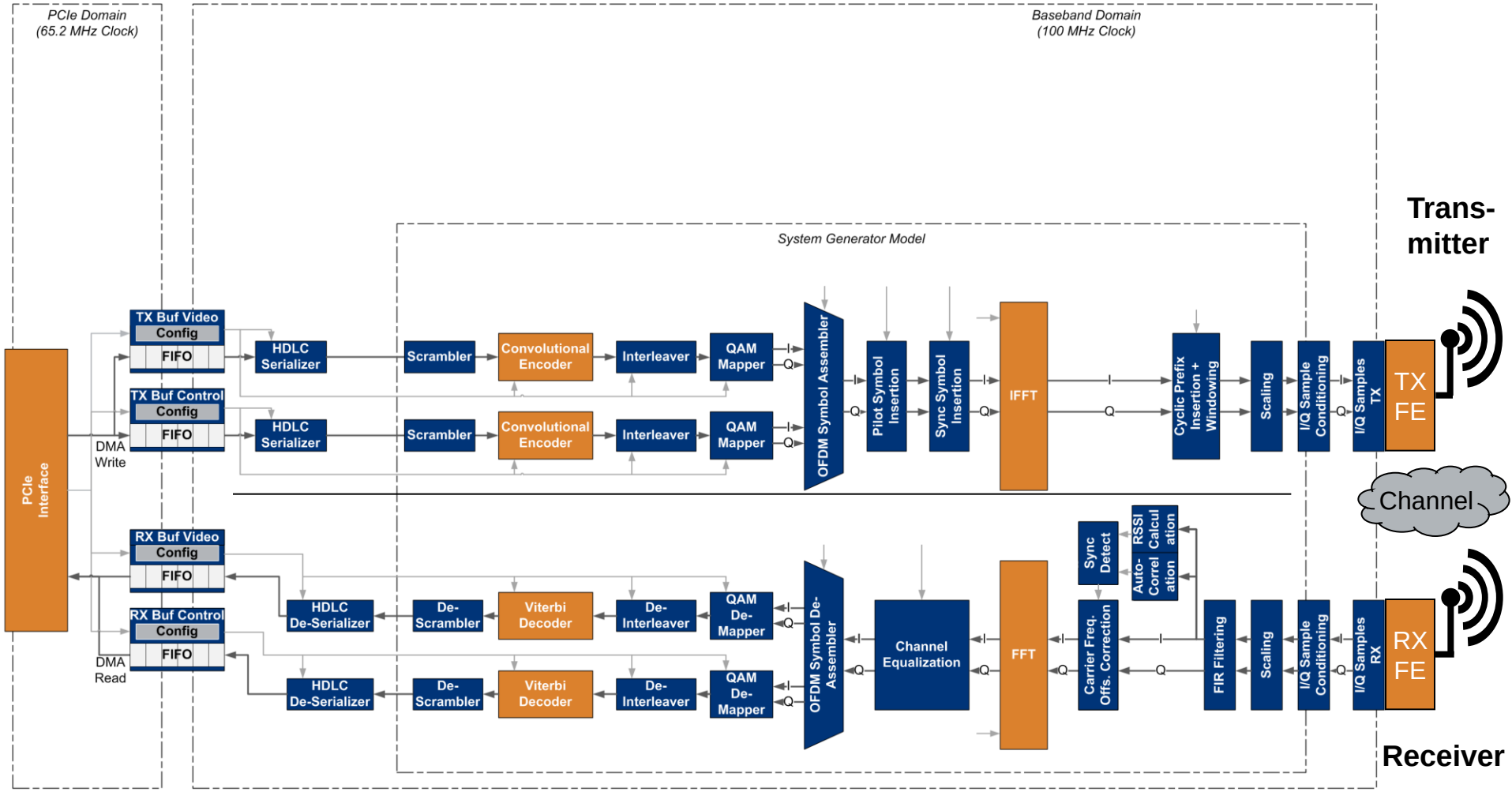
Waveform


Baseband Domain
(100 MHz Clock)
System Generator Model
TX Input
Scrambler
Convolutional Encoder
Interleaver
QAM Mapper
OFDM Symbol Assembler
Pilot Symbol Insertion
Sync Symbol Insertion
IFFT
Cyclic Prefix Insertion + Windowing
Scaling
I/Q Sample Conditioning
I/Q Samples TX
TX FE
Trans-mitter
Channel
RX FE
I/Q Samples RX
I/Q Sample Conditioning
Scaling
FIR Filtering
Carrier Freq. Offs. Correction
Auto-Correl ation
RSSI Calcul ation
Sync Detect
FFT
Channel Equalization
OFDM Symbol De-Assembler
QAM De-Mapper
De-Interleaver
Viterbi Decoder
De-Scrambler
RX Output
Receiver

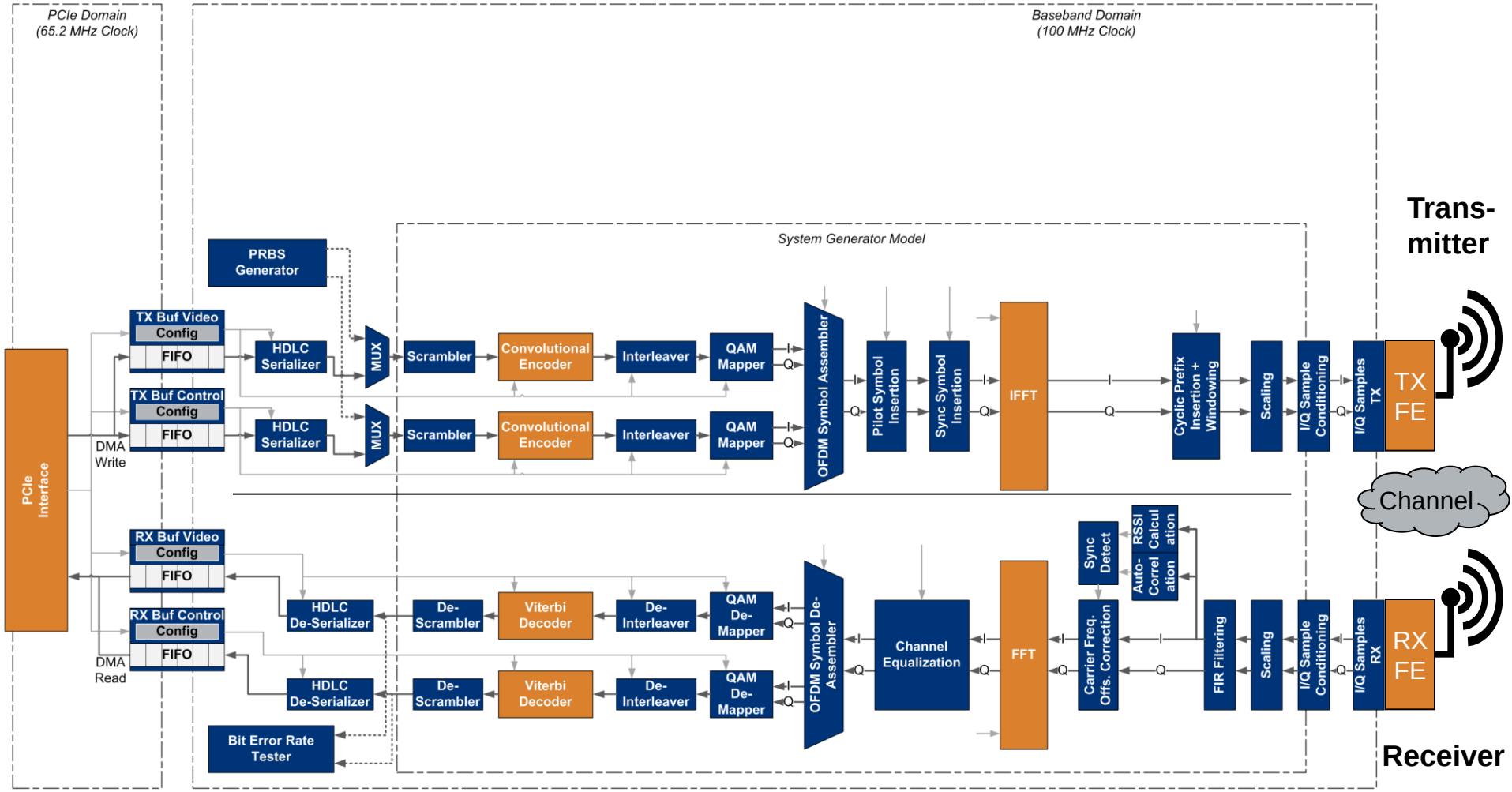
Waveform


Baseband Domain
(100 MHz Clock)
System Generator Model
TX Video
TX Control
Scrambler
Scrambler
Convolutional Encoder
Convolutional Encoder
Interleaver
Interleaver
QAM Mapper
QAM Mapper
OFDM Symbol Assembler
Pilot Symbol Insertion
Sync Symbol Insertion
IFFT
Cyclic Prefix Insertion + Windowing
Scaling
I/Q Sample Conditioning
I/Q Samples TX
TX FE
Trans-mitter
Channel
RX Video
RX Control
De-Scrambler
De-Scrambler
Viterbi Decoder
Viterbi Decoder
De-Interleaver
De-Interleaver
QAM De-Mapper
QAM De-Mapper
OFDM Symbol De-Assembler
Channel Equalization
FFT
Carrier Freq. Offs. Correction
Sync Detect
Auto-Correl ation
RSSI Calcul ation
FIR Filtering
Scaling
I/Q Sample Conditioning
I/Q Samples RX
RX FE
Receiver

Waveform


PCIe Domain
(65.2 MHz Clock)
Baseband Domain
(100 MHz Clock)
System Generator Model
PCIe Interface
DMA Write
DMA Read
TX Buf Video Config
FIFO
TX Buf Control Config
FIFO
RX Buf Video Config
FIFO
RX Buf Control Config
FIFO
HDLC Serializer
HDLC Serializer
HDLC De-Serializer
HDLC De-Serializer
Scrambler
Scrambler
De-Scrambler
De-Scrambler
Convolutional Encoder
Convolutional Encoder
Viterbi Decoder
Viterbi Decoder
Interleaver
Interleaver
De-Interleaver
De-Interleaver
QAM Mapper
QAM Mapper
QAM De-Mapper
QAM De-Mapper
OFDM Symbol Assembler
Pilot Symbol Insertion
Sync Symbol Insertion
IFFT
OFDM Symbol De-Assembler
Channel Equalization
FFT
Sync Detect
RSSI Calculation
Auto-Correlation
Carrier Freq. Offs. Correction
Cyclic Prefix Insertion + Windowing
FIR Filtering
Scaling
Scaling
I/Q Sample Conditioning
I/Q Sample Conditioning
I/Q Samples TX
I/Q Samples RX
TX FE
RX FE
Trans-mitter
Channel
Receiver

Waveform


PCIe Domain
(65.2 MHz Clock)
Baseband Domain
(100 MHz Clock)
System Generator Model
PRBS Generator
TX Buf Video
Config
FIFO
TX Buf Control
Config
FIFO
HDLC Serializer
HDLC Serializer
MUX
MUX
Scrambler
Scrambler
Convolutional Encoder
Convolutional Encoder
Interleaver
Interleaver
QAM Mapper
QAM Mapper
OFDM Symbol Assembler
Pilot Symbol Insertion
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IFFT
Cyclic Prefix Insertion + Windowing
Scaling
I/Q Sample Conditioning
I/Q Samples TX
TX FE
Trans-mitter
PCIe Interface
DMA Write
Channel
RX Buf Video
Config
FIFO
RX Buf Control
Config
FIFO
DMA Read
HDLC De-Serializer
HDLC De-Serializer
De-Scrambler
De-Scrambler
Viterbi Decoder
Viterbi Decoder
De-Interleaver
De-Interleaver
QAM De-Mapper
QAM De-Mapper
OFDM Symbol De-Assembler
Channel Equalization
FFT
Sync Detect
Auto-Correl ation
RSSI Calcul ation
Carrier Freq. Offs. Correction
FIR Filtering
Scaling
I/Q Sample Conditioning
I/Q Samples RX
RX FE
Bit Error Rate Tester
Receiver

Waveform

Runtime-configurable Parameters:

- BPSK, QPSK, 16-QAM, 64-QAM modulation
- Variable FFT length (8…1024)
- Configurable frame layout
  - Number of OFDM symbols
  - Subcarrier usage (control or data or unused)
  - Cyclic Prefix length
  - Fading between OFDM symbold for spectral smoothing: configurable windowing-length
- Convolution encoder / Viterbi decoder with adjustable code rate 1/7 … 7/8

TDMA

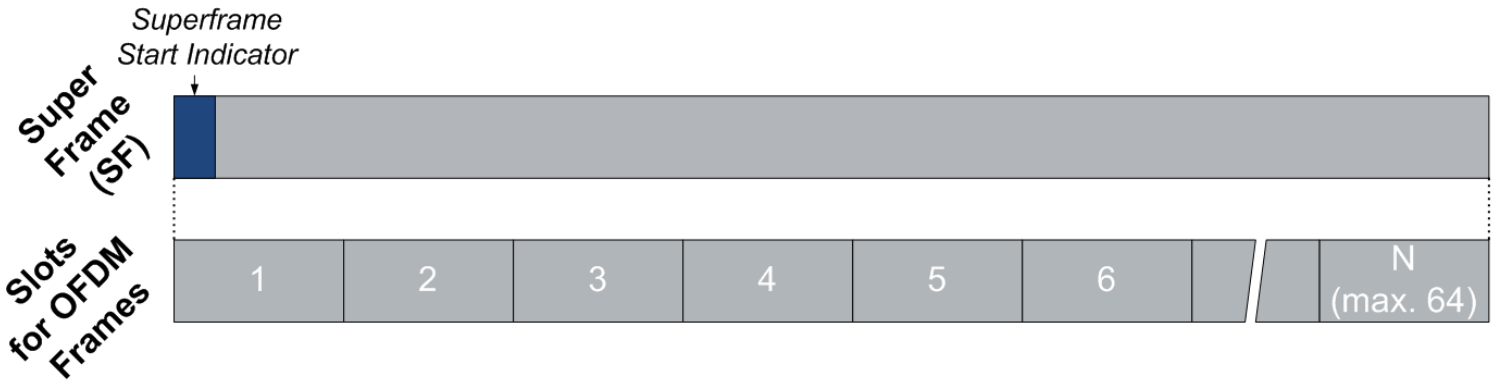
For Channel access of different users (UGV, UAV, base station)

Users are not equal: One master node to set the timing of the superframe

➡ must be visible to all users ➡ UAV

TDMA

For Channel access of different users (UGV, UAV, base station)



The more traffic a user requires, the more slots are reserved for him to transmit

TDMA

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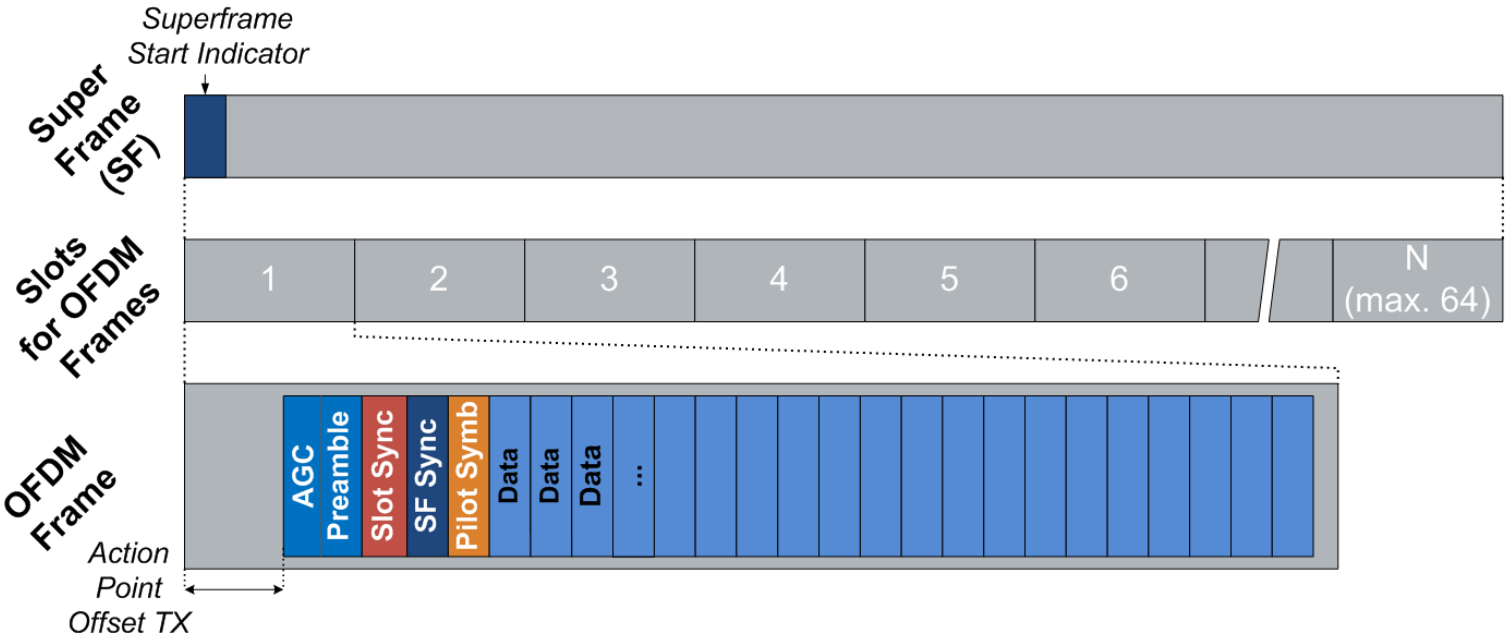

TDMA

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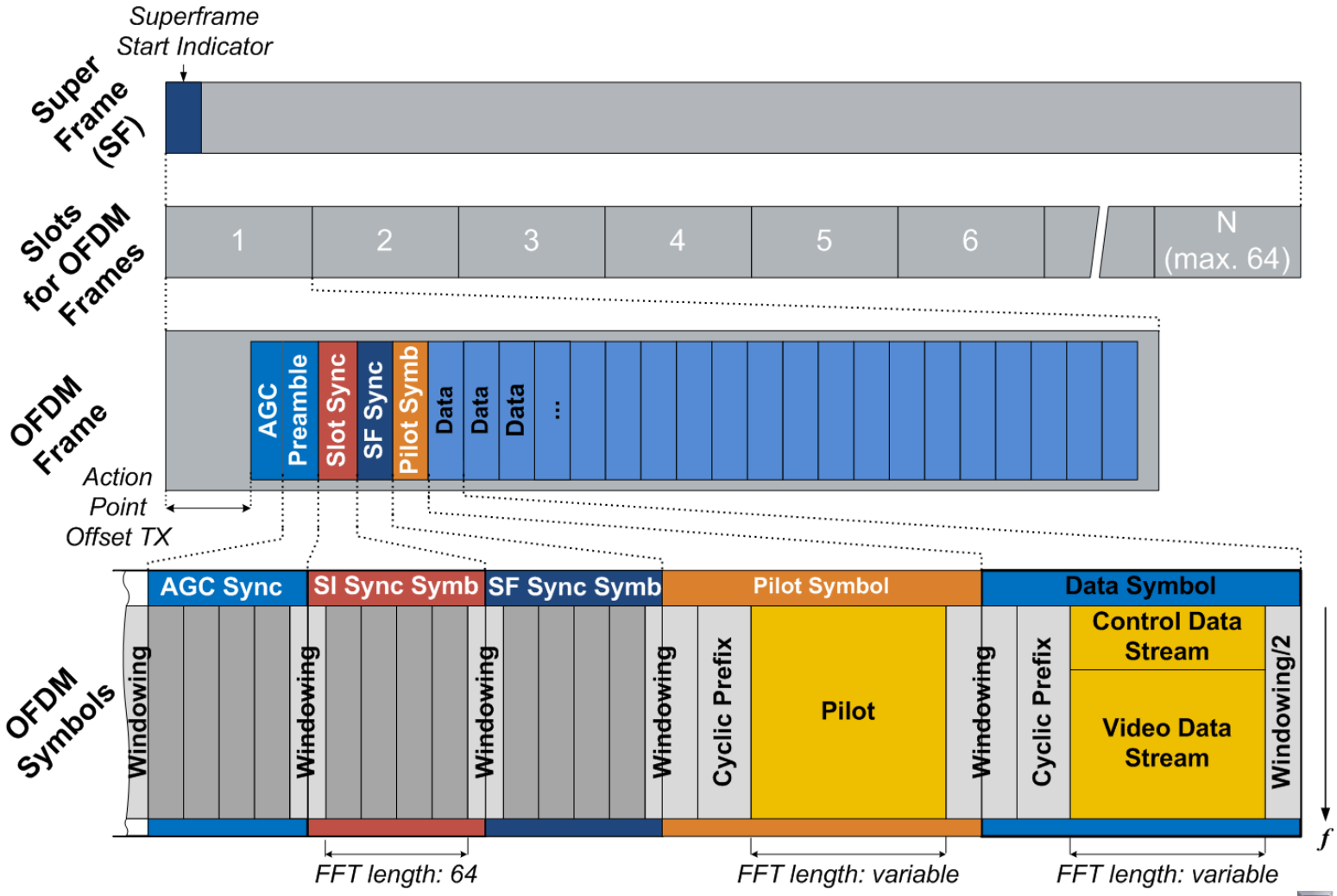

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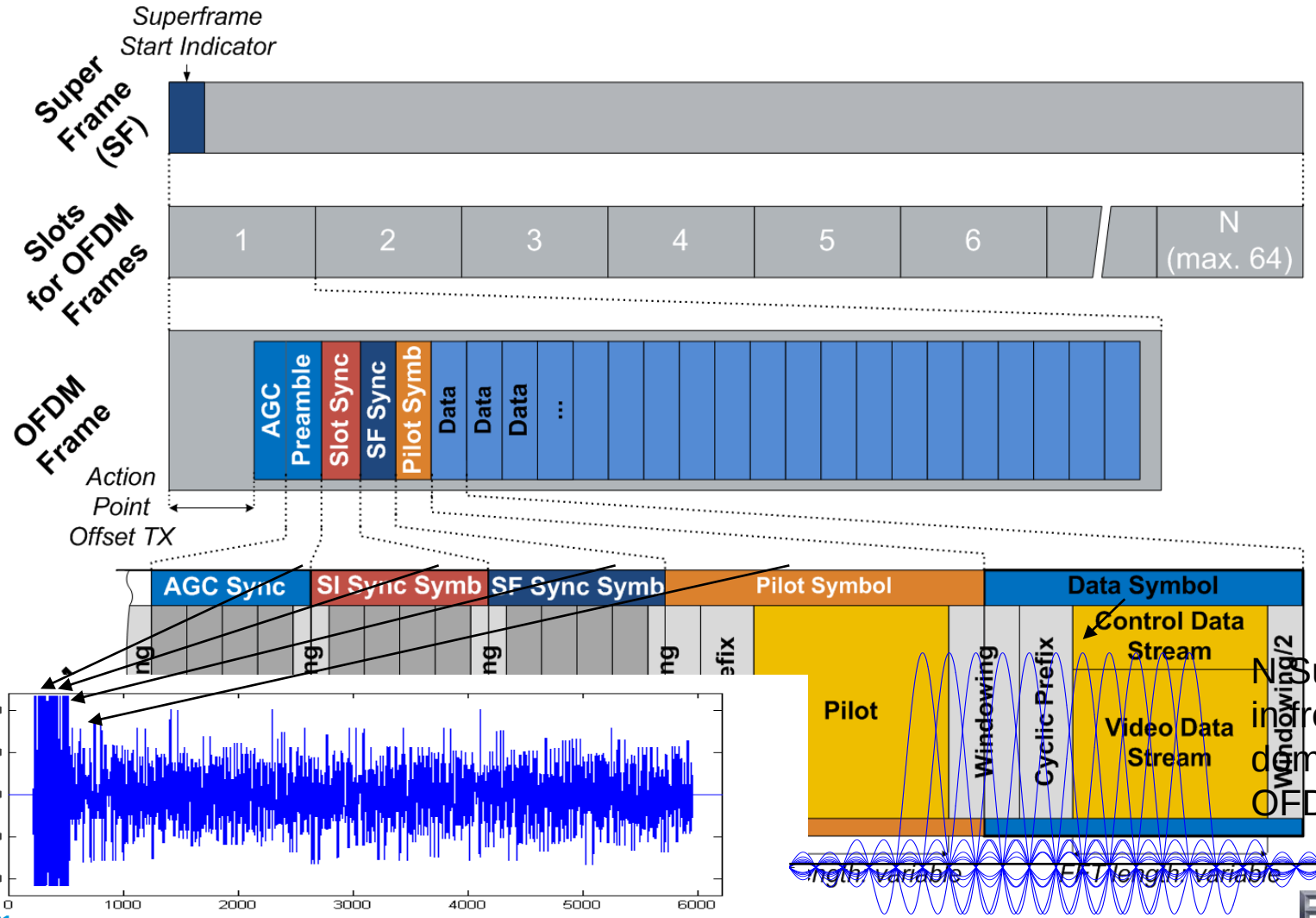

N Subcarriers in frequency domain for each OFDM Symbol

Designing and testing

1. **FPGA design**
   Hybrid approach of pure VHDL and a model driven design environment (MathWorks Matlab/Simulink including Xilinx System Generator)
   → allows at a very early stage elaborated simulations (e.g. with Simulink Rayleigh or Rician fading channel models)

2. **Hardware tests with fading simulator**
   Stressing the SDR platform in predefined environment with fading simulator R&S AMU200A
   → static and dynamic real-time fading scenarios, Doppler, AWGN noise, …)

3. **Open field tests**
   Final tests with UAVs (two types, maximum speed 120 km/h) and UGV (maximum speed 12 km/h)

Conclusion

Overview over an OFDM-based waveform, designed for communication links among autonomous robotic platforms

- communication focus: unidirectional video link between a UGV and its base station; established indirectly with an UAV as relay
  (+ further direct and indirect links for video and control data)
- Waveform supports separated logical links for video and control data concurrently
- Waveform offers outstanding flexibility according its parameters on runtime
- Hardware platform features very small form factor
- Hardware platform offers universal system interface (TCP/IP, UDP/IP)

Thank you for your attention!

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