Cascade Linear Phase Recursive Half-Band Filters Implement the Most Efficient Digital Down-Converter

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ABSTRACT

The digital down converter (DDC) is a fundamental component in modern receivers. Two different architectures, operating on very different principles, have become dominant in modern receiver systems. The first of these is the Edwin Armstrong heterodyne model formed by three processes, a quadrature heterodyne, a low-pass filter, and an M-to-1 down sampler. The second is the band centered polyphase filter in which the three processes are performed in the reverse order, an M-to-1 aliasing down sampler, an M-path partitioned low-pass filter, and an M-point complex phase-alignment vector. The second option finds great favor in multichannel receivers in which multiple narrowband signals are separated by the single filter coupled to an IFFT that provides the multiple M-point phase alignment vectors. In this paper we present a polyphase filter form of the single channel DDC that offers significant computational advantages over the conventional single channel DDC. This architecture may present the minimum power implementation of a DDC and likely will find great value in battery operated radio receivers.

1. INTRODUCTION

There are many ways of performing the task of a digital down converter. The DDC converts a real sampled data signal centered at an arbitrary intermediate frequency to a complex base band signal centered at zero frequency. The most common form of the DDC is based on Edwin Armstrong's heterodyne receiver. It contains three processes: a quadrature direct digital synthesizer (DDS) feeding a pair of multipliers that perform the desired spectral translation, a pair of sampled data low-pass filters that reduce the signal bandwidth, and a down sampling process that reduces the output sample rate in proportion to the filter bandwidth reduction. In modern receivers the filter is implemented in a multirate architecture that embeds the resampling process in the filtering process.

A ubiquitous resampling filter present in many systems is the K-stage cascade Integrator comb (CIC) or Hogenauer filter. This filter consists of K-digital integrator stages, an M-to-1 down sampler, and K-derivative stages. Figure 1 shows the evolution of the M-to-1 resampled K-stage boxcar integrator transfer function to separate numerator and denominator filters and their reordering by the noble identity to the Hogenauer partition with the comb filters at the input rate becoming derivative filters at the output rate. The attraction of this filter is that it performs the filtering and resampling without multipliers. In many systems the CIC performs an M/4-to-1 bandwidth and sample rate reduction followed by a pair of half band filters that correct for the CIC's main lobe spectral distortion and a final house cleaning filter to obtain a 4-to-1 bandwidth reduction and 4-to-1 down sampling. This is seen in Figure 2 which shows the form of the CIC based DDC as often seen in the Gray-chip family.

An important consideration often overlooked when comparing the CIC filter to other filtering options is the bit width of the registers in the CIC Integrators. The prototype M-to-1 resampling boxcar filter has a gain of M and of course a K-stage version of the boxcar filter has a gain of M^K. The registers in the integrators of the CIC, and in general the registers of the derivatives, must accommodate this gain. The number of bits required for the integrator registers is shown in eqn.(1) as the sum of the number of bits representing the input signal plus the number of bits to accommodate the K stages of gain. Specifically say we require 16 bit input samples processed by a 6-stage filter performing 1000-to-1 down sampling. Inserting these values in eqn.(1) we find that b_{accum}=16+60 =76 bits. There would be 6 integrators on each of the I and Q legs of the DDC for a total of twelve 76 bit registers operating at the input rate.

The total number of bits circulating in the CIC integrators would be 912 bits which is the equivalent to 57 16-bit words. Alternate DDC architectures that use less than 57 16-bit words at the input sample rate may be a better choice for the DDC than the CIC based version. When we include two multiplies required to implement the DDS I-Q conversion we have some 59 16 bit arithmetic operations.

$$b_{ACCUM} = b_{DATA} + \text{ceil}[\log_2(M^K)] \quad (1)$$

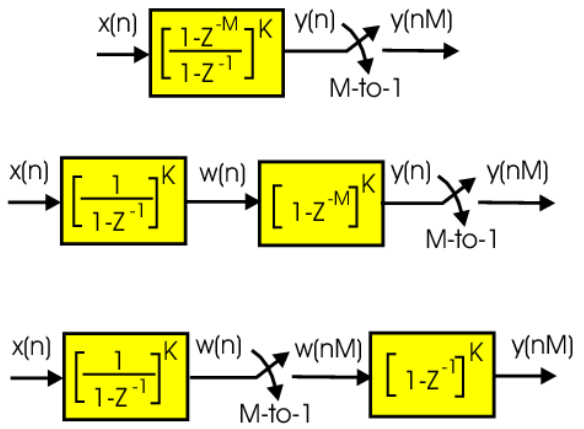

Figure 1. Successive Transformations of M-to-1 Down Sampling K-Stage Boxcar Integrator to Cascade Integrator Comb and then to Hogenauer Partition.

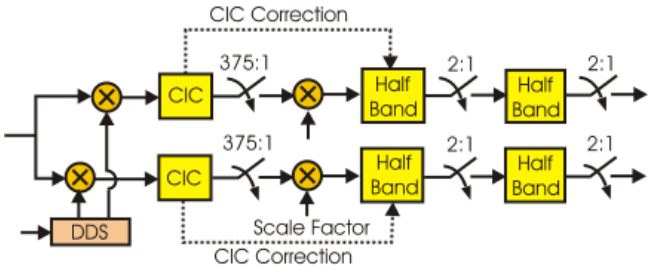

Figure 2. Digital Down Converter Containing Direct Digital Down Converter, M/4-to-1 Resampling CIC filter, One Half-Band Compensating Filter and One Half Band Clean-up FIR Filter.

1. ALTERNATE ARCHITECHURE

The design we present here replaces the resampling CIC filters with a cascade of 2-to-1 down sampling half band filters. A cascade of traditional true half band filters is very efficient because half the coefficients are zero and each successive filter in the chain operates at half the speed of the previous stage. What we propose here is a novel variant of the half band filter, namely a two-path recursive all-pass linear phase implementation. The form of this filter is shown in Figure 3. The core stages of this filter are shown in Figure 4. The transfer functions of these cores are first and second order polynomials in Z^2. Note the upper path is a pure delay line with linear phase. The lower path is designed to match the phase of the upper path in the pass band region and to differ from the upper path by π in the stop band region. Since the upper path is linear phase, the composite filter is also linear phase up to the pass band edge (as shown later in Figure 11). Since the polynomials forming the filter stages are polynomials in Z^2 we can invoke the noble identity and pull the 2-to-1 down sampler through the filter and perform the 2-to-1 down sampling at the input to the filter. When we do this, the polynomials in Z^2 become polynomials in Z. This transformation is shown in Figures 5 and 6. Figures 7, 8, and 9 present a ninth order version of this two path filter. Note this particular filter has only 4 coefficients for which the down sampling workload is remarkably only 2-multiplies per input sample.

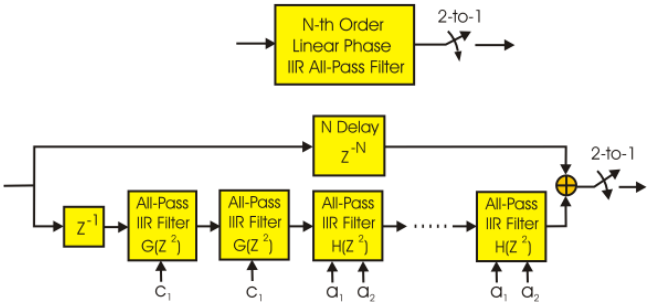

Figure 3. Two-Path, Half Band Linear Phase Filter.

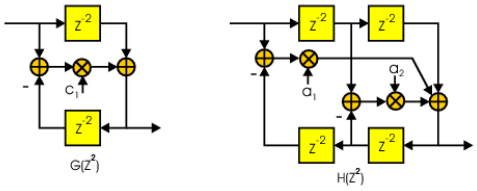

Figure 4. Recursive All-Pass First Order and Second Order Filters Formed by Polynomials in Z^2.

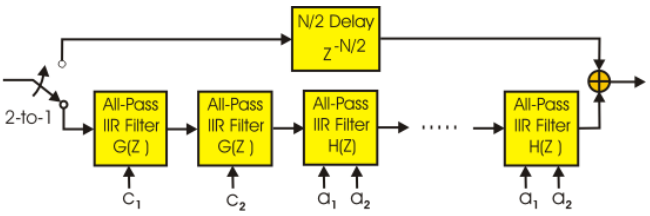

Figure 5. 2-to-1 Down Sampled Two-Path, Half Band Linear Phase Filter.

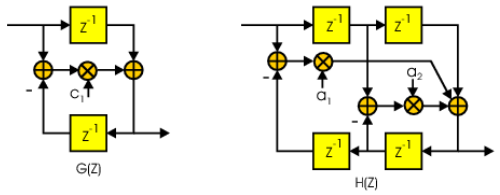

Figure 6. Recursive All-Pass First Order and Second Order Formed by Polynomials in Z.

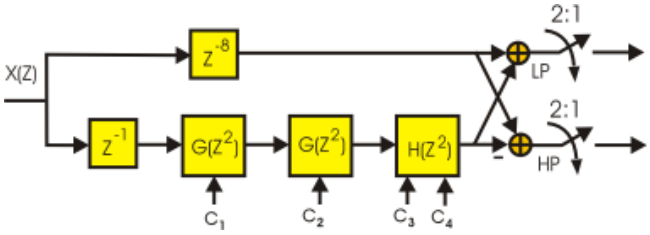

Figure 7. Ninth Order Two-Path, Half Band Linear Phase Filter.

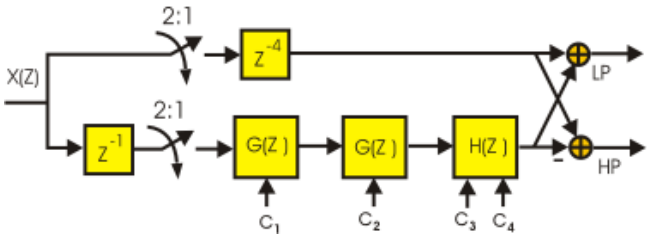

Figure 8. 2-to-1 Resampled Ninth Order Two-Path, Half Band Linear Phase Filter.

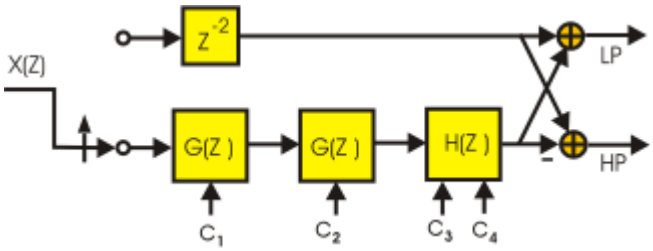

Figure 9. Commutator 2-to-1 Resampled Ninth Order Two-Path, Half Band Linear Phase Filter.

We will shortly have need for four versions of this half band filter that are centered on the four cardinal directions that are multiples of π/2. Using the notation of a 4-point DFT we will refer to these filters by their bin numbers, 0, 1, 2, & 3.The transfer function for the upper and lower arms, denoted TP and BT, of Figure 7 are shown in eqn.(2). We can perform the low-pass to band-pass transformation that converts the low-pass Bin-0 filter to the Hilbert transform Bin-1 filter by the substitution shown in eqn.(3). When this substitution is made in eqn.(2) we obtain eqn.(4) where we see the effect of the transformation is to reverse the polarity of the coefficients in the second order polynomials and to declare the bottom path to be the imaginary part of the complex impulse response. This is precisely what happens when the Hilbert transform filter is coupled with the upper path delay line to form the analytic signal filter. The pole zero diagrams of the Bin-0 and Bin-1 filters are shown in Figure 10. Figure 11 shows the group delay and frequency response of this simple half band filter. From the two lower subplots we note that the filter exhibits linear phase in its stop band interval and its complementary pass band interval. For this design, these intervals are 25.64% of the normalized frequency axis. The pass band of the filters extends 0.64% beyond the 25% point where adjacent filters overlap. This 0.64% overlap is required to have a signal located at the crossover boundary be in one of the four filters. As the sample rate is lowered by the succession of half band filters, the overlap region must increase as the signal bandwidth of interest occupies a larger fraction of the sample rate. The DDC system for which this design was performed extracted a single 20 kHz bandwidth signal from a 100 MHz sample rate. This bandwidth is one part in 5000 and at the end of 10 half-band filter chain. The filters required to accomplish this task use 4-coefficients for filters 1-through 6, use 5-coefficients for filters7-through 9, and use7-coefficients for filter 10.

$$TP_1(Z) = \frac{1}{Z^8}$$
$$BT_1(Z) = \frac{1}{Z}\frac{1+c_1Z^2}{Z^2+c_1}\frac{1+c_2Z^2}{Z^2+c_2}\frac{1+c_3Z^2+c_4Z^4}{Z^4+c_3Z^2+c_4} \quad (2)$$

$$Z^{-1} \Rightarrow jZ^{-1}$$
$$Z^{-2} \Rightarrow -Z^{-2} \quad (3)$$

$$TP_2(Z) = \frac{1}{Z^8}$$
$$BT_2(Z) = \frac{j}{Z}\frac{1-c_1Z^2}{Z^2-c_1}\frac{1-c_2Z^2}{Z^2-c_2}\frac{1-c_3Z^2+c_4Z^4}{Z^4-c_3Z^2+c_4} \quad (4)$$

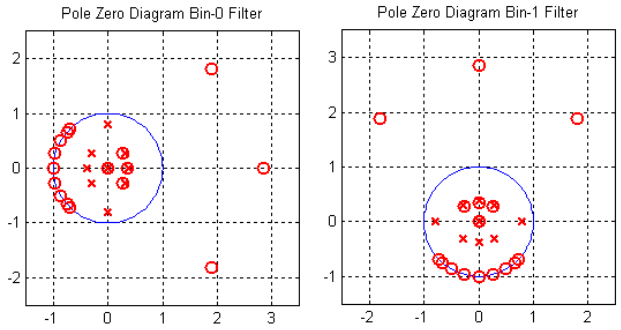

Figure 10. Pole-Zero Diagrams for Half-Band Bin-0 and Half-Band Bin-1 Filters.

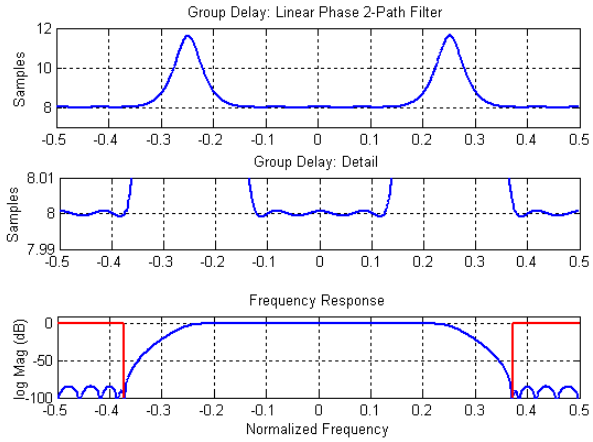

Figure 11. Group Delay, Zoom to Group Delay Detail and Frequency Response of Half-Band Filter.

The first improved option for the DDC has us replacing the CIC filter with the cascade of recursive half band filters as shown in Figure 12. Remember that when delivering 2-inputs to compute 1-output, the workload per input sample to the first filter is 1 multiply per input and the workload per input sample to the next filter is also 1 multiply per input but occurs at half the rate so the workload for the next stage referenced to the input stage is 1/2 multiply per input sample. Following this reasoning, the workload for the cascade chain per path is shown in eqn.(5). Here we see that, for a ten stages cascade, the workload per path is approximately 3. multiplies per input sample. Thus the workload of the I-Q filter chains is approximately 6 multiplies per input sample. Note that the coefficients in the filter are fixed and they can be implemented with simple logic rather than with full Booth multipliers. If we include the I-Q quadrature mixing, the entire DDS requires only 8-multiplies per input sample. This is a significant improvement over the CIC's 59 equivalent arithmetic operations.

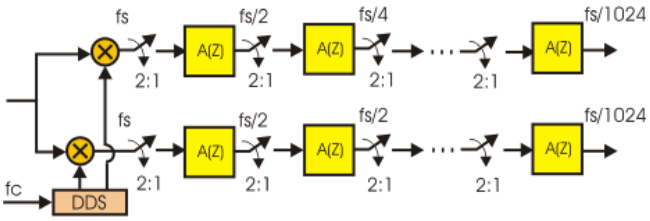

Figure 12. Digital Down Converter with Cascade Recursive Half-Band Low-Pass Linear Phase Filters

$$W = \left(1+\frac{2}{2}+\frac{2}{2^2}+\frac{2}{2^3}+\frac{2}{2^4}+\frac{2}{2^5}+\frac{2.5}{2^6}+\frac{2.5}{2^7}+\frac{2.5}{2^8}+\frac{3.5}{2^9}\right) \quad (5)$$
$$= 3.01$$

2. IMPROVED ALTERNATE ARCHITECTURE

A improved second option for the DDC has us moving the DDS from the input of the cascade half band filter chain to its output. When operated at the low output rate, its contribution to the workload is insignificant. To accomplish this shift we have to modify the half-band filters. The modification is trivial only requiring sign changes in the two path filters. At each location in the half band chain, the half band filter has to be selected from one of 4-possible half band filter options. As commented upon earlier, the four filters are centered at the four cardinal directions or phases, 0, $\pi/2$, $2\pi/2$, and $3\pi/2$ which we labeled as bins 0, 1, 2, & 3 successively. In the architecture of Figure 13, every possible input center frequency is associated with a unique succession of nine sets of phase selections presented to each stage by the channel selector. The selection process proceeds in the following manner. We note that due to the effect of the sample rate halving, at each stage the relative position of the selected signal center frequency is aliased or doubled when normalized to the new output sample rate. As an example, we track the four successive locations of a signal initially located at normalized input frequency of 0.1 which places it in the bin-0 filter (-0.125 to +0.125) of the four possible filters. The effect of the upcoming successive alias shifts due 2-to-1 resampling is illustrated in Figure 13. After the first half-band filter and 2-to-1 down sample it has aliased to the normalized frequency 0.2 which places it in the Bin-1 filter (+0.125 to +0.375). Following the second half band filter and 2-to-1 down sample it has aliased to 0.4 which is in the Bin-2 filter (+0.375 to +0.625). The third half band filter and 2-to-1 down sample places it at 0.8 or at -0.2 which is in Bin-3 (+0.6255 to +0.875). A fourth half-band filter and 2-to-1 down sample places it at 1.6 or 0.6 or -0.4 modulo(1) which is back to Bin-2 (+0.375 to +0.625). At the end of the sequence of 2-to-1 down sample aliasing

and half band filter the signal of interest will reside at some offset centered location. In the example just cited, the final center frequency is -0.4 at sample rate $f_S/16$. A final heterodyne at this output rate, as show in Figure 13, shifts the center of the final aliased band back to zero frequency.

Forming the four bin filters from a single prototype half band filter is a simple matter of changing the sign of two adders. The first adder performs the sum or difference of the two paths as shown in Figure 9. Here we see that the sum of the two paths forms the low-pass filter, the Bin 0 output and that the difference of the paths forms the high pass filter, the Bin-2 output. The second sign change was described earlier as coefficient sign change resulting from the low-pass to band pass transformation of eq(2). The easiest place to effect the sign change is at the left most adder in the transfer function G(Z) shown in Figure 6.

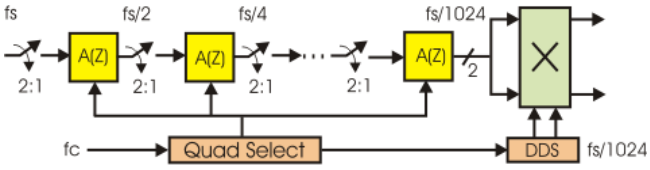

Figure 13. Digital Down Converter with Cascade Recursive Half-Band Four-Bin Linear Phase Filters.

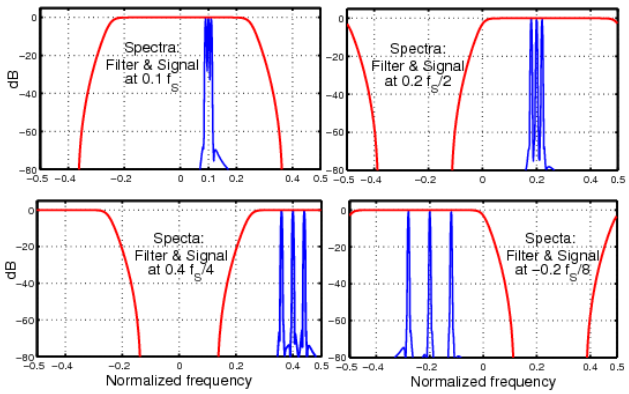

Figure 14. Spectra of Signal Aliased to Different Sampled Data Frequencies in Successive 2-to-1 Sample rate Reductions.

3. CONCLUSION

The DDC filter structure shown in Figure 12 is a very efficient technique to reduce bandwidth and sample rate. It performs a base banding operation and 1000-to-1 down sampling with approximately 8 arithmetic operations per real input sample. Two of these operations are the quadrature mixing at the input to the filter chain. In the DDC filter structure shown in Figure 13 the quadrature mixing is moved to the output of the filter chain where its contribution to the workload is insignificant so that the workload drops to approximately 6 arithmetic operations per real input sample. These workload numbers compare quite favorably with the CIC work load of nearly 59 real arithmetic operations per input sample distributed over the quadrature heterodyne and the very wide bit width of the many input integrators.

We finally note that the dual of the two process presented here will form a digital up converter (DUC) with the same computationally efficient work load, a work load nearly an order of magnitude smaller than the traditional CIC based DUC.

4. REFERENCES:

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