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A TUNABLE WIDEBAND RF FRONT-END FOR SDR

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ABSTRACT

Today's direct-conversion SDR platforms are capable of tuning over extremely wide frequency ranges compared to traditional superheterodyne transceiver architectures. However, these radios can suffer from a number of problems due to a lack of front-end RF filtering, including poor dynamic range and desensitization. In this paper, we examine preliminary work on a tunable bandpass filter we are designing to mitigate this problem. The filter is electrically tunable and can be adjusted to cover a carrier frequency range of over two to one with Q on the order of 4.

1. INTRODUCTION

It is said that history repeats itself, and radio transceiver design is no exception. Today's direct-conversion radios bear a striking resemblance to the heterodyne and homodyne transceivers first developed in the early twentieth century [1]. These designs existed years before Armstrong and others invented the now-ubiquitous superheterodyne receiver architecture [2], and researchers are now revisiting radio's roots in an effort to improve performance. The difference is that the parts available today offer performance orders of magnitude better than those available in the late nineteenth century. Many components on the market offer very high sensitivity and operate from nearly DC to microwave frequencies.

Superheterodyne receivers generally work very well in adverse conditions, but they suffer from the image frequency problem. This occurs when a signal is present at $f_{LO} - f_{IF}$, where the RF signal is at $f_{LO} + f_{IF}$. Both signals will be converted to the same IF due to basic trigonometric rules. The problem can be mitigated if a bandpass filter is chosen with a bandwidth less than twice that of the IF, so as to exclude the image frequency from the passband.

By converting directly to baseband, direct conversion receivers avoid the image frequency problem (because f_{IF} is essentially 0 Hz) and thus can offer much wider tuning ranges. However, this means that the mixer must be able to see the full spectrum of potentially tunable signals, and it greatly increases the odds that a receiver will be overloaded.

Placing a bandpass filter prior to the receiver to narrow the spectrum can mitigate this problem. In this paper, we discuss our work on the design of an electrically tunable bandpass filter for SDR applications to mitigate the overload problem. The filter is designed to operate over a two to one bandwidth. In addition, the filter is designed with standard electronic components that are inexpensive and readily available, unlike more exotic filter technologies.

The rest of this paper is organized as follows. In section 2, we describe our filter and the design process. In section 3 we examine our preliminary results and problems encountered, and in section 4 we look at areas of improvement and future work. Finally, in section 5 we offer our conclusions.

2. A DESIGN FOR A FREQUENCY AGILE BANDPASS FILTER

Filter design has been studied in great detail, and countless texts, papers, and documents have been written on the topic. However, little attention has been paid to discrete, electrically tunable filters in the literature. Almost all textbook designs are for fixed-frequency filter design. In the present case, we are not only interested in an electrically tunable filter but one that has a relatively narrow bandwidth at very- and ultra-high frequencies. In this section, we describe the development of a filter that meets these criteria.

2.1. Background

Resonance occurs when there is equal capacitive and inductive reactance present in a circuit. While inductive reactance has generally proven to be difficult to tune electrically, capacitance can be easily changed with a varactor diode. Varactor diodes also have the benefit of being very inexpensive electronic components.

When varactor diodes are placed into a reverse bias condition, the capacitance located at their junction changes as a function of the applied reverse bias voltage [3]. This property allows us to tune a resonant circuit to a desired center frequency with a simple DC voltage signal.

One of the primary goals of our work is to produce an inexpensive filter design. This is accomplished by using readily available surface-mount components, which narrows our choice of filter topology (for instance, filters designed to be integrated onto a chip are not appropriate). In this paper, we present extensive simulation results for a series of capacitively coupled shunt resonators. This design exhibits a relatively narrowband response and has fewer components than other designs [4].

In many circuit designs, impedance matching can be effected with a tapped coil. More commonly known as an autotransformer, the tapped coil transforms the low terminal impedance up to the impedance of the circuit [5]. However, such a method is not practical for this application because it

cannot be electrically controlled. Hence, instead of feeding the circuit with the inductor, we divided the shunt capacitor into two series devices, permitting us to electrically tune the input impedance of the circuit as needed to improve coupling into and out of the filter.

2.2. Filter Topology and Schematic

Figure 1 shows a simplified schematic of the filter. There are four tunable capacitors in the form of varactor diodes D1-D4, two shunt inductors L1 and L2, and series inductors (L3 and L5) at the ports that act as low pass filters. The filter is symmetric about the vertical axis, and each half of the circuit forms a resonant "tank" circuit. The two series varactor diodes serve as the primary means to tune the circuit. By adjusting the values of these elements, we can vary the passband frequency of the circuit over a range of nearly 2:1, and also vary the input impedance to match our source and load impedances.

The series input inductors serve to attenuate high frequency oscillations within the circuit that are a result of package and parasitic reactance from each component.

2.3. Component Selection

In order to most accurately model the filter circuit, it is necessary to select real-world components and use their SPICE models in the circuit simulation. This will help account for parasitic reactance from packaging, and also for loss within the device.

We examined a variety of varactor diodes available on the market, and selected the Skyworks SMV1251 for this project. This diode offers a tuning range from approximately 38 pF at a bias voltage of 0.5V to 3.5 pF at 5.0V. The diode comes in a SOD-323 package, which measures 54 mil wide by 70 mil long, and the package inductance is approximately 1.5 nH. Resistive losses are specified at approximately 1.4 Ohms [6].

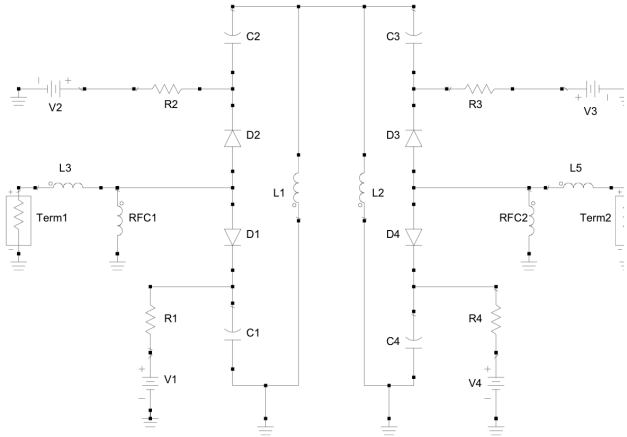

Figure 1. Simplified schematic of the tunable bandpass filter.

We selected the Coilcraft 0402HP line of inductors for the inductors in this project. These devices measure 40 mil by 20 mil, and offer very low loss and parasitic capacitance [7]. These characteristics make them ideal for filter applications.

2.4. Tuning the Filter

The filter is designed to be tuned by a cognitive radio engine. While it is possible to tune the filter by way of a direct transfer function, this is prohibitive in practice due to the complex circuit models that must be employed for each component used in the circuit.

Tuning is most easily accomplished by adjusting the values of the four capacitors, exciting the circuit with a signal at the desired frequency, and measuring the input and output power of the circuit. The capacitor values are set by adjusting the bias voltage across the varactor diodes, and this can be achieved by way of a microcontroller or digital-to-analog converter. The input and output power levels can be measured with a small directional coupler connected to an analog-to-digital converter.

The center frequency of the filter is set by adjusting D2 and D3, and the bandwidth and matching is set by adjusting D1 and D4. The process is repeated until the center frequency, bandwidth, and network loss comes within predetermined parameters.

3. PRELIMINARY RESULTS

Early simulations of our filter design have proven to be very promising. We have extensively simulated the performance of a filter designed to cover the range from 137 MHz through 300 MHz, and will discuss our findings below.

3.1. Frequency Response

Figure 2 shows a plot of the frequency response of the filter tuned to three different center frequencies ranging from 158 MHz to 326 MHz. Figure 3 shows plot of the reflected power at the input to the filter. At 158 MHz, the predicted insertion loss is approximately 2 dB, and the return loss 18 dB. This indicates that 1.5% of the incident power on the filter is reflected due to an impedance mismatch, and 63% is transmitted through the filter. The remaining 35% is lost due to resistive losses within the filter. Performance at higher frequencies is slightly worse, however our simulations have shown that by using a smaller inductor, the center frequency of the filter can simply be shifted up with minimal additional resistive losses.

3.2. Low Power Time-Domain Response

In Figure 4, the filter is tuned to a center frequency of 158 MHz. It is then fed with signals at 158 MHz, 400 MHz, and 1 GHz, and output voltage is plotted. The open circuit generator voltage is set for a peak amplitude of 20 mV in all cases. Figure 7 shows the frequency content of the output signal for the 158 MHz case, which is very clean. Harmonics are not immediately apparent in the plot.

Figures 5 and 8 show a similar plot, but the filter is tuned to 244 MHz in this case. Finally, Figures 6 and 9 show the same set of plots, with the filter tuned to 326 MHz. In both of these cases, the output spectrum indicates no harmonic content. It is worth noting that the small humps below the fundamental frequency are from the transient startup response of the filter.

3.3. High Power Time-Domain Response

Figures 10-15 show the same information as Figures 4-9, except in this case the open circuit generator voltage was increased to 1 V pk. This is a very powerful RF signal for a receiver, corresponding to 5 mW into 50 Ohms. In this case, the frequency spectrum indicates some harmonic content, though it is better than 20 dB below the fundamental frequency.

3.4. Intermodulation/IM3 Performance

Figure 16 shows the result of a two-tone test. The two-tone test is used to determine the susceptibility of an RF circuit to intermodulation distortion. We excited the filter about the center frequency of 158 MHz with two tones separated by 20 MHz. Both signals have an equal open circuit amplitude of 0.5 V_{pk}. As the plot shows, the second harmonic of the signals is visible, but no visible intermodulation products are visible.

3.5. Sensitivity to Diode Bias Conditions

Finally, we sought to determine how the circuit would behave if the diodes were driven into forward conduction. We excited the circuit with an open circuit voltage of 2 V_{pk} at 158 MHz and plotted the transient and spectral response. As the plots show, this does result in significant harmonic content visible out to nearly 3 GHz.

There remains a significant amount of work to be done on this project. Major tasks remaining include designing filters for higher frequency bands up to 3 GHz, integrating the filters and designing control circuitry and adding a power amplifier for transmit along with transmit/receive circuitry. Once these tasks are complete, we must lay out a printed circuit board, fabricate it, and populate and test the board to determine if the filter performs similarly to the simulations.

4. IMPROVEMENT AND FUTURE WORK

4.1. Completion of the Filter Set

While this paper only presents data from one filter section that was completed in the spring of 2011, we have since revised the filter circuit and designed a suite of filters to covers from 100 MHz to 3 GHz.

The final filter design completed in the summer of 2011 differs significantly from the design presented in this paper. The new filters are composed of three series resonators which are inductively coupled with shunt inductors. We found that this new design offered the best compromise of tunability, bandwidth, loss, and cost. A 12-bit digital-to-analog converter controls the filters.

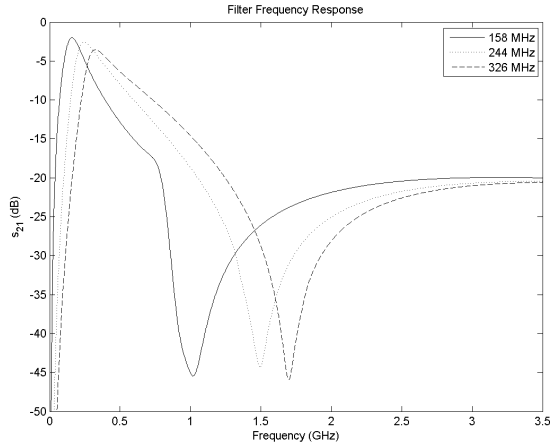

Figure 2. Frequency response of the filter at various settings.

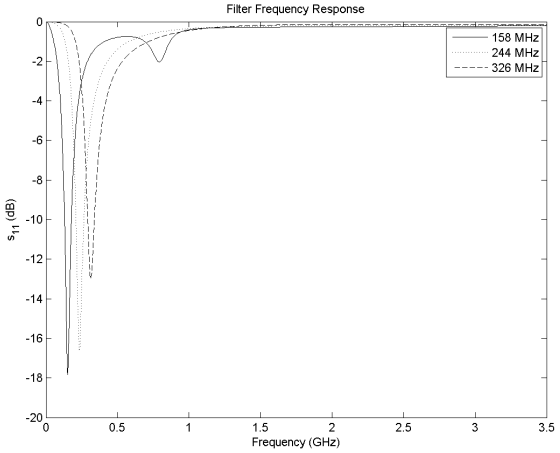

Figure 3. Return loss of the filter at various settings.

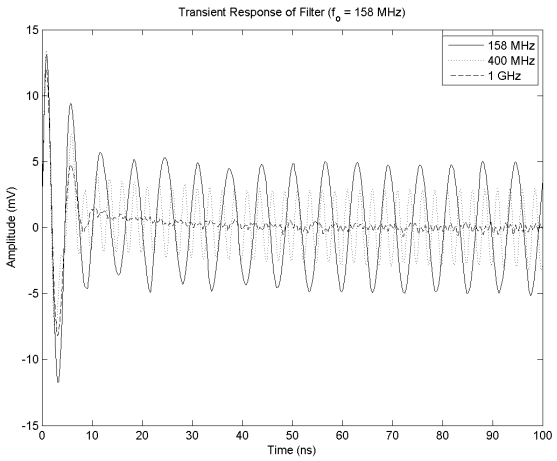

Figure 4. Transient response of the filter, with the center frequency set to 158 MHz.

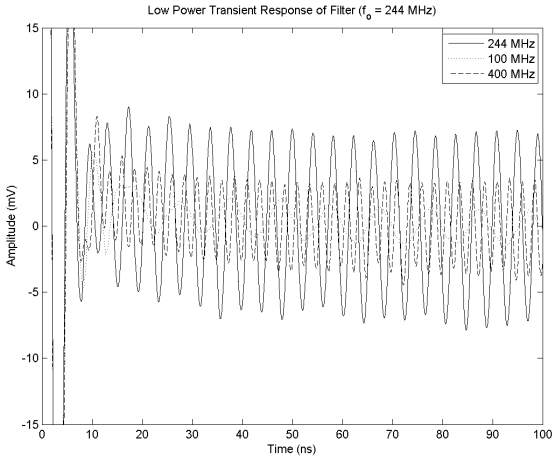

Figure 5. Transient response of the filter, with the center frequency set to 244 MHz.

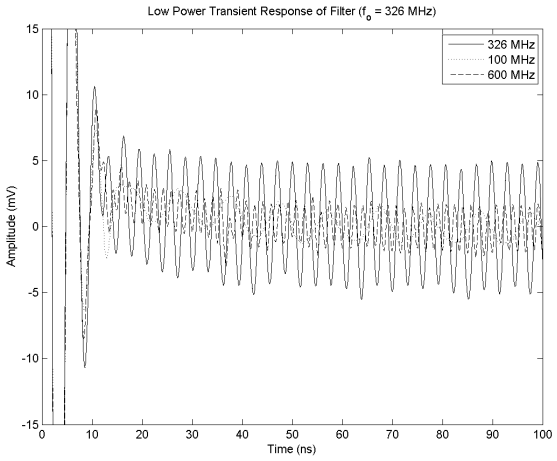

Figure 6. Transient response of the filter, with the center frequency set to 326 MHz.

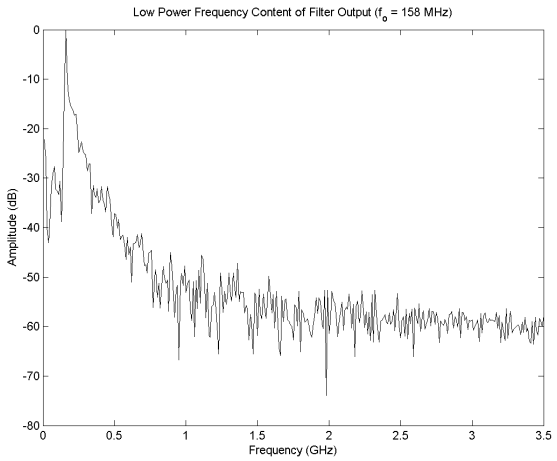

Figure 7. Spectral response of the filter, with the center frequency set to 158 MHz.

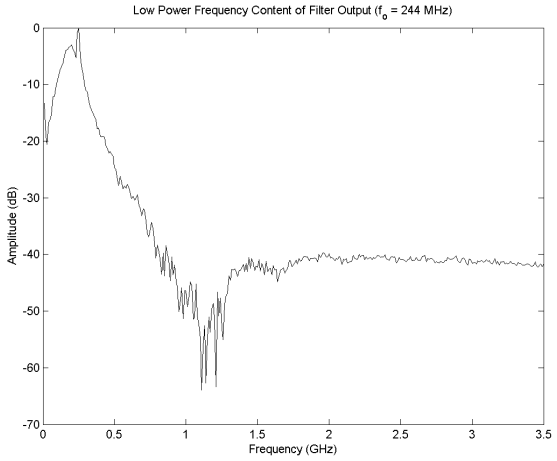

Figure 8. Spectral response of the filter, with the center frequency set to 244 MHz.

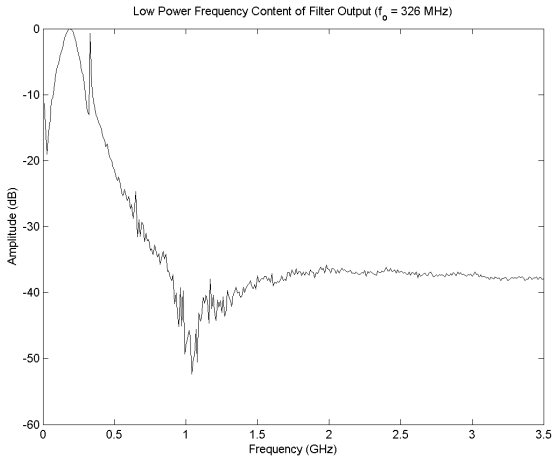

Figure 9. Spectral response of the filter, with the center frequency set to 326 MHz.

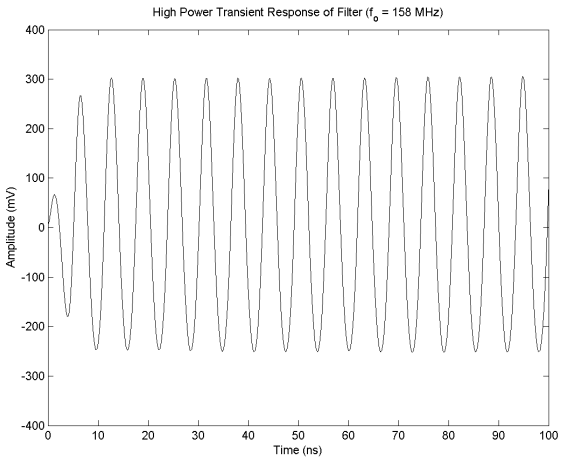

Figure 10. Higher power transient response of the filter, with the center frequency set to 158 MHz.

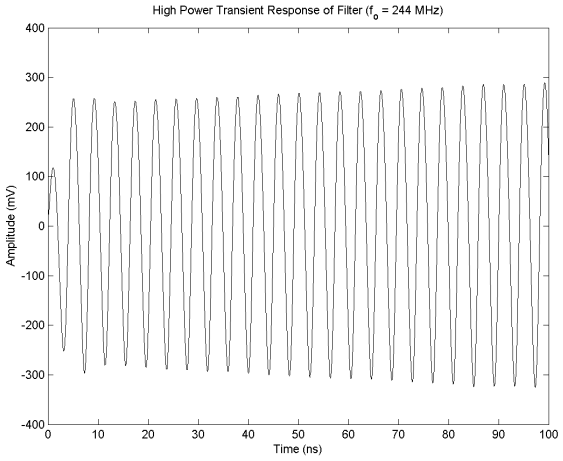

Figure 11. Higher power transient response of the filter, with the center frequency set to 244 MHz.

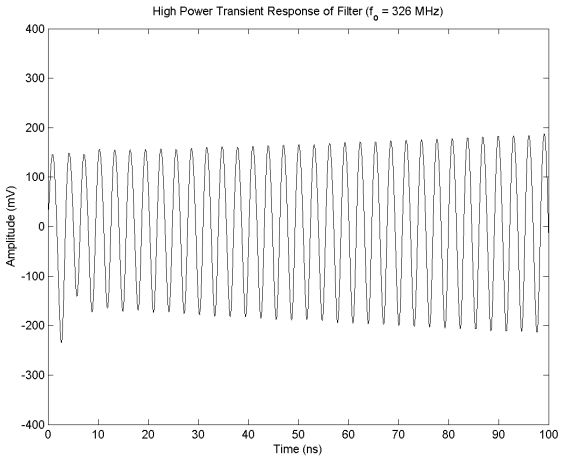

Figure 12. Higher power transient response of the filter, with the center frequency set to 326 MHz.

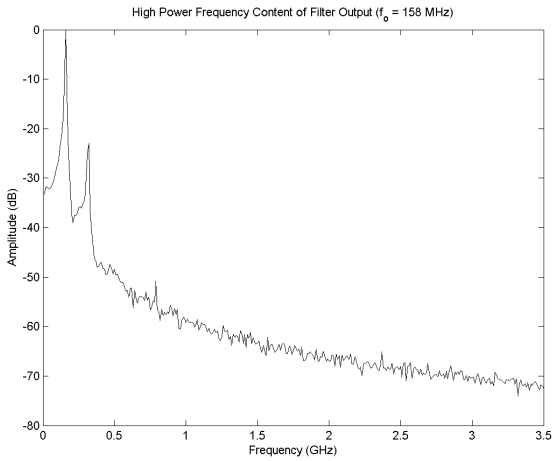

Figure 13. Higher power spectral response of the filter, with the center frequency set to 158 MHz.

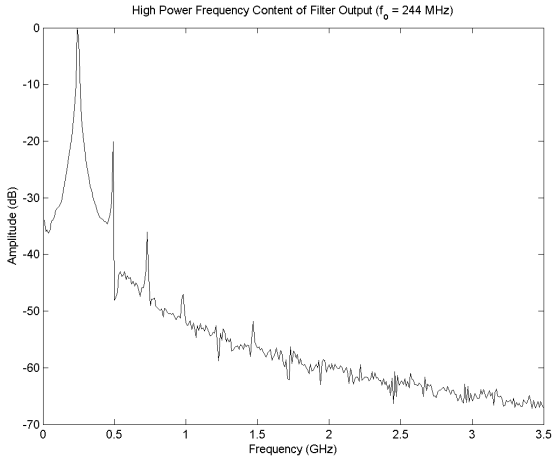

Figure 14. Higher power spectral response of the filter, with the center frequency set to 244 MHz.

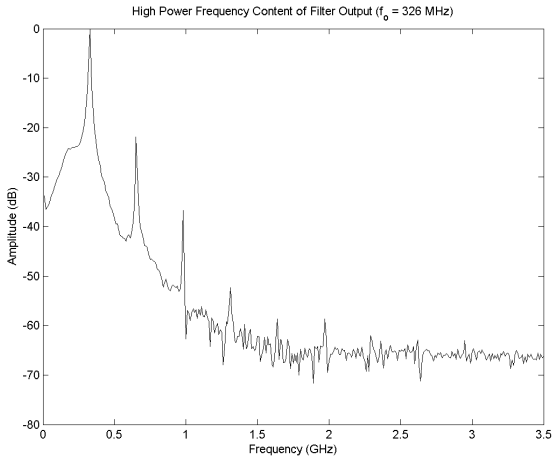

Figure 15. Higher power transient response of the filter, with the center frequency set to 326 MHz.

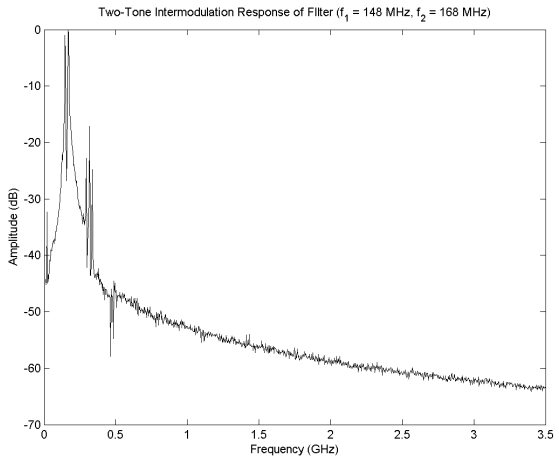

Figure 16. Two-Tone intermodulation test for a filter tuned to 158 MHz. Input frequencies are 148 MHz and 168 MHz.

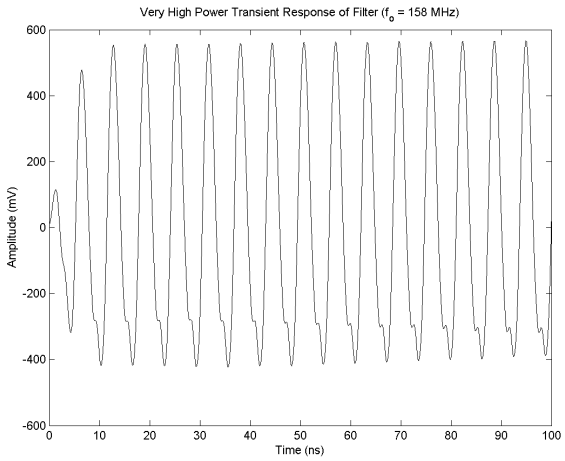

Figure 17. Transient response of the filter with the diodes driven into forward conduction.

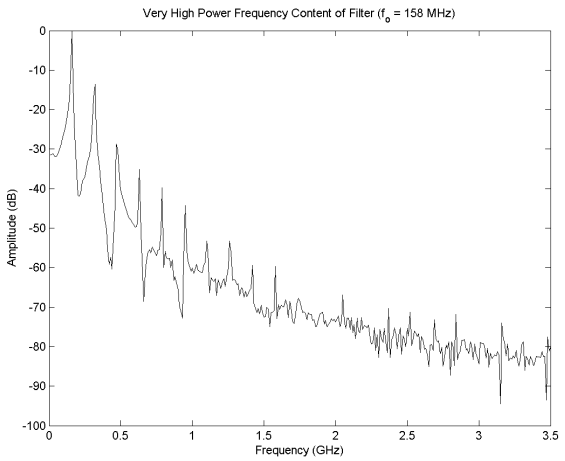

Figure 18. Spectral response of the filter with the diodes driven into forward conduction.

4.2 Physical Testing

After the filter boards have been fabricated and returned to us, it will be necessary to perform a series of tests to confirm our simulated results. We will examine tuning bandwidth, Q, loss, group delay, and power handling capability to fully characterize the filter system.

5. CONCLUSION

In this paper, we have discussed the development of a wideband, frequency agile front-end filter for SDR applications. The filter will help improve receiver performance by providing a tunable bandpass filter prior to downconversion and digitization, reducing desensitization due to strong out-of-band signals. We simulated a sample filter for the band between 150 MHz and 330 MHz, and examined in detail its performance in a number of areas. Finally, we discussed the work needed to build and characterize a final version of the device.

6. REFERENCES

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