Algorithm-Architecture Co-Design for Efficient SDR Signal Processing

Min Li, limin@imec.be
Wireless Research, IMEC

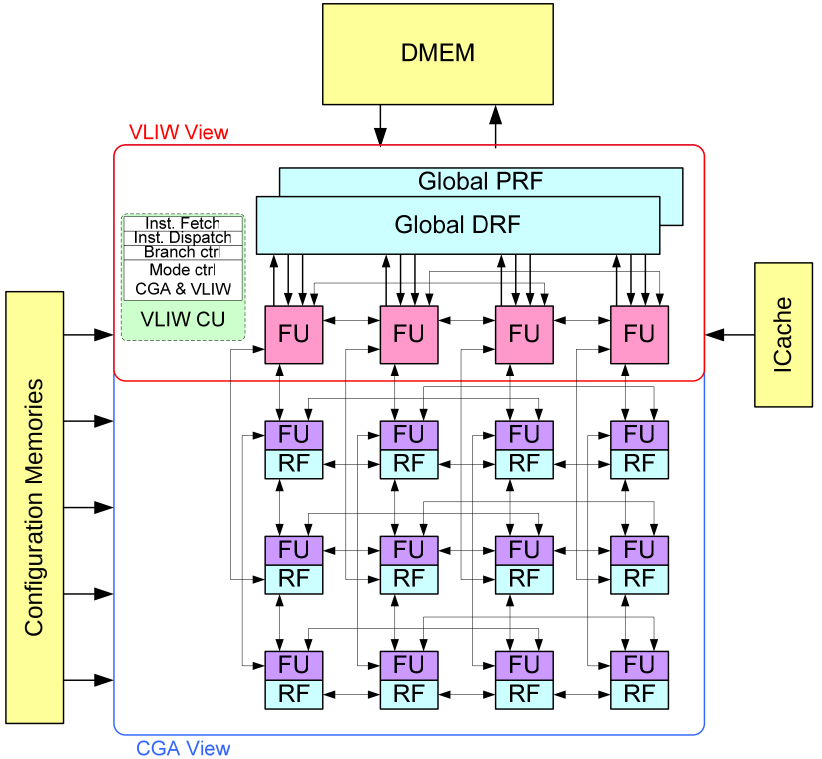
Introduction

SDR Baseband Platforms Today are Usually Based on ILP + DLP + MP

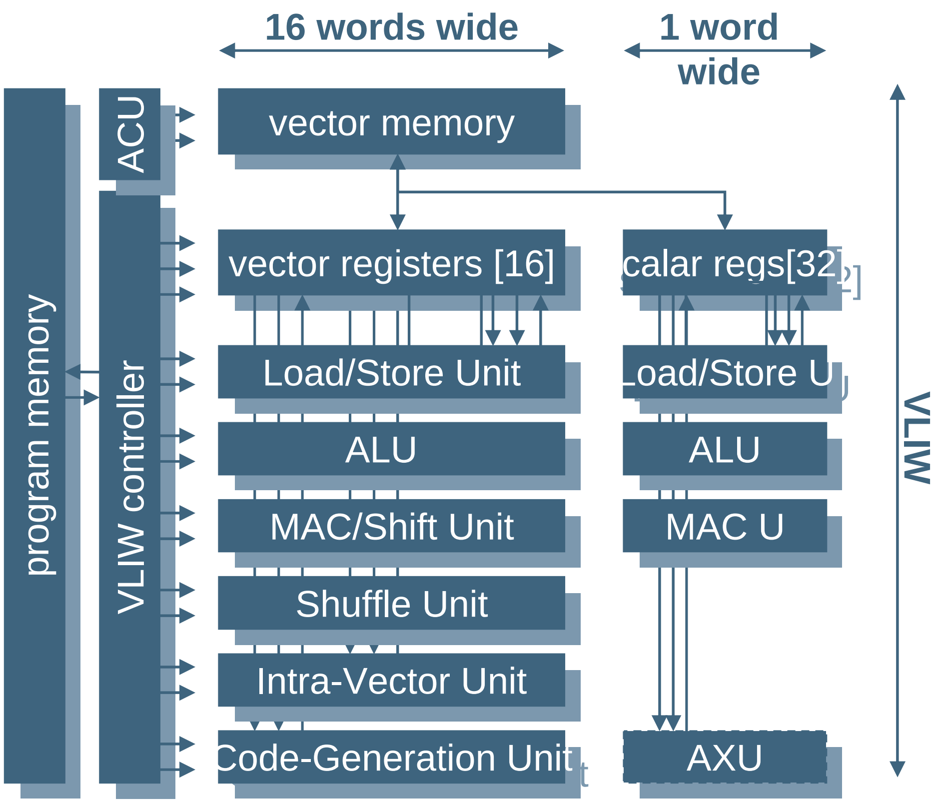
- Massive parallel SDR Baseband platforms with
  - ILP: Instruction Level Parallelism
  - DLP: Data Level Parallelism
  - MP: Multiprocessor
- Typical examples:
  - Infineon MUSIC platform, UMICH SODA, Linkoping/CORSONICS BBP2, IMEC BEAR for flexible air interface
  - ....

ILP+DLP+MP SDR Platforms Can POTENTIALLY Support Advanced Baseband Signal Processing

IMEC ADRES



NXP EVP



ILP+DLP+MP SDR Baseband Implementations Are VERY PREMATURE Today

- Usually the SIMPLEST receiver algorithms are implemented
- The throughput is much lower than ASICs
  – SODA: WCDMA and 11a, maximum 24Mbps
  – LIU/CORSONICS BBP2: WiMAX, 31.67Mbps
- The power consumption is not good enough
  – SODA: 0.5w with 90nm
- NOT comparable with ASIC counterparts
  – Power, communication performance, throughput

Exciting Challenge: from Basic Mobile SDR Baseband to ADVANCED Mobile SDR Baseband

Entering mobile market

Yesterday	Today	Tomorrow
SDR baseband for **military** and **infrastructure** application	BASIC SDR baseband for **mobile**	Energy efficient ADVANCED SDR baseband for **mobile**

Algorithm-Architecture Co-Design of Advanced SDR Baseband

- Pushing only from architecture/compiler side is not enough
- A strong platform aware algorithmic thrust is highly desired as well

PLATFORM-AWARENESS is Very Important When Designing SDR Baseband

Platform 1 in Roman Army

Platform 2 in Roman Army

Analysis of ILP + DLP Programmable Arch.
Constraints, Advantages and Disadvantages

- Constraints: architectures and associated compilers requires well-fit algorithms and codes
  - Many advanced algorithms are originally difficult to map/implement, such as various sphere decoders
- Disadvantages: lower power-efficiency
  - GOPS/mW is worse than ASIC
- Super advantages: multiplexing of data-path and memory is much easier on ASIP
  - Heterogeneous and flexible implementations are easier on ASIP

2 Principles for The Co-Design of Advanced SDR Baseband Systems

- Principle #1: Well matched algorithms and architectures/compiler
  - Algorithms need to be compatible with the constraints imposed by the architecture and associated compiler
  - Fine-tuning of the architecture, such as application specific instructions
- Principle #2: highly flexible system with energy awareness
  - Exploit the advantages of SDR baseband platforms

Case Studies: Major Components in MIMO-OFDM/OFMDA and CDMA Transceivers

- MIMO
  - Sphere detector, soft-output sphere detector and so on
- OFDM/OFDMA
  - Channel estimator, modulator/demodulator, synchronizer and so on
- CDMA
  - Equalizer and so on
- Generic blocks
  - Partial FFT, matched filter, FEC and so on

Enhancing The Friendliness between Algorithm and Architecture

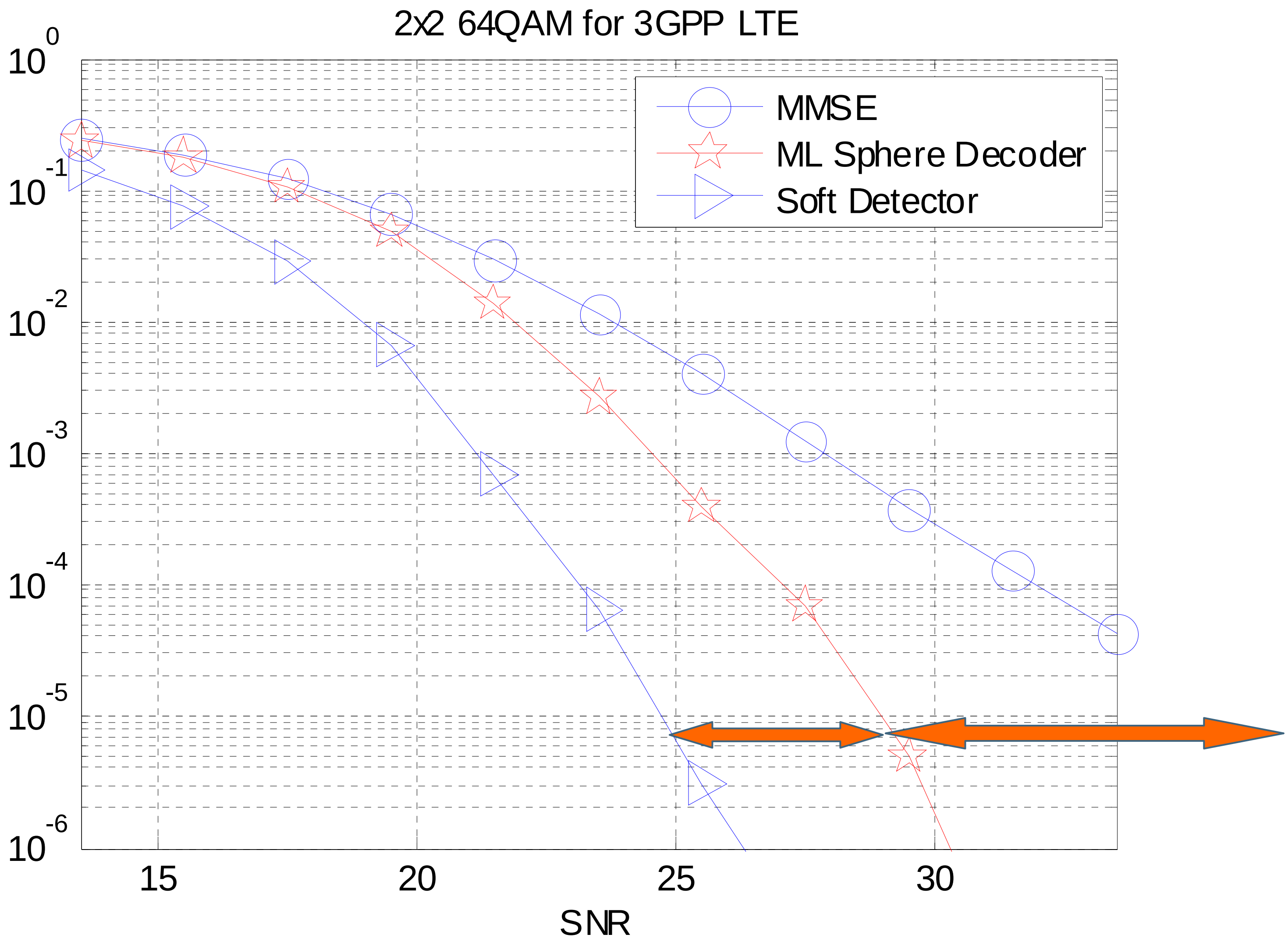
Summary of Our Approaches

- Algorithmic transformations
  - Make algorithmic structures compatible with architecture and compiler
- Pre-compiler code transformation
  - Fine-tuning of the mapping on architectures to optimize efficiency
- Fine-tuning of architectures
  - Application specific instruction set design and implementation

Case Studies
3 of Them will Be Introduced

- Sphere detector
- Soft-output sphere detector
- Partial FFT/IFFT
- OFDM channel estimator with sparse matrix multiplication
- .....

ML Sphere Detector Outperforms MMSE by 4-8 dB, Soft-Output Detector Improves More



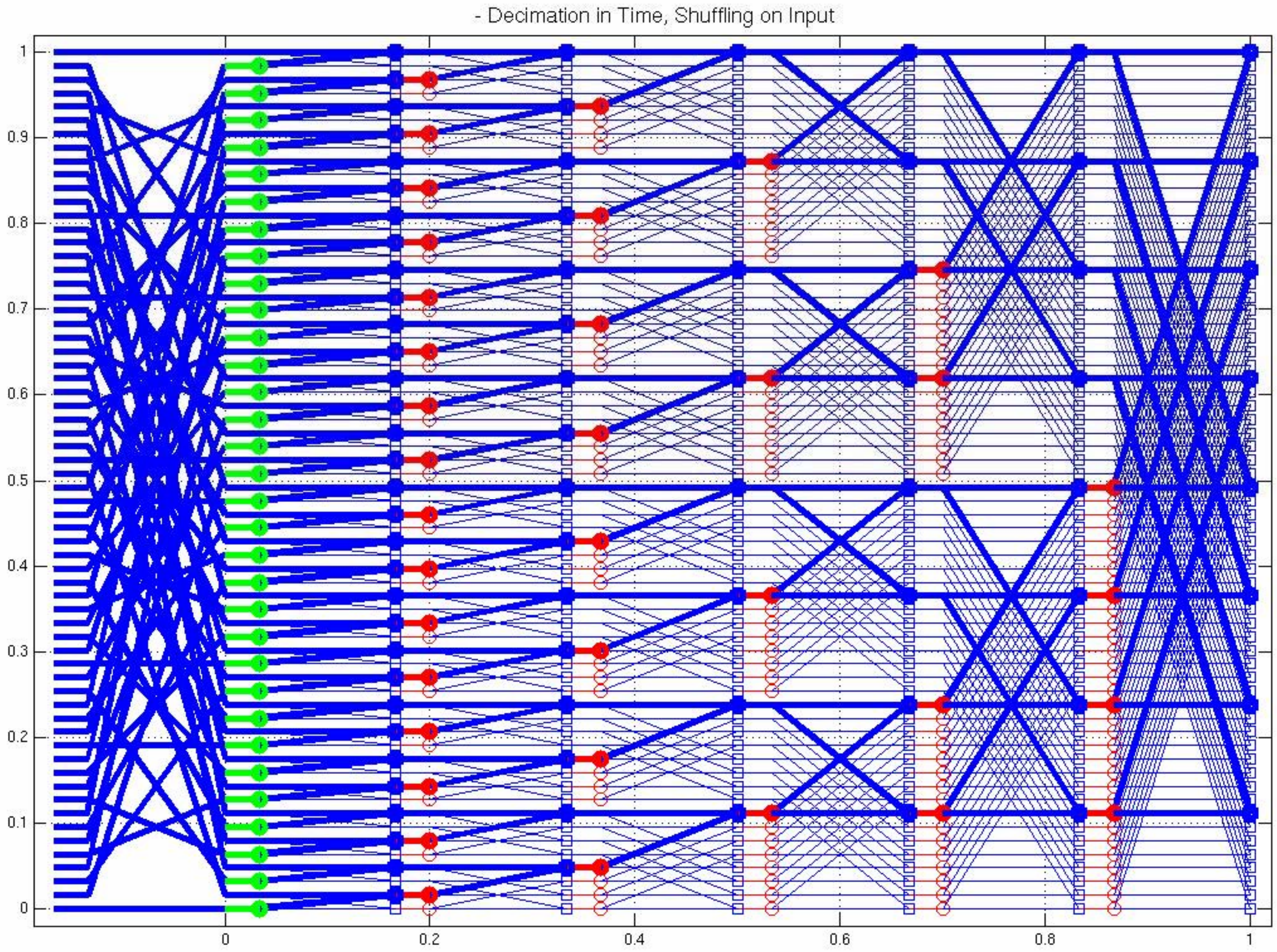
The FIRST Sphere Detector Explicitly Designed for Parallel Programmable Architectures

- The world's first sphere detector that can be efficiently implemented on VLIW, SIMD and vector architectures
- Scalable throughput from 4.5 Mbps to 112 Mbps (4x4 64QAM) even on TI TMS320C6416
- Higher than 75% scheduling density on 4x4 ADRES architecture

The FIRST SOFT OUTPUT Sphere Detector on Parallel Programmable Architectures

- Very challenging even for ASIC (100 Mbps at 1.2W)
- The world's first soft-output sphere detector that can be efficiently implemented on VLIW, SIMD and vector architectures
- Designed with 4 application specific instructions
- 2x4 ADRES with 16-way SIMD achieves 192Mbps for 2x2 64QAM, about 385Mbps for 2x2 16QAM

Partial FFT (PFFT): FFT with Partial Input or Output



PFFT: 30+ Years Theoretical Research But Few Real Life Implementations

- Highly recognized importance in countless engineering areas
- More than 30 years theoretical research
  - Complexity oriented analysis and bound analysis
- Few practical implementations
- We reported the first generic implementation of PFFT on ILP architectures
  - Demonstrated on TMS320C6000 as well

Enhancing Energy Awareness with Dynamic Scalability

imec

We Can Exploit The Dynamics in Wireless Communication Systems for Energy Efficiency

- Both user requirement and environment are dynamic

Voice call on highway

Online game in metro

Voice call on street

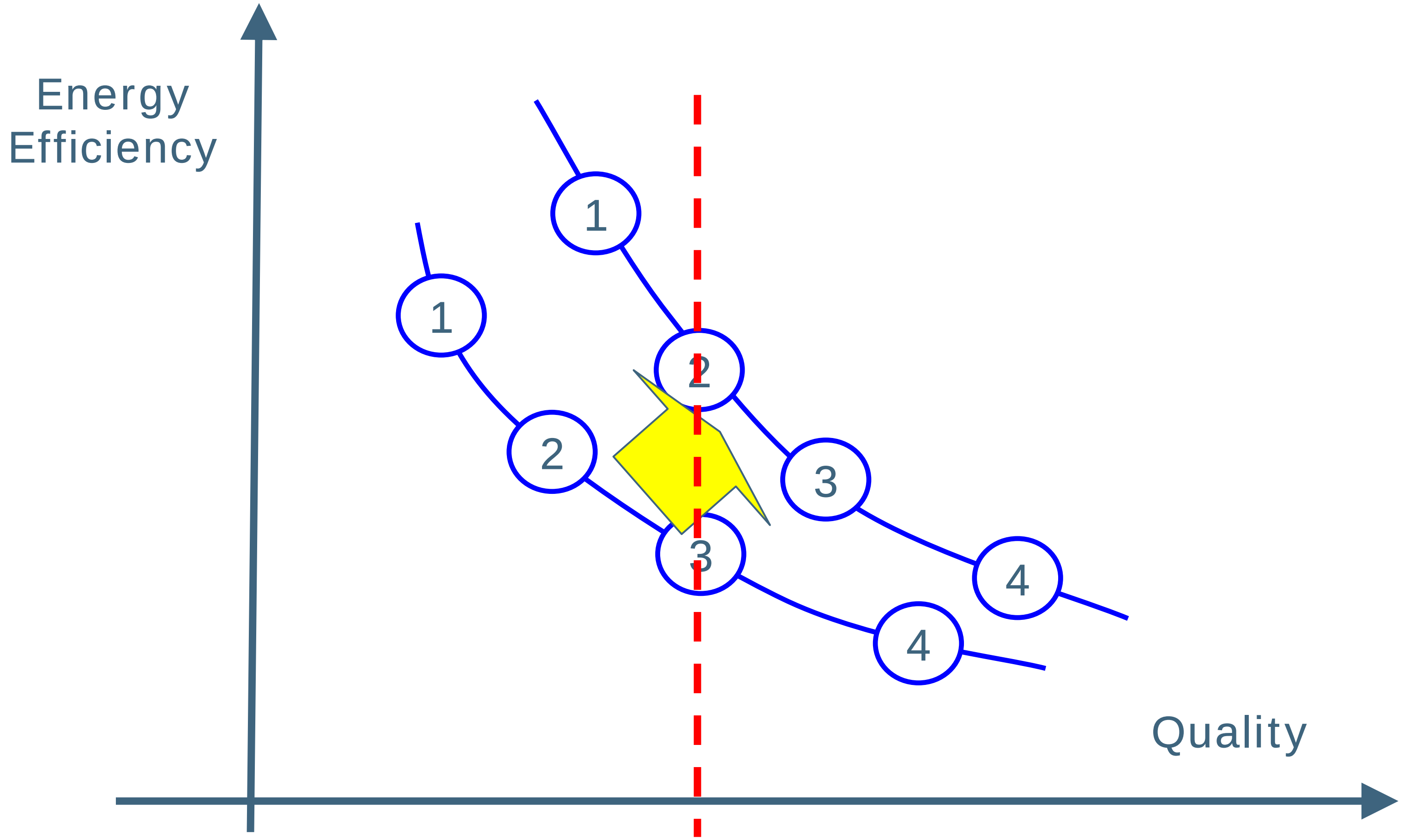
Video streaming in car

Opportunities for SDR Baseband

- Two viewpoints toward complexity
  - Computation complexity and memory complexity
  - Structure complexity (heterogeneity, number of blocks, etc.)
- On SDR baseband platform
  - Computation complexity is much more costly than that in ASIC
  - Memory complexity is as costly as that in ASIC
  - Structure complexity is much less costly than that in ASIC, the multiplexing of memory and data-path is much easier

From Uniform, Regular Design to Highly Agile, Heterogeneous Design

Scalable Energy Aware Baseband with Dynamic Controller



Case Studies of Major Components in MIMO-OFDM Receiver

- OFDMA modulator
  - 2x to 12x improvements of energy efficiency
- Efficient near-ML MIMO detector
  - 2.8x to 28x improvements
- Adaptive filter implementation
  - Up to 5x improvements
- OFDM channel estimator
- Synchronizations in MIMO-OFDM
- .....

Conclusions

Conclusions

- We shift mobile SDR baseband from basic systems/algorithms to more advanced ones
- Enhancing the friendliness between algorithm and architecture/compiler
- Enhancing the energy awareness with dynamic scalability
- Case studies:
  - Major components in MIMO-OFDM/OFDMA systems
  - Demonstrated on both ASIPs and commercial DSP (TMS320C6000)

Questions