MANUFACTURABLE 60GHZ CMOS LNA**s**

Amneh Akour (The Ohio State University, Columbus, Ohio, USA; akoura@ece.osu.edu);
Mohammed Ismail (The Ohio State University, Columbus, Ohio, USA; ismail@ece.osu.edu);
and Roberto Rojas (The Ohio State University, Columbus, Ohio, USA; rojas@ece.osu.edu)

ABSTRACT

Emerging broadband applications are pushing for the need to build high data rate wireless transceivers at 60GHz for high volume low cost mobile devices. Central to the success of implementing such transceivers is the robust design of 60GHz CMOS RF front ends, especially the low noise amplifiers (LNAs). Two different topologies are used to build LNAs; two-stage CG-CS LNA and three-stage CS LNA. The performance of these topologies is compared to select the best one with the best transmission line type. This paper proposes a digital self-calibration technique for LNAs' to enhance the yield to at least 90%. The proposed technique is shown to maintain typical specified performance at worst case corners and hence allowing for manufacturable 60GHz RF CMOS design for high volume applications without leading to over-design or increasing power consumption. The LNA has been designed and tested in IBM 90nm technology. It is shown that the proposed calibration restores LNA performance in the presence of random process, supply and temperature variations.

1. INTRODUCTION

Design and development of wireless access and wireless LAN system operating at 60 GHz is considered as part of the fourth-generation (4G) systems. There exist numerous multimedia applications calling for wireless transmission over short distances. The third-generation cellular systems are not built based on low-cost technology and may not be able to cope with data rates in excess of 2 Mb/s. Due to these limitations, WLAN systems come into the picture. WLAN products are based on either the IEEE 802.11b standard at 2.4 GHz with a gross capacity up to 11 Mb/s, or the IEEE 802.11a/g at 5 – 6 GHz and 2.4 GHz with input data rates of 6 - 54 Mb/s. Because of the data rate limitation of this type of communication, WLAN does not support the required data rates for attractive services. To achieve higher network capacity, two approaches can be used: increasing the spectral efficiency by using higher order modulation methods, and/or using more bandwidth. The European Advanced Communications Technologies and Services (ACTS) program, the Multimedia Mobile Access Communication (MMAC) Committee in Japan, and the Federal Communication Commission (FCC) address the 59 - 66 GHz frequency band for general unlicensed applications to get ultra-high speed wireless indoor LANs supporting 156 Mb/s [1], [2].

The first generations of 60 GHz transceiver have been implemented by GaAs PHMET technology [3], or by SiGe Bipolar technology [4] - [8]. The availability of wider spectrum, the need for higher data rate, and the potential for high volume applications are generating interest in investigating the applicability of advanced CMOS technologies for solutions in X-band (8-12 GHz), K-band (18-26 GHz), and V-band (40-70 GHz). CMOS transceivers potentially provide highly integrated inexpensive mm-wave devices and can eventually be transformed into main stream high volume applications. FET f_T, f_{MAX}, and NF_{MIN} will improve with every new process generation, although the concurrent constraints on supply voltages will present an increasing challenge.

Designing 60 GHz CMOS transceivers has many challenges and limitations. CMOS substrate suffers from excessive high path losses due to oxygen absorption, high sheet resistance of silicide gate, high gate leakage, low breakdown voltage, and the channel-length modulation because of the thinner gate oxide thickness and short channel length. To overcome these limitations, new CMOS technologies need to be used with double-sided narrow finger and close substrate contacts to the device. Actual performance of devices at mm-wave frequency is highly layout dependent, so large-signal performance can still be maintained if care is taken through careful layout. . The array layout, dubbed the "round table" layout, is preferred to reduce the impact of external parasitics on determining the maximum frequency of activity [9]. While FET with f_T, and f_{MAX} greater than 300 GHz are now available in 90nm CMOS nodes, accurate and scalable FET models in mm-wave regime are a challenging task. The present FET CMOS models have been designed and tested only up to 10 GHz frequency.

This paper proposed a methodology suited to self-calibrate 60 GHz LNAs so that they achieve high yield at different corners under random process, temperature and

supply variations. The proposed solution takes advantage of the technology scaling and used digital calibration to control the current mirror that bias several points of the LNA.

2. MODELING ACTIVE AND PASSIVE DEVICES

2.1. Modeling Active Devices

Most of the compact model parameters for active devices have been extracted for low-frequency applications. This causes inaccuracy in using these parameters for mm-wave applications. Some device mechanisms that are not well captured at low frequencies have considerable effect on the performance of the device at higher frequencies. The effect of substrate resistances and capacitances is an example of such effect [10]. The induced gate noise is another example of an effect not modeled in the present most low-frequency compact models. At mm-wave frequencies, the layout effect contributes to the inaccuracy in these models. Small inductors, resistances and capacitors, due to the device interconnections to the outside world, introduce additional components to the low-frequency model. These components change and dominate the performance of the device as the frequency increases.

A detailed full-wave electromagnetic simulation is required for an accurate prediction of these parasitics; however, this simulation can be difficult and lengthy. Therefore, each small finger of the transistor is modeled with the "intrinsic" transistor model as the core for a hybrid mm-wave model , while interconnects are captured by combination of selective electromagnetic simulation and experimental techniques. Additional parasitic resistances and inductances as well as a substrate network have been added to the hybrid-Л model of the core transistor [11]. The effect of the induced gate noise needs to be added to this model for accurate parameter extraction of the noise.

2.2. Modeling Passive Devices

The scaling in new CMOS technologies has not been very effective in scaling down passive components since the circuits and passive elements still occupy most of the chip area. Compact and low loss passive components in silicon process are required to counteract the induced losses of interconnects due to the conductive silicon substrate at high frequencies. At mm-wave frequencies, the required inductors for matching networks and resonators become increasingly small on the order of 30 - 300 pH. Therefore, transmission lines have to be used for device connection and signal distribution to retain the signal fidelity in the mm-wave regime. We have adopted two types of transmission lines in designing passive components for these 60 GHz LNAs: microstrip and coplanar waveguide

transmission lines. Efficient and accurate modeling of transmission lines is one of the most challenging tasks in designing 60 GHz radios. Microwave models used by the simulators are based on some assumptions: thin conductors, the ground planes are far from the signal line, and high-quality dielectrics, but these assumptions are invalid in CMOS technology. Silicon is a lossy substrate, the substrate is very close to the signal line, and metal thickness is on the order of the dimension of the conductor width and signal-to-ground spacing.

The extraction of the model can be performed using:
a) Electromagnetic Simulation of passive components and circuits based on finite size physical layout (Ansoft HFSS). To improve the simulation time in this simulator, different assumptions are made: uniform doped silicon substrate, multi-layer dielectric are modeled with two layers, and constant loss tangent. This simulator provides us with accurate results, but at the expense of long simulation time and inability to include poorly characterized effects. If the above assumptions are invalid in the real substrate, this simulator can give unexpected and false results and models.
b) Electrical Models in Agilent ADS. Electrical models in ADS can provide designers with acceptable and scalable models for transmission lines especially if Momentum (a full-wave technique based on the Method of Moments (MoM)) is used to extract the parameters. Models in ADS can be extracted easily, can be integrated easily in commonly-used simulators and optimizers, and require less simulation time because the substrate, although of finite thickness, is assumed to be infinite in the other two dimensions. This assumption does not add any significant errors for the present application. The required parameters to model transmission lines in ADS are: characteristic impedance, effective dielectric constant, attenuation constant, and loss tangent.

For accurate modeling for the two types of transmission lines mentioned above, we designed and simulated them using the Method of Moments in ADS. The output files for the simulated devices are imported and used to model all passive components in the 60 GHz LNA under the Cadence environment. Some prototype transmission lines are designed and taped out (Figure 1) to test the accuracy and the validity of using MoM to model passive components at 60 GHz.

3. 60 GHZ LNA DESIGN

The LNA (Low Noise Amplifier) is the first gain stage in the receiver path, so its noise figure directly adds to that of the system. Therefore, the LNA needs to be designed to meet certain tight specifications in to achieve high performance for the whole receiver. Many parameters are used to measure the performance of the LNA: gain, input/output matching or return loss, noise figure, reverse

isolation, linearity, and stability. CMOS FETs were considered slow, noisy devices up to about a decade ago. The scaling in CMOS technology has improved their performance dramatically. Different architectures have been used to build LNA at low frequencies: Common-Source topology, cascaded common-
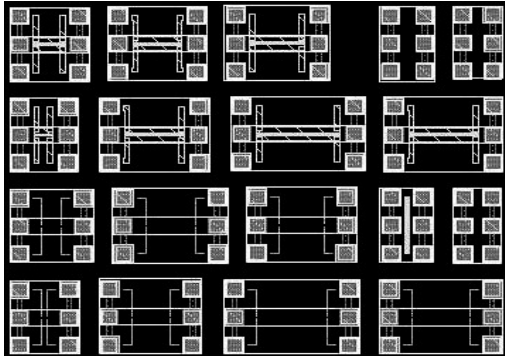

Figure (1) 60 GHz Prototype transmission lines

gate and common-source, folded cascode common-source, and inductive source degeneration. The most famous topology used in designing LNA at low frequency is inductive cascode common source degeneration . The two transistors in this architecture share the same bias current and save power through the use of the same bias current. Cascode topologies provide low noise figure, good input matching, and high reverse isolation.

At frequencies well below the fT of transistor, cascode topologies provide a low noise figure, good input matching, and high reverse isolation. On the other hand, at high frequencies, the pole at the cascade node shunts a considerable portion of the RF current to ground. This results in the lowering of the gain and raising the noise contributed by the cascade device. Furthermore, the circuit is very sensitive to package parasitics due to the small required degeneration and gate series inductances. Therefore, either other topologies are required to build 60 GHz LNA or some modifications need to be introduced to the inductive source degeneration LNA to overcome the above limitations.

One proposed solution to design a 60 GHz LNA uses a single transistor as a common-gate stage before voltage amplification [12] as shown in Figure (2). The common-gate stage degrades the input matching and increases the noise figure unless large devices are used. To solve this problem, a resonator is built at the source to cancel generated capacitance at this node. Similarly, the output mode must resonate to cancel the capacitance seen at the transistor drain and introduced by the next stage.

Another way to build a 60 GHz LNA uses multi cascade stages with input, output, and interstage reactive matching [11] as shown in Figure (3). Gain stages of

NMOS common source cascode amplifiers can used to reduce miller capacitance and improve the stability.

An inductive cascode source degeneration topology can be used to build a 60 GHz LNA, but some modifications need to be introduced as discussed in [13]. The capacitance introduced at the output node limits the bandwidth and raise the contribution of the cascode transistor to the output noise. This capacitance can be resonated by an inductor connected at this node. It can be shown that introducing an inductor at this node in this proposed topology generates a stability problem in designing the LNA.
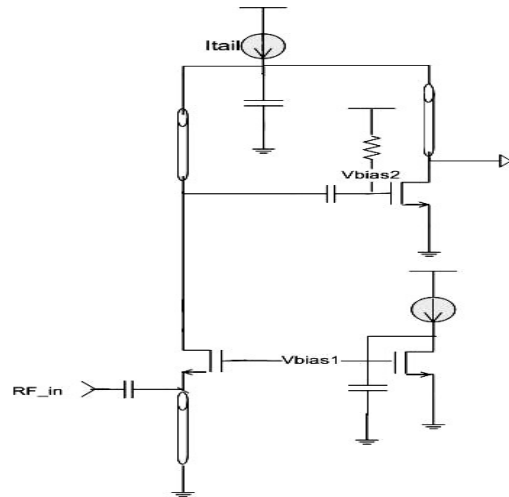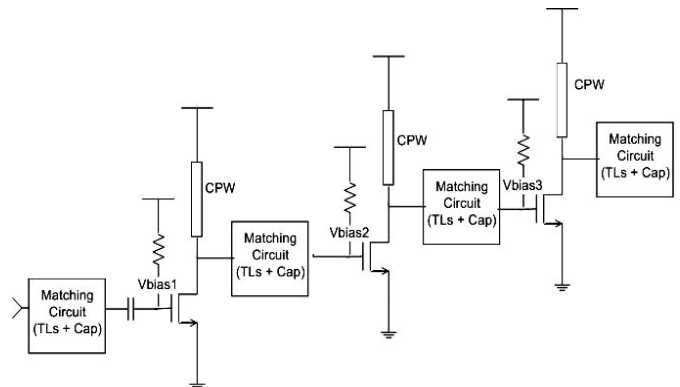

Figure (2) Two stage CG – CS LNA

Figure (3) Three-Stage CS LNA

The first two topologies are used to design two LNAs in IBM 90nm technology. Some key parameters are used to improve the performance of the two LNAs in order to check the validity of the proposed calibration technique in this work.

4. CALIBRATION TECHNIQUES FOR 60 GHZ LNA

The integration of analog mixed signal circuits in a System-On-Chip (SOC) platform is considered a key solution for the new generation of complex radio transceivers. CMOS technology scaling and innovation improve the performance of the digital part tremendously, but the radio part remains a major bottle-neck. The integration of analog and digital circuits faces several challenges such as coupling digital noise through substrate and power lines. A fully integrated CMOS radio requires several design cycles to meet the product specifications with relatively low yield. Analog circuits are affected strongly by random variations in process, temperature, operating conditions, and power supply variations. These variations do not scale with process. This causes an increase in the NRE cost and missing market windows. There are two possibilities to solve these problems: either by designing at worst-case corner simulation; but this leads to over-design and increases power consumption, or by building self-calibration circuits inside the RF blocks resulting in radio circuits that meet all the specifications.

The above challenges in designing RF blocks are more critical at 60 GHz than at low radio frequencies. An excellent self-calibration technique has been proposed in [14] to calibrate inductive source denegation LNAs operating at one-digit radio frequencies. Calibration cycle requires taking the input and output of the device under test (DUT) using suitable and sensitive sensor, converting the dc output voltage of the sensor into its equivalent digital signal, analyzing the results, generating a correcting signal using digital calibration algorithm, and then feeding back the correcting signal to the DUT as shown in Figure 4 [14]. The calibration circuit should have fast calibration time, low additional power consumption during calibration and during operation.
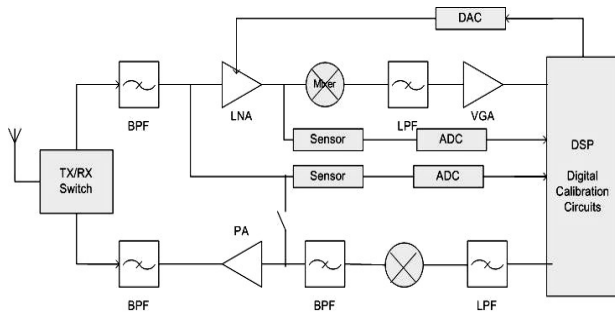

Figure (4) Built-in self test concept

Since this technique were only used and applied for LNAs at low radio frequencies, more research need to be performed in order to use it for 60 GHz LNAs. This work will adapt some calibration techniques to perform calibration of different 60 GHz LNAs topologies to meet the gain and input/output matching requirements. The digitally corrected word will be used to control biasing and load circuits of the LNA to bring back the gain and input/output matching circuits to their nominal values. Adding the two capacitors in parallel with Cgs and Ls can not be used for the 60 GHz LNA, because this will further decrease the value of the inductors making design more sensitive to packaging parasitics and process variations. Therefore, other calibration techniques need to be used to improve the performance of the LNA under worst case conditions and under process and temperature variations.

The gain of the LNA depends strongly on the transconductance of the NMOS input transistor, gm, and gm is related and controlled by the biasing current flow through the input transistors. Therefore, the best way to calibrate the gain is controlling the biasing current that affects the input transconductance. This can be performed by changing the basing points V_{bais2} and I_{tail} for the circuit in figure 1 and the biasing points V_{bais1}, V_{bias2} and V_{bias3} for the circuit in figure2. In addition, a switchable load can be used for additional control.

The biasing of the LNA is achieved by ratioed mirroring currents derived from a reference voltage supply generated using a bandgap circuit. Vbias is changed by switching 4 PMOS transistors sized with binary weights for each biasing voltage separately. These transistors are switched digitally using a 4-bit control word. The output biasing voltage varies by +/- 100 mV around its nominal value. Figure 5 shows the current mirror biasing and calibration circuit for both V_{bais} and I_{tail}. Figure 6 shows the gain variation for different biasing calibration words. This variation covers the expected degradation in the LNA gain under random process, temperature and supply variations.
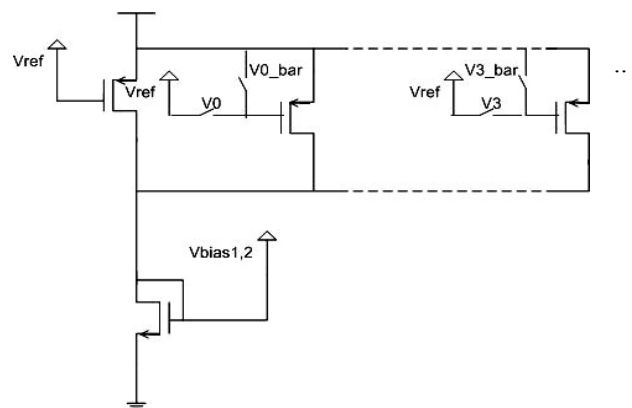

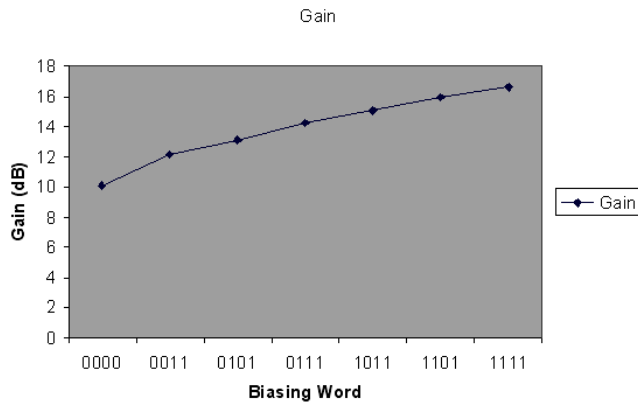Figure (5) Current mirror calibration circuit

Figure (6) Gain variation vs. biasing voltage word

To calibrate the input/output matching for the LNA, variable passive components can be used instead of the fixed ones. Designing variable transmission lines is very difficult. Therefore, there are two possibilities to perform that task: either using variable capacitor (varactors) instead of variable transmission lines, or using switchable transmission lines in the input/output matching circuit. More work in using these two approaches is ongoing.

5. RESULTS

As a demonstration of the proposed calibration techniques, a full transistor level simulation of a common gate – common source and multi common source LNAs is performed. The two reference LNAs are designed in IBM 90nm technology. Table 1 shows the simulation results for both LNAs under typical case where the normal simulation corner is used and no extra parasitics are included at 60 GHz frequency (V_{dd} = 1.2V, Temperature = 25^0C). When the parasitic elements, process corners, voltage or temperature change, the reference LNA performance is completely degraded as shown in Table 1. The corner conditions vary from -10^0C to 75^0C and +/- 10% power supply variations. The reference voltage for the biasing circuit was designed using a bandgap circuit. Parametric simulations have been run on the biasing voltage of the input transistors to demonstrate its effect on the overall gain of the LNA. The simulation shows that the gain of the muti-CS LNA varies from 10.1 – 17.5 dB. The calibration of the PMOS current mirrors (V_{bias}) are designed to have a tuning range of +/-25%.

The calibrated LNAs for the two topologies have been designed using the circuit shown in figure 5 to tune the gain of the LNA by controlling the biasing voltage for the input transistors. The proposed calibration method has been executed for the same corner conditions (TT and SS) under different correction words to show the effect of the

Table 1. Simulation results for the reference LNAs

	CG + CS	Multi CS
Av (dB) [TT]	9.7	16.67
NF (dB) [TT]	13.06	11.04
Av (dB) [SS]	6.34	12.45
NF (dB) [SS]	15.1	12.89
Av (dB) [FF]	9.9	17.03
NF (dB) [FF]	12.87	10.43

calibration circuits on each LNA's gain. Table 2 shows the simulation results of the calibrated LNAs under different corner conditions. As shown in these results, varying the biasing word can bring the LNA back to meet its specifications under typical and worst case conditions. More work is needed using tunable load and matching circuits to calibrate the input/output matching for the LNA. As noticed from the results, an additional benefit of the gain calibration is the improvement of the noise figure of the LNA.

Table 2. Simulation results for the calibrated LNAs.

	CG + CS	Multi CS
Av (dB) [TT]	9.7	16.67
NF (dB) [TT]	13.06	11.04
Av (dB) [SS]	9.43	16.17
NF (dB) [SS]	12.88	11.36

The remarkably improved performance of the two LNA topologies under different corners using the proposed calibration techniques offers interesting possibilities in designing 60 GHz LNAs with high yield from the first design cycle.

6. ACKNOWLEDGMENT

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