

# MULTIBAND PUBLIC SAFETY RADIO USING A MULTIBAND RFIC WITH AN RF MULTIPLEXER-BASED ANTENNA INTERFACE

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## ABSTRACT

Various public safety personnel often cannot readily communicate with one another due to the lack of interoperability in their radios. One of the solutions to this problem is to provide user a multi-band multi-mode radio (MMR). In this paper we present the design of an experimental prototype multiband radio, which operates in public safety frequency bands from 100 MHz to 1 GHz. In our design we use a direct conversion CMOS transceiver RFIC developed by Motorola Research Laboratories, which covers the frequency range 100 MHz to 2.5 GHz and contains multiple receivers and transmitters. Although direct conversion has some significant advantages over superhet-based design particularly due to its low power consumption and cost, there is a significant challenge to achieve performance comparable to existing single and dual-band radios. Furthermore, it is difficult to cover all of these bands using the same type of monopole antennas already in common use. Our design employs a multiband antenna-transceiver interface consisting of an RF multiplexer which yields acceptable overall performance for operation in public safety frequency bands using a simple monopole antenna. An FPGA is used to implement all the digital signal processing and a small Gumstix computer including a touch screen LCD is used as a user interface.

## 1. INTRODUCTION

Multiband multimode radio (MMR) is a class of radio which can operate in multiple frequency bands using multiple modes. This is a desirable solution to solve interoperability problem in public safety applications [1, 2]. In this paper we present an experimental prototype design for a low-cost MMR which provides simultaneously very large instantaneous bandwidth (up to 10's of MHz) to process multiple channels concurrently and very large tuning ranges to cover multiple bands of frequencies. This paper follows up on our previous paper [3], which described our motivation and early stages of development. Figure 1 shows the image of our designed prototype. Detailed description and all the documents related to this are available at the

project website in [4].



Figure 1: Experimental prototype MMR.

This paper is organized as follows. Section 2 describes the high level system design, whereas Section 3 presents the description of the RFIC, which we used to design this MMR. Description of the novel RF front end is presented in Section 4. Section 5 briefly discusses the digital signal processing and a more detailed description of the prototype is given in Section 6.

## 2. HIGH LEVEL SYSTEM DESIGN

An overall system diagram of our prototype MMR is presented in Figure 2. A low cost 18 cm-long monopole antenna is attached to a RF multiplexer specifically designed to match with the antenna impedance in such a way that the highest possible sensitivity can be achieved in our desired frequency bands. Four RF switches control the receive channel selection of RF multiplexer. Additional two switches are used to control the transmit RF channels. After further amplification and filtering, the four receive channels are connected with the four receiver inputs of the direct conversion RFIC. In the same way, two transmit channels

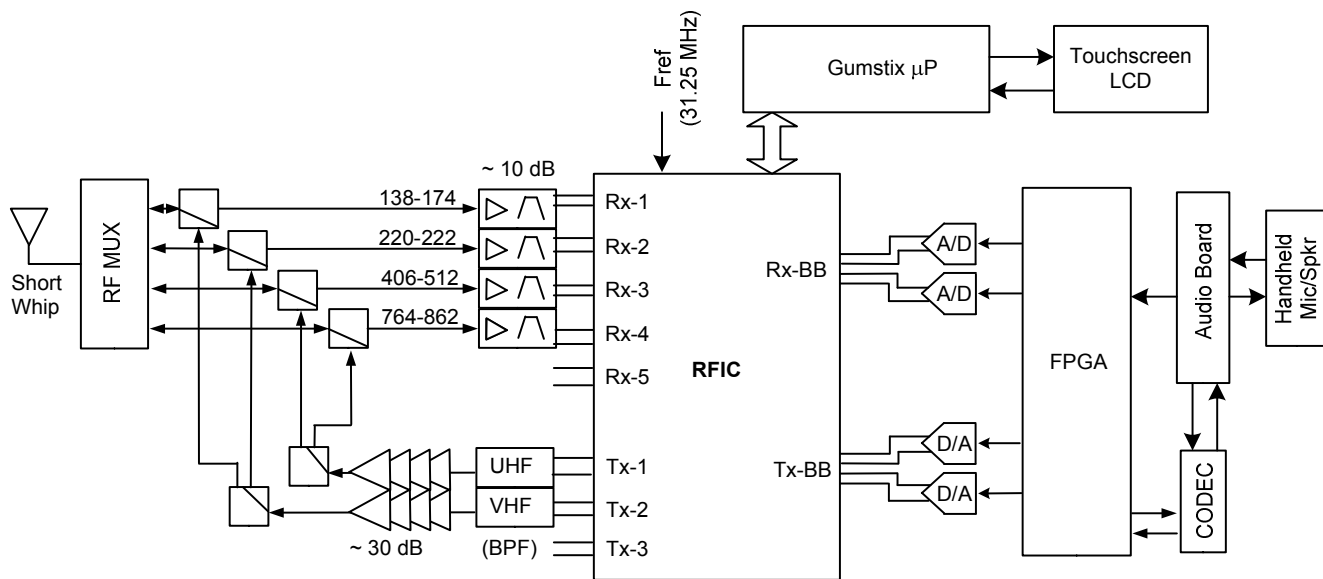


Figure 2: Overall system diagram.

are connected with the two transmit ports of the RFIC.

RFIC receiver channels convert the incoming RF signal to baseband differential in-phase (I) and quadrature-phase (Q) analog signals. A/D converters digitize these I and Q signals and send these to an FPGA for further processing. In transmit, the D/A converters convert digital transmit signal from FPGA to analog I and Q signals and send these to the RFIC, which upconverts to the carrier frequency by direct conversion. All the modulation/demodulation and digital signal processing are implemented in the FPGA. We also designed an audio board which interfaces a conventional handheld PTT speaker/microphone to the FPGA via a separate CODEC. A compact Gumstix computer including a touch screen LCD are used as a user interface of this radio [5].

### 3. MULTIBAND DIRECT CONVERSION RFIC

Although superheterodyne architecture has been preferred for public safety MMR for many years, the design gets complicated, expensive and power hungry if we want to cover large range of frequencies using this approach [2]. Direct conversion can be an alternative approach that alleviates these problems, but historically has been shunned due to limited performance. Motorola Research Laboratories has recently developed a multiband direct conversion RFIC using 90 nm CMOS [6]. Figure 3 shows the internal block diagram of this prototype RFIC. This IC is designed for the operation in 100 MHz to 2.5 GHz frequencies. Three independent direct digital synthesizers (DDS) are used

provide local oscillator (LO) signals to the receivers, transmitters, and feedback signal sources from a common 1GHz PLL. The only external reference signal required is 31.25 MHz at -10 dBm.

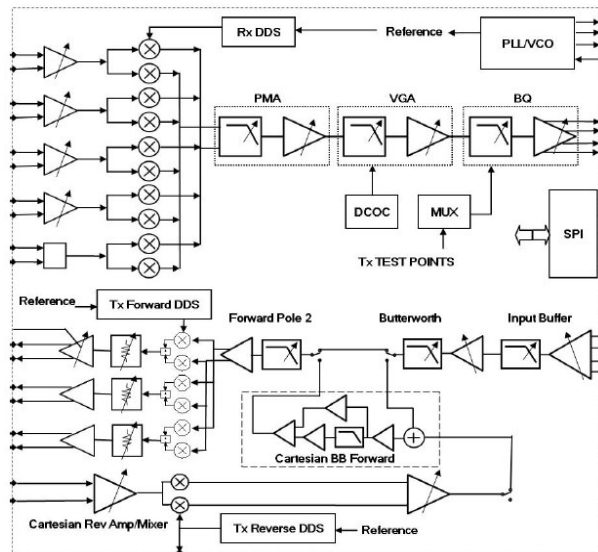


Figure 3: Internal block diagram of RFIC.

There are five receiver paths which share a common analog baseband low pass filter section with programmable corner frequency in approximately 10% steps from 4.5 kHz to 10 MHz. There are provisions for DC offset correction and dynamic matching [7]. These result in significant improvements in IP2, LO flicker noise, and DC offset compared to previous RFIC-based direct conversion designs.

Similarly, there are three transmitters which share a common baseband input. Differential baseband in-phase and quadrature-phase inputs from external digital-to-analog converters (DACs) are applied to programmable low pass filters similar to those of the receiver with 10% bandwidth steps from 6 kHz to 10 MHz bandwidth. There are three selectable transmitter paths with up to 75 dB (30 dB continuous and 45 dB stepped power control) of on chip programmable gain available (power control). A transmitter feedback network is provided for closed-loop narrow band linearization or open-loop alternative transmit signal analysis and processing.

The RFIC is configured and controlled using a serial peripheral interface (SPI) link. Approximately 262 registers are programmed to set the various parameters.

Prior to using this RFIC in our design, we evaluated it using several standalone evaluation boards and found performance to be generally consistent with specifications published by Motorola [8, 9].

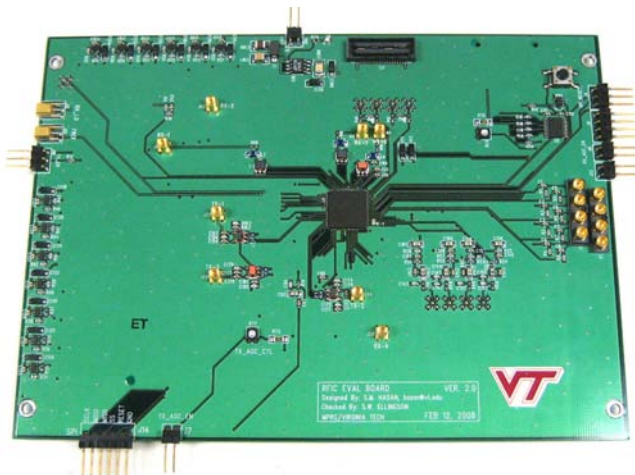


Figure 4: Image of RFIC implementation in the current MMR prototype.

Figure 4 shows the implementation of the RFIC in the current MMR prototype. Since the receivers in the RFIC require differential signals, transformers have been used as a baluns to convert between single-ended to differential signals. Ports Rx-1 to Rx-4 use the M/A-COM ETC1-1-13 1:1 transformer (frequency range 4.5 to 3000 MHz). Similar to the receiver section, the RFIC also provides the transmitter output in differential form, which is converted into single-ended using a transformer. Tx-1 and Tx-2 ports use the M/A-COM ETC4-1T-7 1:4 transformer (frequency range 6 to 1000 MHz).

Without optimization, the measured average gain of the receiver section of RFIC is 48 dB, input 1dB compression

point is -26 dBm and the sideband rejection is around 29 dB. Average transmitter output power is -4 dBm, output 1dB compression point is -5 dBm and average sideband rejection is 22 dB. The performance of this RFIC, specifically the sideband rejection, can be improved significantly if we optimize the various programmable parameters. But we have not yet attempted to do so in the current design.

During receive our current RFIC board consumes 1.1W power (10V@0.11A) and during transmission it consumes 1.7W (10V@0.17A) power.

#### 4. RF FRONT END

New generation single-chip CMOS direct conversion transceivers create the opportunity to design a low-cost efficient multiband multimode radio. However the inherent antenna problem remains essentially unsolved for such radios; specifically how they can be integrated into the design without degrading performance or leading to objectionable sizes or shapes. To be accepted by users, these radios must achieve performance comparable to existing single- and dual-band radios, using the same type of monopole antennas already in common use.

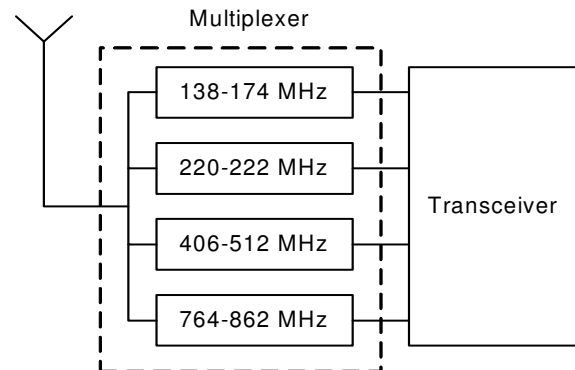


Figure 5: Antenna-RFIC interface concept using multiplexer.

Our front end/antenna interface concept is shown in Figure 5. Taking advantage of the Motorola RFIC's parallel transceiver architecture, we designed a four channel RF multiplexer, one side of which is matched with the antenna impedance and the other side is matched with the impedance of RFIC input/output ports. This design is documented in detail in [10], and the board-level implementation is shown in Figure 6. This front end board contains RF multiplexer filters as well as amplifiers, additional bandpass filters and variable attenuators to control receive gain. This front end has acceptable overall performance for operation in four bands – 138–174 MHz, 220–222 MHz, 406–512 MHz, and 764–862 MHz – when used with a monopole just 20 cm long with 5 mm radius. This is achieved not from an impedance-

matching perspective, but rather from the perspective of receive sensitivity. Specifically, we have designed the multiplexer in such a way that the receiver is guaranteed to have sensitivity which is external-noise dominated if the receive noise figure (determined by electronics following the multiplexer) can be constrained to be no worse than 1-2 dB. Although our existing design does not currently achieve this, such a noise figure is within the capabilities of existing low-cost electronics.

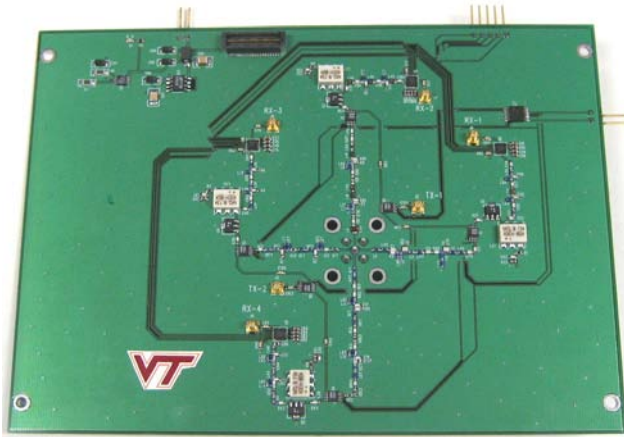


Figure 6: Image of the RF front end board.

Figure 7 shows the circuit topology used in each multiplexer channel. Performance of our designed multiplexer is presented in Figure 8. These results are expressed in terms of transducer power gain (TPG), defined as the ratio of power delivered by a matching network to a load, to the power delivered to a perfectly matched load directly from the antenna. Although the performance in 138-174 MHz appears to be poor, the resulting sensitivity turns out to be limited only by environmental noise under the conditions described above. Furthermore, the intentionally degraded efficiency of the 138-174 MHz channel enables improved efficiency in the other bands, as we explained in the next paragraph. For transmit operation, this filter would be switched to a more conventional match for improved efficiency.

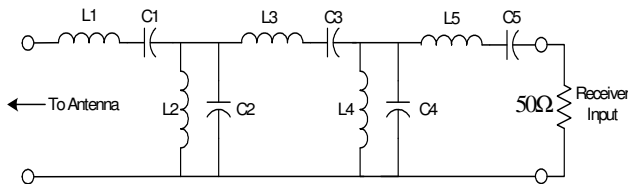


Figure 7: Circuit topology of each multiplexer channel.

The front end design procedure is as follows. Our design criteria to achieve the maximum possible sensitivity are that

the ratio of external (unavoidable) noise to internally generated noise at the output of a receiver front end should be large, and the TPG should be reasonably flat over the passband. We started our design using fifth order Chebyshev bandpass filters and performed joint optimization changing the component values to achieve maximum flatness for the first two channels and to get the maximum TPG for the other two channels.

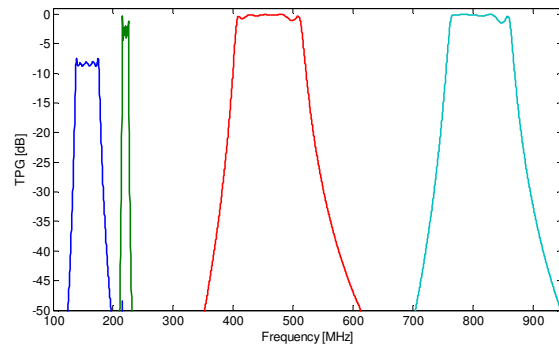


Figure 8: Performance of the designed RF multiplexer.

## 5. DIGITAL SIGNAL PROCESSING

The differential I and Q signals from the RFIC is digitized using the AD9248 dual 14-bit A/D converter from Analog Devices. Similarly, the AD9761 dual 10-bit D/A converter is used to provide differential analog I and Q signals. Figure 9 shows the image of the ADC/DAC board. All of our digital signal processing is performed in an Altera Stratix II FPGA. This FPGA is extreme overkill for this application; only about 5% of the logic elements are used for single channel analog FM. This FPGA was chosen to facilitate experimentation with multiple simultaneous modes at a later time. The firmware is written completely in Verilog HDL.

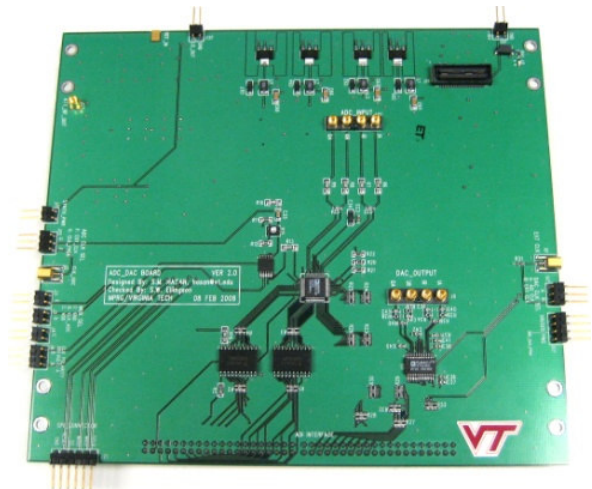


Figure 9: Image of the ADC/DAC board.

We used EP2S60 Stratix II DSP development board from Altera for convenience in implementation, as it includes also a suitable CODEC. This board communicates with the ADC/DAC board through an 80 pin ADI connector.

## 6. CURRENT STATUS OF THE PROTOTYPE

Our experimental prototype multiband multimode radio is able to operate in 138–174 MHz, 220–222 MHz, 406–512 MHz, and 764–862 MHz public frequency bands. Reception and transmission of narrowband FM signals have been demonstrated in all of the above frequency bands. A separate audio daughter board which contains push-to-talk circuitry, microphone and speaker amplifiers, has been implemented to send the PTT signal to FPGA. The whole radio is controlled using a Gumstix computer through a touch screen LCD panel. When the user selects a frequency from the touch screen LCD, the Gumstix programs the RFIC through SPI and sends the channel information to FPGA for controlling the Rx/Tx switches and attenuation in the RF front end board. The Gumstix computer is used just as a user interface and no digital signal processing is implemented in it.

This prototype consumes approximately 1.5A of current at 16V. We use a 4A.hr battery to operate the whole radio, which lasts for about 1.5 hours at this current draw. No attempt has been made to optimize power consumption. Although we implemented just narrow-band FM in our current design, it is possible to implement more modes in FPGA without any change in the hardware configuration, as explained above.

A goal of this work has been to determine whether the new direct conversion RFICs can replace existing superhet architectures. We have found there some issues (specifically image rejection and selectivity) which remain to be improved to implement this in an actual product. Much work in optimization of programmable parameters in the RFIC remains. In order to get the full benefit of differential design the RF front end including the RF multiplexer filters should be transformed into differential from single ended topology. A good user interface is also necessary.

## 7. ACKNOWLEDGEMENTS

This project is supported by the National Institute of Justice of the U.S. Dept. of Justice under Grant No. 2005-IJ-CX-K018. The authors are thankful to Gio Cafaro, Bob Stengel and Neiyer Correal of Motorola Research Laboratories for providing RFIC chips as well as extensive and patient technical assistance. Also thanks to Rithirong Thandee, Mahmud Harun, Kyehun Lee and Philip Balister for their assistance during this project.

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