A 65NM CMOS RF FRONT END DEDICATED TO SOFTWARE RADIO IN MOBILE TERMINALS

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ABSTRACT

The next generation of mobile terminals is faced with the emergence of the Software Radio concept. The Software Radio concept aims at designing a reconfigurable radio architecture accepting any cellular or non-cellular standards working in the 0-5 GHz frequency range. But technical challenges have to be overcome in order to address this concept. The main bottleneck is the Analog to Digital conversion which cannot be done at Radio Frequencies, at an acceptable resolution and at an acceptable level of power consumption. The idea proposed here was to interface an analog pre-processing circuit between the antenna and a Digital Signal Processor (DSP). It pre-conditions the RF signal. It uses the principle of an analog Fast Fourier Transform (FFT) to carry out basic functions with high accuracy in a low-cost technology like 65nm CMOS. This paper presents the schematics, the design and the behavioral simulations of this analog discrete-time device which gives the hardware flexibility required for a cognitive radio component.

1. INTRODUCTION

Various Software Defined Radio architectures are appearing since the last decade in wireless devices. It answers to the demand of reconfigurable systems to address different kinds of applications such as audio, graphic or video data in mobile terminals. These terminals are the place for a real multimedia convergence and have to be able to accommodate different wireless standards with different carrier frequencies, channel bandwidths, modulation schemes or data rates [1] [2].

Multifunctional circuits and systems are part of the solution. They can integrate the concept of Software-Defined Radio (SDR) in just one chip. A SDR circuit can be tuned to several defined frequency bands, select defined reasonable channel bandwidths, and detect known modulations. As far the SDR concept is limited to multifunctional systems, the Software Radio (SR) concept enlarges SDR to all Radio standards. A SR circuit can be tuned to any frequency bands, select any reasonable channel bandwidths, and detect any known or unknown modulation. This paper presents the architecture of an analog radio front-end receiver dedicated to SR.

Progress has been made on Digital Signal Processor (DSP) and baseband functions for SR. But to address the SR concept, progress has to be made also on low-power analog radio front-end. An ideal receiving SR architecture is only software. It is composed of a Low Noise Amplifier (LNA), an Analog to Digital Converter (ADC) and a Digital Signal Processor (DSP). The DSP is reprogrammable using existing standards and can address all the SR constraints by adapting himself to the received information. This solution is not feasible within the next 15 years for mobile devices. Today, it is not technically possible to create a fully digital SR system for a mobile terminal: Analog to Digital conversion (ADC) requires a 16-bit resolution and at least a 10-GHz sampling frequency [3] [4]. This ADC does not exist at an acceptable rate nor at an acceptable level of power consumption, the latter being critical as far as mobile terminals are considered.

A SR architecture was proposed to challenge these constraints. It is made by a LNA, an analog processor to perform low power analog calculations at RF frequencies, a low frequency ADC and a DSP. Thus, the RF signal is pre-conditioned analogically by a component located between the LNA and the ADC (Fig. 1) which avoids the technological bottleneck of the ADC. This component was called Sampled Analog Signal Processor (SASP). It does basic analog operations on discrete time voltage samples. The purpose is to reduce the RF signal data rate before digital conversion. The processor is fully analog and allows working directly at RF frequencies at an acceptable power consumption. It is reconfigurable by software through analog parameters defined by a DSP. The SR concept dedicated to mobile terminals is consequently addressed by a hardware component fully controlled by a DSP which is able to adapt all the receiving chain by itself. Whereas the digital conversion technological bottleneck is avoided, new challenges appear in the analog domain.

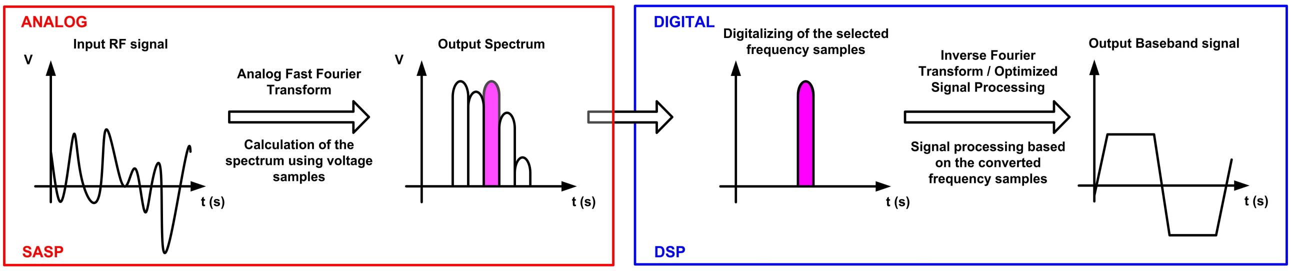

ANALOG
Input RF signal
V
t (s)
Analog Fast Fourier Transform
Calculation of the spectrum using voltage samples
Output Spectrum
V
t (s)
SASP
DIGITAL
Digitalizing of the selected frequency samples
t (s)
Inverse Fourier Transform / Optimized Signal Processing
Signal processing based on the converted frequency samples
Output Baseband signal
t (s)
DSP

Figure 2: Principle of a Software Radio Analog Processor

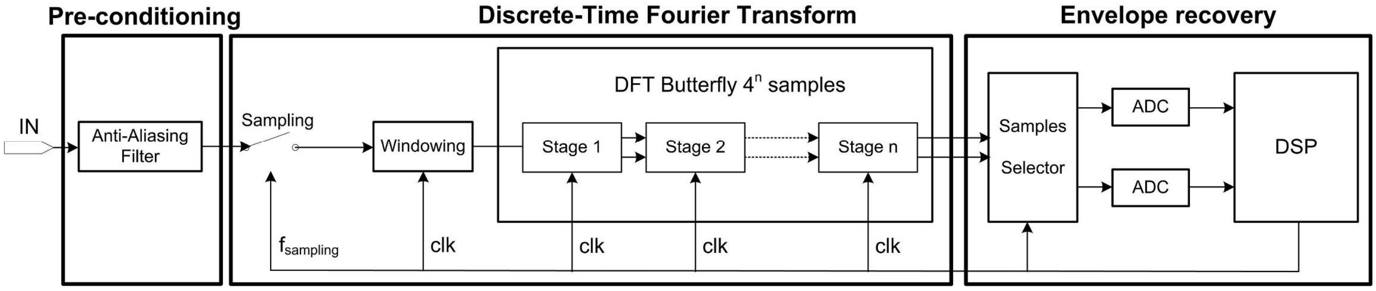


Figure 3: Architecture of a Software Radio Analog Processor

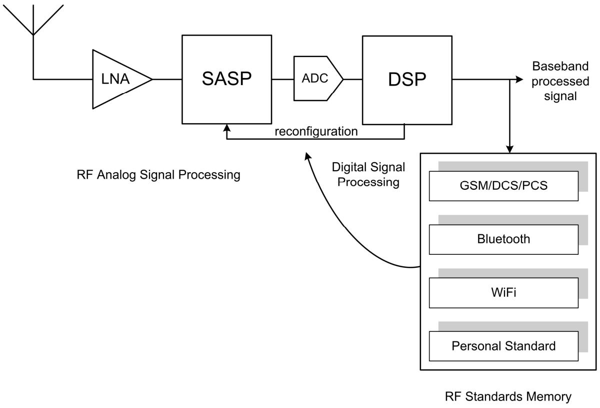


Figure 1: Proposed SR receiving architecture

2. THE SAMPLED ANALOG SIGNAL PROCESSOR

The SASP aimed at selecting a spectral envelope of a RF signal among all RF signals. To reach that target, the SASP processed analogically the RF input signal spectrum thanks to an analog Discrete Fourier Transform (DFT). Once the spectrum processed, voltage samples representing the signal envelope to be treated are converted into digital. The selection of few voltage samples among thousands replaces the classical mixing and filtering operations. It reduces dramatically the A/D conversion frequency from GHz frequencies to MHz frequencies (Fig. 2).

Two parameters inherited from the DFT equation (Eq. 1) mastered the SR requirements such as reprogrammability and flexibility: the sampling frequency $f_{sampling}$ and the number of voltage samples N are taken into account to determine the spectral accuracy.

Basic analog operations are done on RF signal voltage samples. One operation was to delay the voltage samples. The second was to weight and calculate the samples. The combination of both operations gives the analog DFT calculation.

$$X(k)=\frac{1}{N}\sum_{n=0}^{N-1}x(n)W_N^{nk}$$

k=0,1,…,N-1 (1)

$$W_N = e^{-j(2\pi/N)}$$

where N is the number of samples and x(n) is the input voltage sample value.

The RF incoming signal is sampled N times. Its spectrum is carried out using N discrete time voltage samples. Only the samples representing the signal envelope required are selected and digitized. This selection dramatically reduced the working frequency of the ADC and thus the processing speed of the DSP. Each sample represents a frequency range of $f_{sampling}/N$ on a $f_{sampling}/2$-wide spectrum. The processing accuracy and a well-sized output spectrum were determined by the 2 main parameters $f_{sampling}$ and N.

3. THE SASP ARCHITECTURE

The SASP is an analog processor working at RF frequencies. It implements basic analog blocks to provide an analog FFT calculation at RF frequencies. It integrates 3 main parts to calculate the FFT (Fig. 3).

- A continuous-time signal pre-conditioning
- A sampler and the analog FFT
- A RF signal envelope selection unit and the Analog to Digital Conversion

3.1. The Sampler

Once filtered, the RF signal is sampled at least twice the RF signal frequency. Sampling is the most important part of the system because the resolution of the calculation depends on its accuracy. The sampling frequency $f_{sampling}$ determines the FFT timing ($N.f_{sampling}$), the spectrum range (from 0 Hz to $f_{sampling}/2$) and the spectrum resolution ($f_{sampling}/N$). A Track and Hold (T/H) sampler pre-discretizes the signal and displays the voltage samples to the FFT circuit.

Once sampled, the signal is windowed with a Hamming window. It maximizes the FFT accuracy. The choice of this window is done as it is hard-implemented in the circuit and cannot be modified. The Hamming window is the best compromise in term of bandwidth and loss (Eq. 2).
The window period considered is equal to $T_p = N.T_{sampling}$ and is synchronized on the FFT processing period.

$$W(t) = 0.54 + 0.46.\cos(2\pi.t/T_p) \qquad (2)$$

3.2. The Analog FFT

3.2.1. Radix-4 FFT review

The SASP implements the FFT algorithm of Cooley Tukey. A radix-4 pipeline FFT was chosen to improve the speed efficiency. The FFT uses $\log_4(N)$ stages to process analogically the RF signal. Fig. 4 exhibits the example of a 16-sample radix-4 pipelined FFT with 3 stages ($3=\log_4(16)$) [7] [8]. Each stage implements one basic module which runs with two processing phases [7] [8]:

- Summation/subtraction and weighting factor [10].
- Feedback storage.

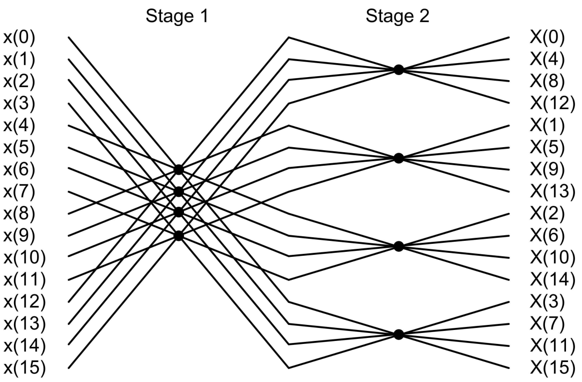


Figure 4: 16-sample radix-4 FFT

3.2.2. Architectural implementation

The signal is processed using voltage samples. As their values are stored analogically, real and imaginary parts of the FFT have to be calculated separately. Thus, a module implements the basic operations through 3 main parts (Fig. 5):

- A delay line
- A Processing Unit [11] composed by a Weigthing Unit and a Matrix Unit to process the basic analog operations on voltage samples.
- A feedback delay line

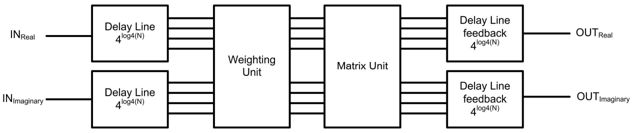


Figure 5: An analog radix-4 module architecture

The delay line carried out a delay equivalent as a z-transformation to z^{-1} by an accumulation delay line that stores the voltage sample during a given time (Fig. 6). It performs three operating states. For example, at a given time (Fig. 6):

- One sample is loaded in a capacitor (S_1 is closed).
- One sample is stored during the delay time (S_2 is open).
- One sample is either carried out on the processing unit or on the output stage (S_6 is closed).

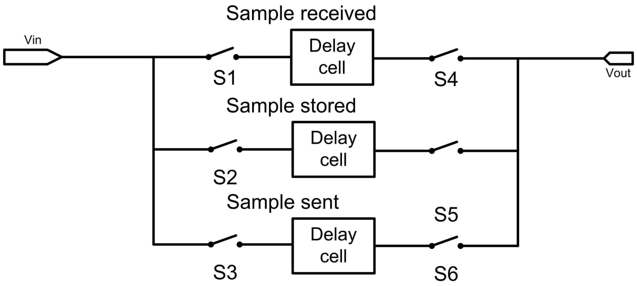


Figure 6: Accumulation delay line

The sample is stored in one of the $4^{\log4(N)} + 4^{\log4(N-1)}$ capacitors of the SASP delay line. The storage time carries out the delay in the line. This principle works on accuracy of voltage samples transfers by opposition to a regular delay line.

The processing unit adds and weights the voltage samples to provide the complex operations into the analog domain. Real and imaginary parts are either added or subtracted or weighted with hard-implemented coefficients. All the pipelined modules give the calculation of the FFT.

4. VALIDATION AND SIMULATIONS

4.1. A BPSK Modulation

Fig. 7 depicts the example of a BPSK modulation. The input bits were encoded through a phase shifting. The RF signal amplitude remained the same, but as the phase changes, the real and imaginary output spectrum were not the same depending on whether a '0' or a '1' is encoded. A BPSK demodulation could be optimized with the SASP by a relevant interpretation of the output spectrum (Fig. 7(a)). A simulation was done with a carrier frequency of 500MHz for simplicity. The BPSK modulated signal received was first windowed. Its length was sized to be the timing of a modulated bit (here 2.048 µs). The sampling frequency was 2GHz. The spectral accuracy was thus 488kHz. The processing was proven (Fig. 7(b)). The same modulated signal is depicted as in Fig. 7(a) but delayed of half a bit timing. The principle remained an adapted interpretation of the output spectrum. The output data rate was 488KHz. In this case, the working frequency was thus divided by more than 1000.

The decimation in frequency reduces the output data rate. The ADC working frequency is equal to $(N/N_{samples}).f_{sampling}$, with $N_{samples}$ the number of samples taken into account in the signal envelope. For instance, the GSM bit rate is equal to 271kbits in a channel bandwidth of 200kHz. Considering a 65536-element SASP, 4 samples could be targeted to recover the RF signal easily. The output frequency was thus 244kHz which is easy for an ADC to convert and for a DSP to handle. As exhibited in the case of a BPSK modulation, a direct frequency domain demodulation can be performed to optimize the digital signal processing.

4.2. The envelope selection

The radix-4 FFT algorithm implemented in the architecture (Fig. 3) displayed the output spectrum sample in a base-4-reversed order. This order implies that two neighbor frequency samples in the spectrum are several samples apart. For instance, in the case of a 4096-point radix-4 Butterfly FFT, the space between 2 neighbor frequency samples is 1024 samples.

If the frequency band to be considered after the FFT calculation is k-sample wide, then the space between each sample to be sent to the DSP is $4^{n-log4(k)}$ samples. The aim of the samples selector was to capture the required output voltage samples knowing their expected output timing. Once the output order is exposed, it is easy to keep the right voltage sample and convert it into digital form. This operation of selection/conversion led to work at a dramatically reduced frequency.

The envelope selection was not limited to the selection of only one RF signal envelope. The output samples representing several envelopes could be buffered to be converted at a lower rate. This is the concept of concurrent reception. Fig. 8 depicts the capture of samples representing two signal envelopes among N samples output by the SASP. It is just a matter of selecting the samples of both envelopes processed from the same received RF signal.

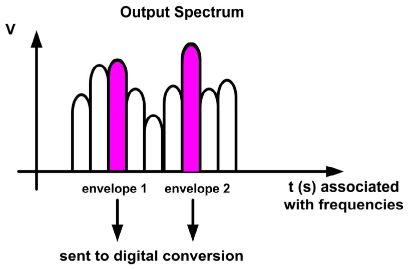


Figure 8: Concurrent reception

5. SASP DESIGN

5.1. Analog implementation

The technology used to design the circuit is the 65nm CMOS technology from STMicroelectronics supplied under 1.2V. The analog implementation of the basic module is mainly concentrated on the design of the delay line and the processing unit. Both of them follow the same design rules

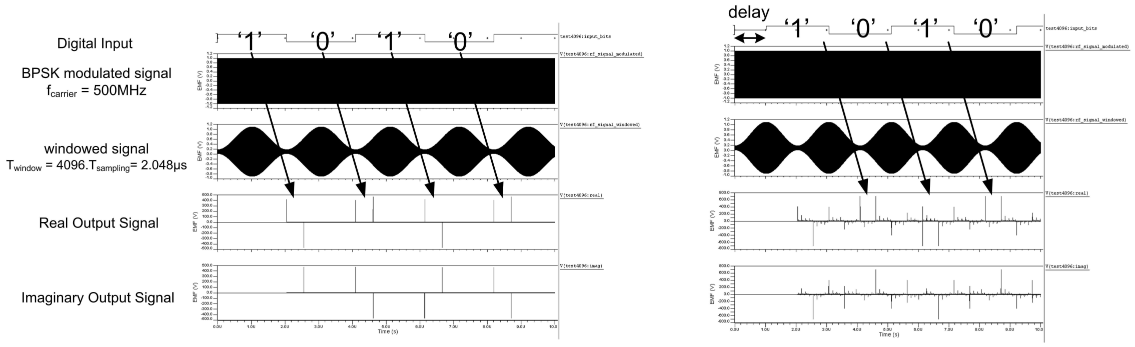


Figure 7: BPSK modulated signal processed by the SASP (a) synchronized (b) non-synchronized

which are used in our processor: the signal is processed with a differential structure with both positive and negative signals centered on a DC voltage of 800mV with a linearity range of 200mV.

5.1.1. The Delay Line implementation

As presented before, the delay line is composed by delay cells implemented by (Fig. 9):

- 2 CMOS switches (one to command the download, one to command the upload of the voltage sample).
- Capacitors to store the samples.

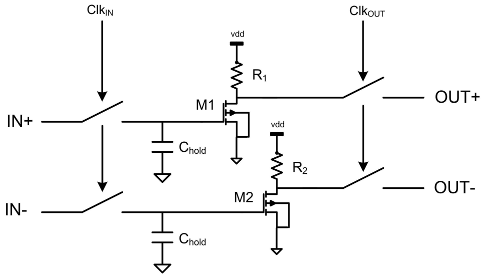


Figure 9: Schematic of a delay cell

Capacitors occupy a major part of the die area. It leads to a trade-off between the capacitor value (as low as possible), the load speed (as high as possible) and the accuracy of the charge transfer (as accurate as possible). The storage capacitor C_{hold} was 50fF.

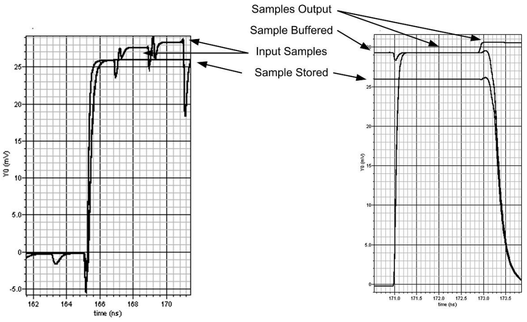


Figure 10: A delayed voltage sample simulation

A voltage sample delayed is simulated in Fig. 10. The inside buffer carried out by resistors R1 and R2 and transistors M1 and M2 amplified by a factor of 1.14 the samples in order to insure a global amplification by 2 of all the circuit to maximize the output dynamic range.

5.1.2. The Processing Unit implementation

The Processing Unit is composed by a Matrix Unit (MU) and a Weighting Unit (WU). Both units are implemented with the same analog structure.

Voltage samples are added and subtracted 4 by 4 in the MU as described in the algorithm matrix in [9]. It is composed by basic adders. Each adder is designed with 4 transistors connected to a common resistor (Fig. 11). Each transistor has a size of W/L=20. The current crossing each transistor is proportional to the input voltage equal to V_{gs}. The current crossing the resistor is the sum of the 4 currents coming from each transistor. Thus, the voltage seen at the drain of the transistors is proportional to the sum of the input voltages. As the circuit is differential, the structure subtracts voltage samples by inverting some of the positive signal input with the negative ones. In Fig. 11 IN3 and IN4 are inverted. Voltage samples on IN3 and IN4 are thus subtracted to those on IN1 and IN2. The Matrix contains adders and mixed adders/subtracters to carry out the FFT calculation.

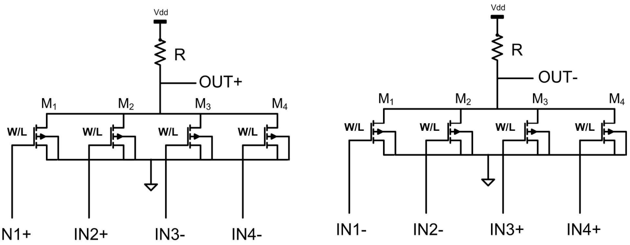


Figure 11: Schematic of the Matrix Unit

WU weights each sample with a coefficient equal to W_N developed in Eq. 1. The real part of the signal is weighted by cos(2π.nk) and the imaginary by sin(2 π.nk) (Fig. 5). Every discrete sample is consequently weighted by a factor within the interval [0,1].

The principle of the voltage/current/voltage conversion coming from the matrix is used to carry out this analog operation.

A switch network (S_x) selects the input voltage of each transistor gate (Fig. 12). The input voltage can be either a voltage sample to be weighted or the DC reference voltage (800mV). The configuration of the switch network determines the coefficient to be applied. Every transistor (M_x) has a different size. It implies that the current crossing each transistor is no more proportional to the input voltage but to the width of the transistor.

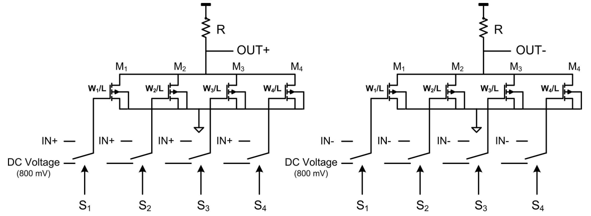
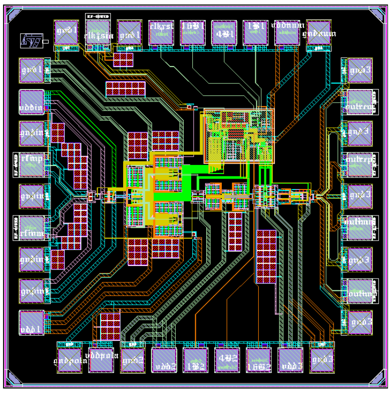


Figure 12: Schematic of the Weighting Unit

5.2. A full analog FFT simulation

The circuit considered here is a 64-point radix-4 FFT processor (Fig. 13). It is a demonstrator sent to foundry to validate the feasibility of the SASP.



Power Consumption
360mW

Dynamic Range
200mV

Maximal sampling
frequency
1GHz

Die Area
1.44mm²

Figure 13: Chip overview of the SASP

A Post Layout Simulation (PLS) is done to validate the circuit behavior taking into account all the parasitic elements (Fig. 14). The SASP carries out analog operations on voltage samples of a sine wave with a frequency equal to $7.f_{sampling}/64=54.6875$MHz. $f_{sampling}$ is equal to 500MHz. Only the 7th voltage samples processed by the processor on a FFT period is selected and displayed to an A/D convertor during all a FFT. It contains the phase and amplitude information of the input signal (Fig. 14). As expected, the spectrum is composed by 2 voltage samples per FFT processed. These samples are thus stored and displayed at the lowest frequency allowed equal to 500MHz/64=7.8125MHz. An A/D conversion is thus possible during that display time (128ns) at a lower frequency and further versions of the SASP with 4096, 16384, 65536 samples can be envisaged.

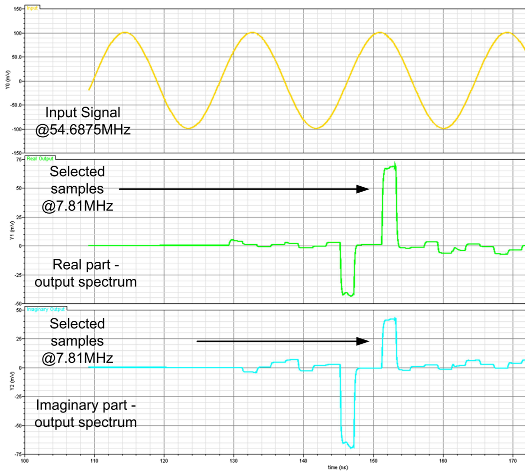


Figure 14: SASP Post Layout Simulation

6. CONCLUSION

The SASP enabled to process RF signals analogically at RF frequencies. It delivered the spectrum of the received signals and selected voltage samples representing the envelope of the signal to be processed digitally. The ADC worked at a dramatically reduced frequency. Once converted, the signal was demodulated by the DSP.

This paper exhibited the behavioral validation of an analog RF Front-End architecture in breakthrough with all the common architectures, compatible with the Software Radio concept. It allowed any channel at any frequency to be received with any modulation and, in addition, paved the way to simultaneous channel reception and to optimized frequency domain demodulation.

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