SDR`08
Washington, D.C. Oct. 26-30
Technical Conference and Product Exposition

A 65nm CMOS RF Front End dedicated to Software Radio in Mobile Terminals

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OUTLINE

- **Software Radio in Mobile Terminals**
- **A Sampled Analog Signal Processor**
  - Principle and System
  - Analog Discrete Electronics
  - Modeling Results
  - Perspectives
- **Conclusion**

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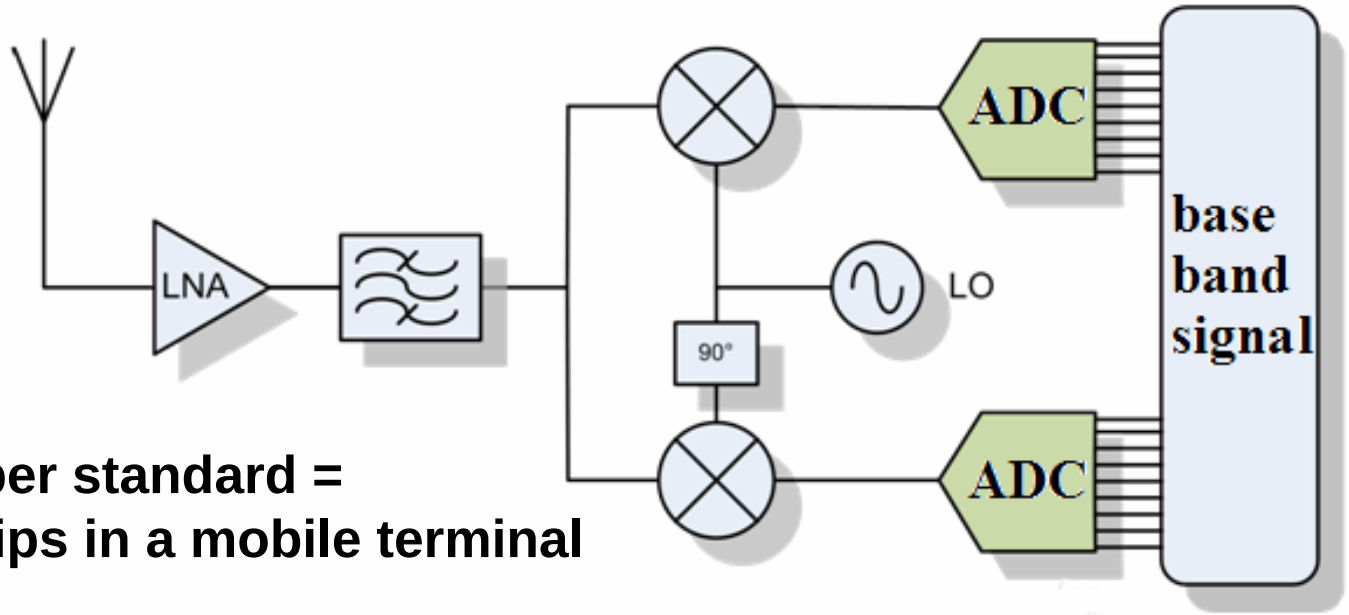
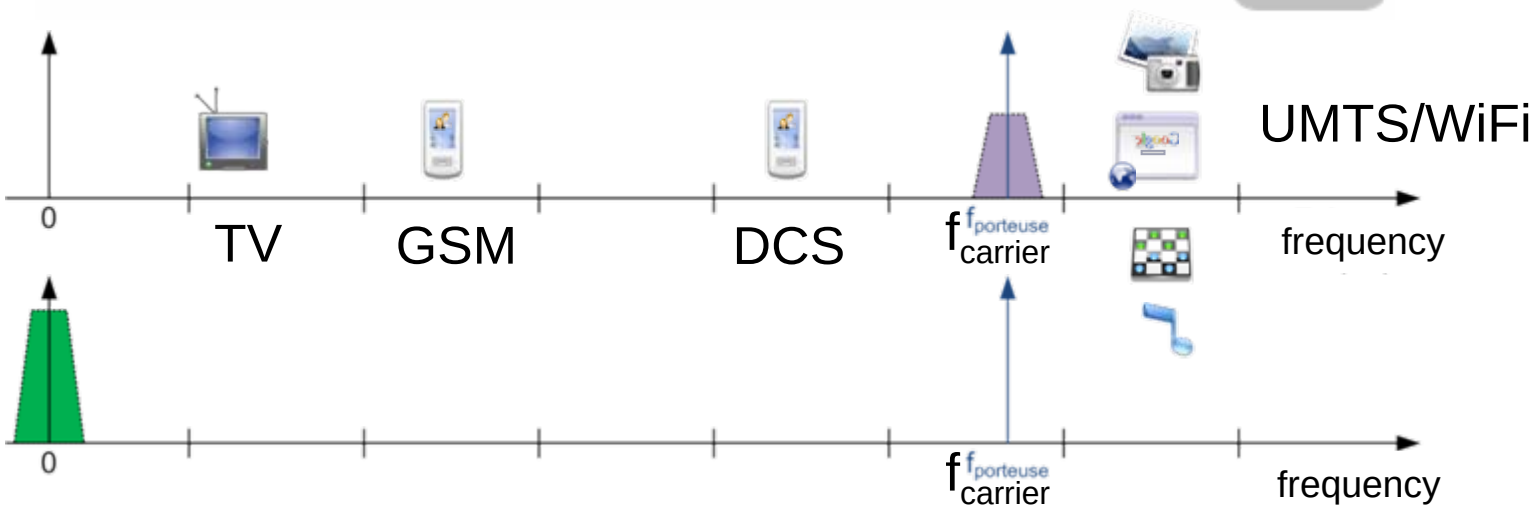
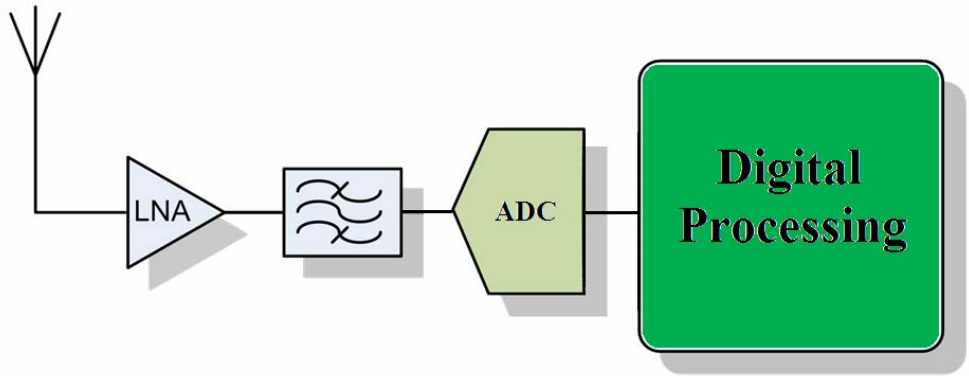
Classical receiving chain



1 chain per standard =
7 to 8 chips in a mobile terminal



Software Radio receiving chain

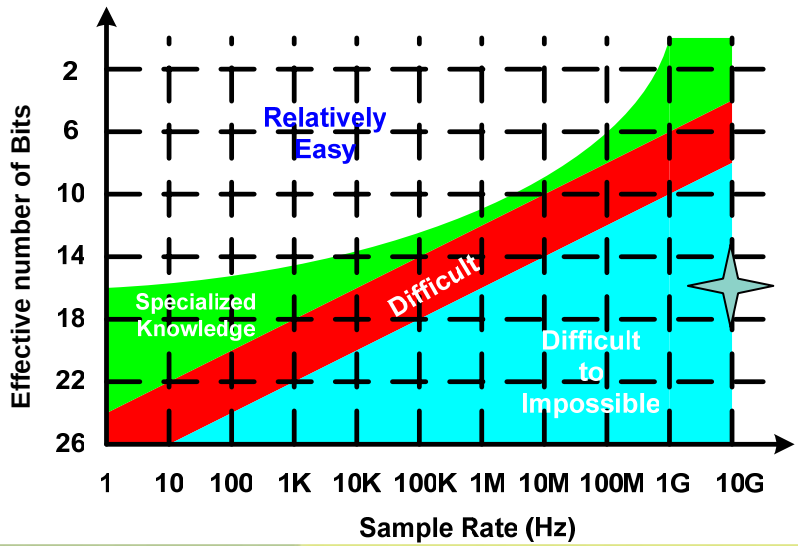


- SR receiving chain

- A/D conversion imposes a high power consumption at RF frequencies and high resolution
- A total SR receiving chain dedicated to mobile terminals is expected to be feasible in 15 years

But …

- Some constraints



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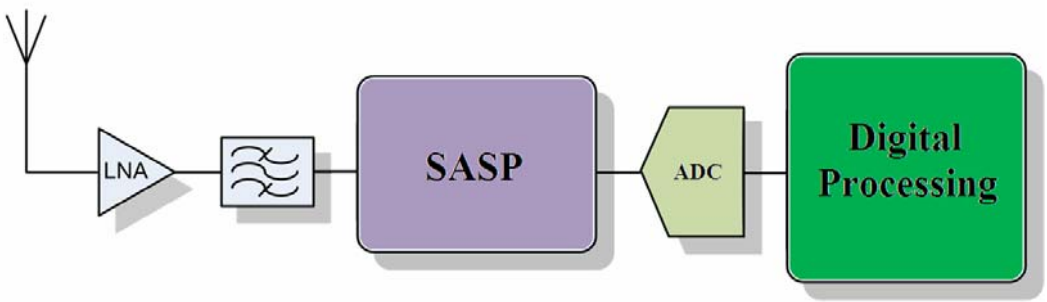
How to make it feasible …

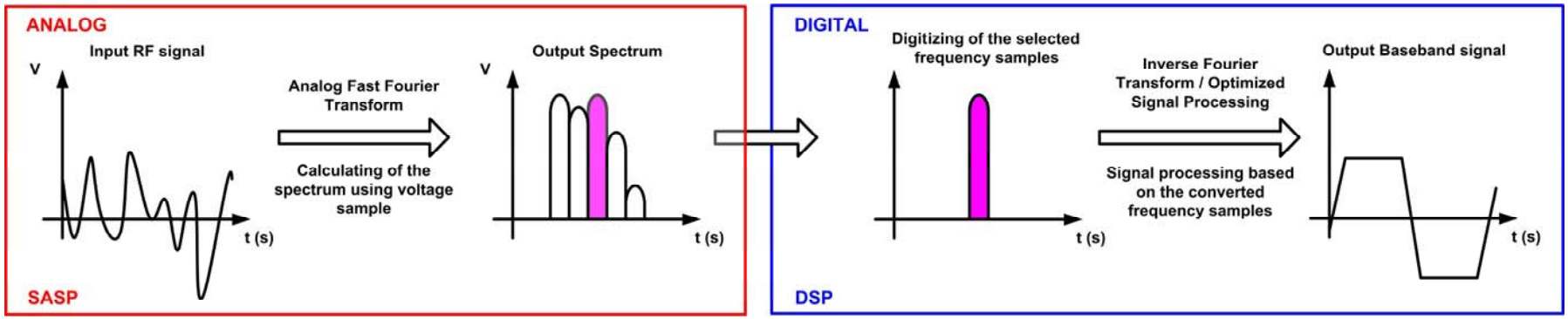
- 2 Ideas are envisaged:
  - An **ANALOG** circuit to work directly at RF Frequencies (10GHz at least)
  - Switch from time-domain to **FREQUENCY**-domain signal processing
- 2 ways to challenge these ideas
  - An Analog Processor working with **VOLTAGE SAMPLES**
  - A time to frequency domain conversion **ALGORITHM**
- A Sampled Analog Signal Processor (SASP) is chosen to interface antenna and A/D conversion



- Proposed SR receiving chain

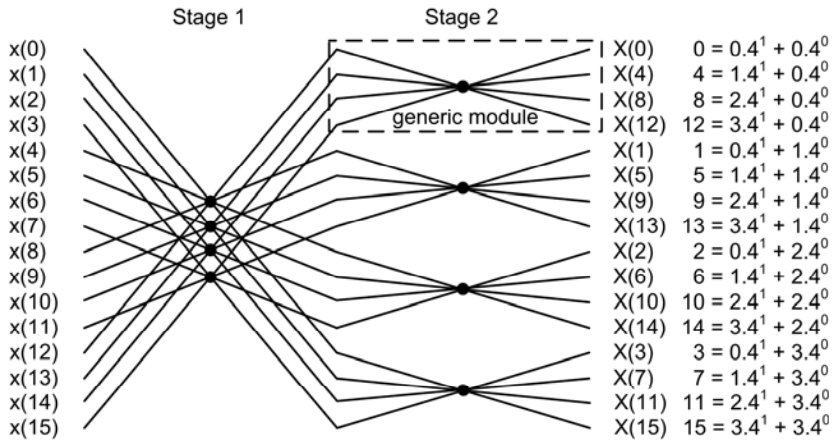
Software Radio Architecture

- A principle: The Frequency Translation

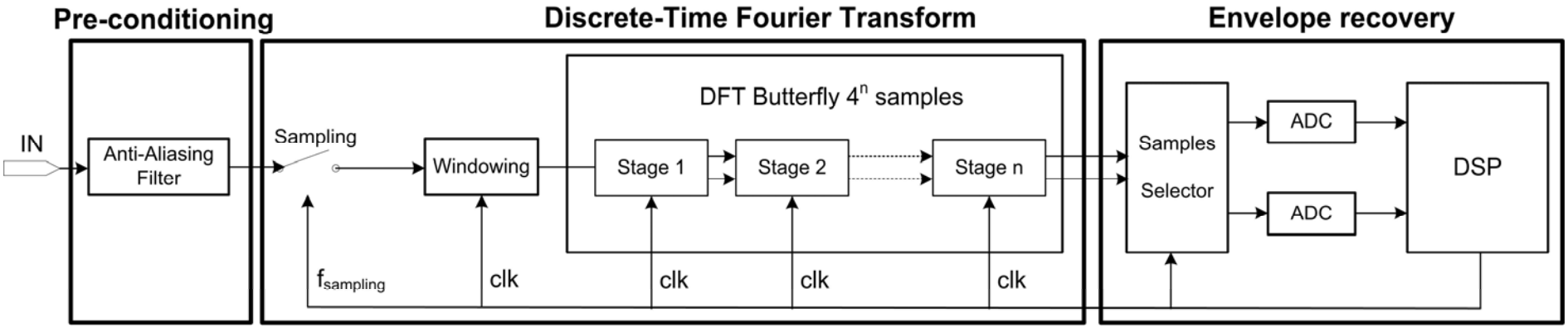


- A way to do it: an Analog Fast Fourier Transform

  - A pipelined FFT is chosen
  - Radix-4 Butterfly algorithm
  - Generic modules are to be implemented analogicaly



Software Radio Architecture

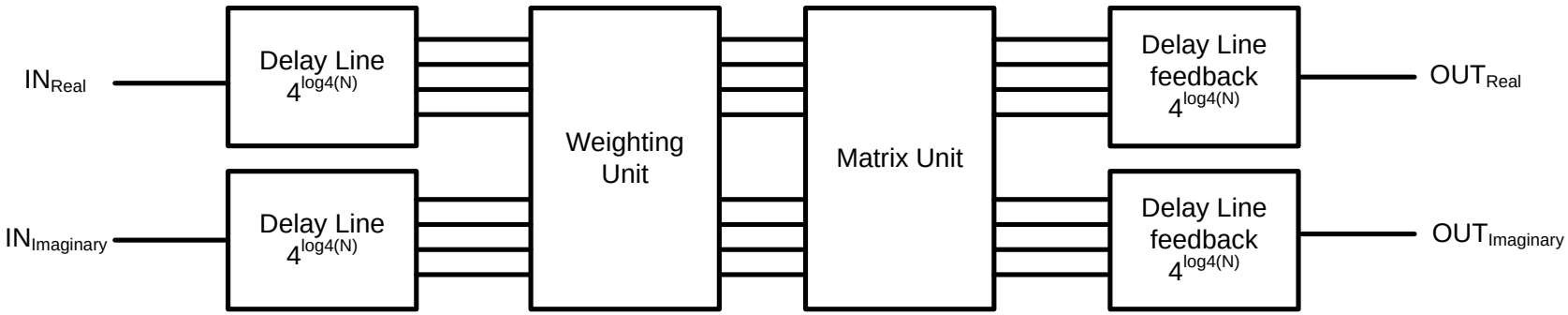


- Analog RF signal processing:
  - Anti aliasing filter
  - Sampling (frequency is the parameter of reprogrammability)

  Avoid interferences and improve FFT calculation
- Discrete Time signal processing
  - Windowing
  - FFT calculation
  - Spectrum output through voltage samples
- Signal envelope recover
  - Samples selections
  - Conversion into numerical to DSP

Discrete Analog FFT

- Composed by generic stages based on the radix-4 butterfly algorithm
- Each stage has the same structure

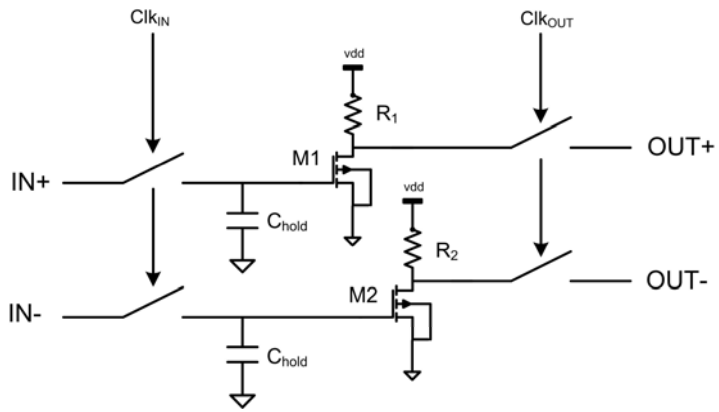


$$\begin{bmatrix} X(k) \\ X(k+\frac{N}{4}) \\ X(k+\frac{N}{2}) \\ X(k+\frac{3N}{4}) \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -j & -1 & j \\ 1 & -1 & 1 & -1 \\ 1 & j & -1 & -j \end{bmatrix} \cdot \begin{bmatrix} W_N^0 F_0(k) \\ W_N^k F_1(k) \\ W_N^{2k} F_2(k) \\ W_N^{3k} F_3(k) \end{bmatrix}$$

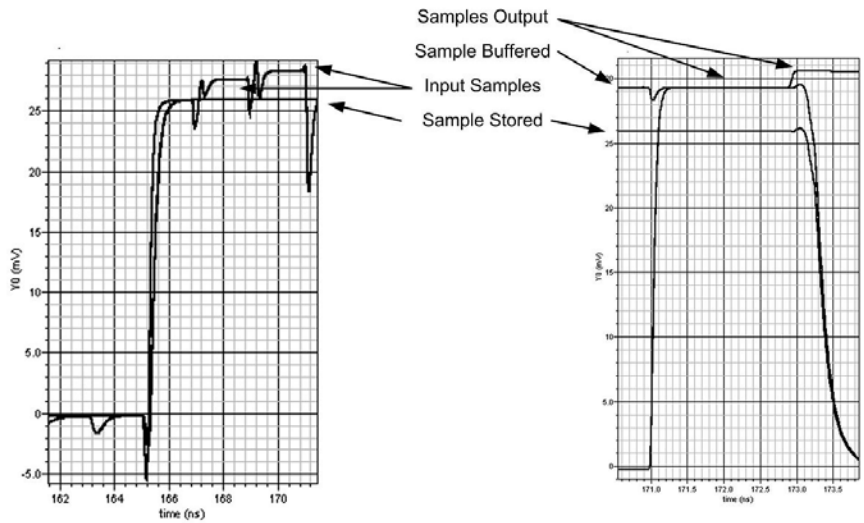
DELAY **ADD** **WEIGHT**

Discrete Analog Operations

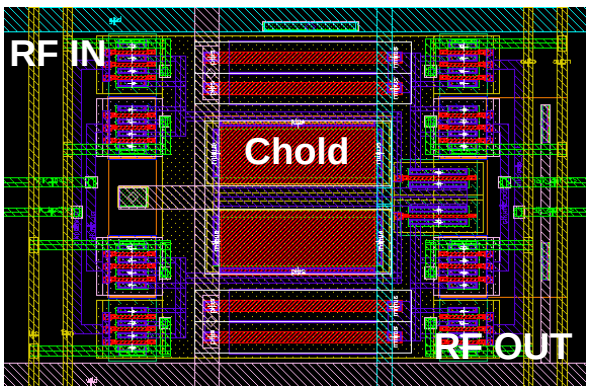
- Delay



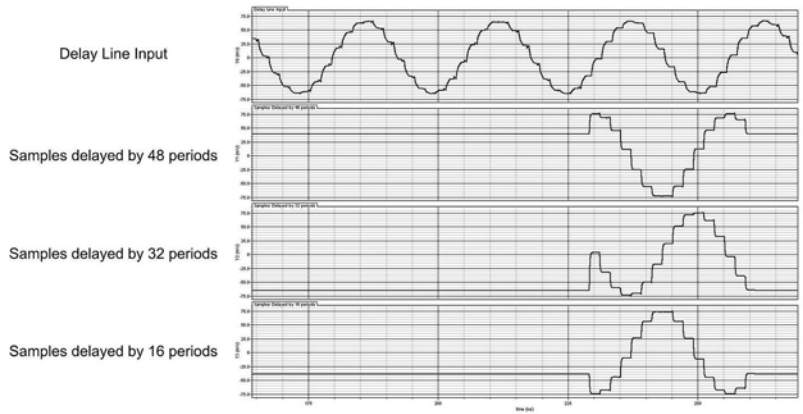
Differential structure



A Charge transfer simulation



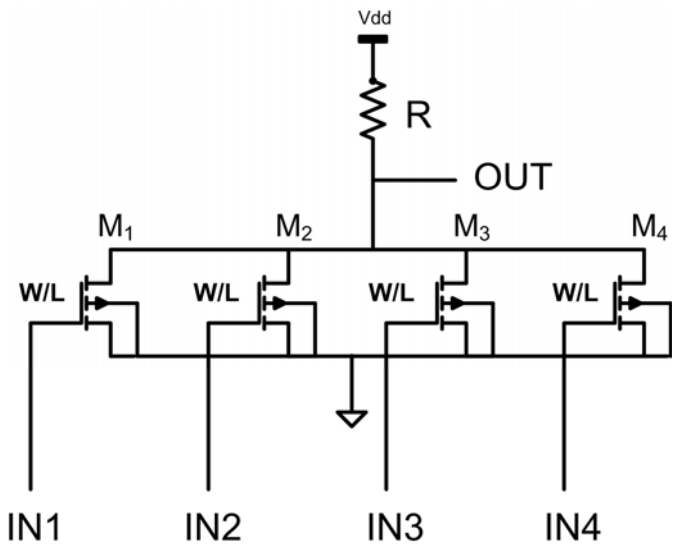
Optimized Layout



A Delay Line simulation

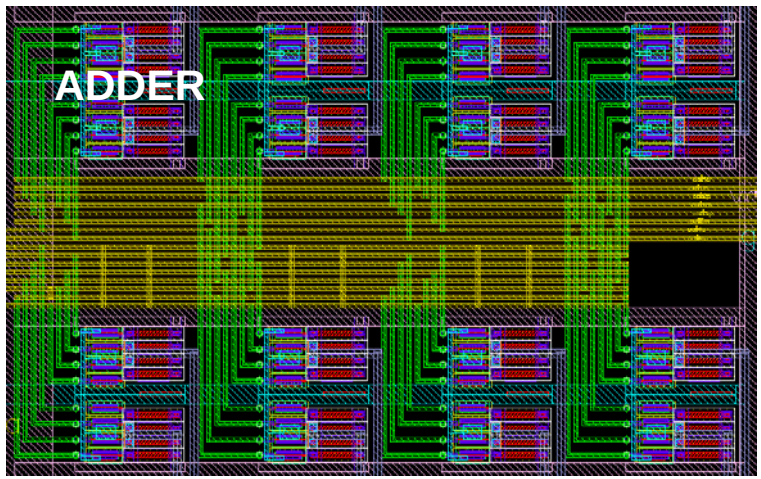
Discrete Analog Operations

- Adder



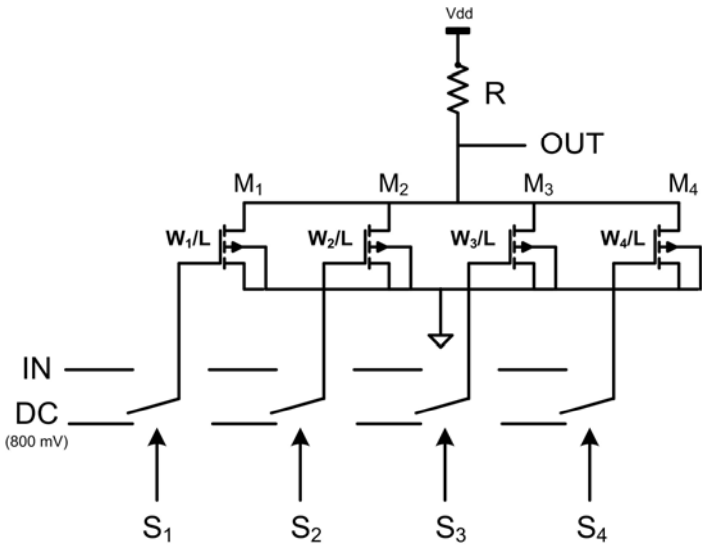
- Voltage samples are converted into current
- Current are added on one node
- The currents sum is converted into voltage

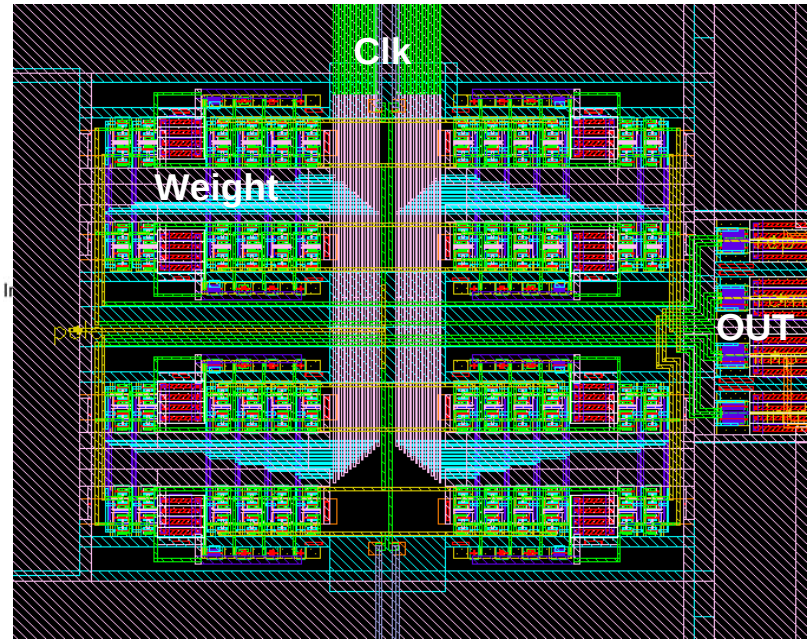
- Each FFT processing stage is composed by a matrix of addition and subtraction
- Adder allows to defined in hardware the add/subtract matrix



Discrete Analog Operations

- Weighter





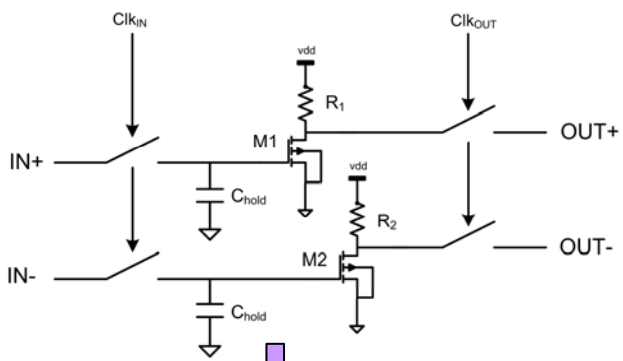
WEIGHTING UNIT COEFFICIENTS APPLICATION

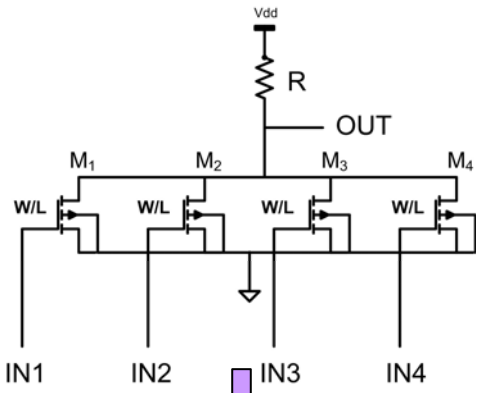
Switch Network Configuration				Coefficients			
S_1	S_2	S_3	S_4				
Transistor Characteristics				For a 100mV input voltage sample simulation			
$M_1\ \frac{W_1}{L} = 2.1$	$M_2\ \frac{W_2}{L} = 5.3$	$M_3\ \frac{W_3}{L} = 7.8$	$M_4\ \frac{W_4}{L} = 9.3$	$cos(2\pi.nk)$	Output	Effective Coefficient	Error
DC	DC	DC	DC	0	0	0	0%
DC	DC	DC	IN	0.383	45.9mV	0.372	2.87%
DC	DC	IN	IN	0.707	84.5mV	0.686	2.97 %
DC	IN	IN	IN	0.924	111mV	0.901	2.48%
IN	IN	IN	IN	1	123.1mV	1	0%

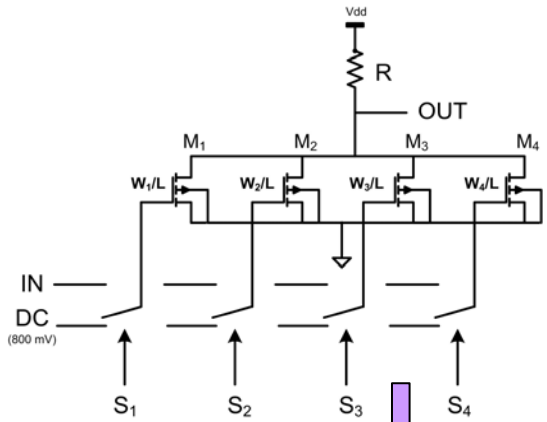
A Sampled Analog Signal Processor

- Three discrete analog operations to perform the FFT

DELAY **ADD** **WEIGHT**







$$W_N = e^{-j(2\pi/N)}$$

$$X(k) = \frac{1}{N}\sum_{n=0}^{N-1} x(n) W_N^{nk}$$

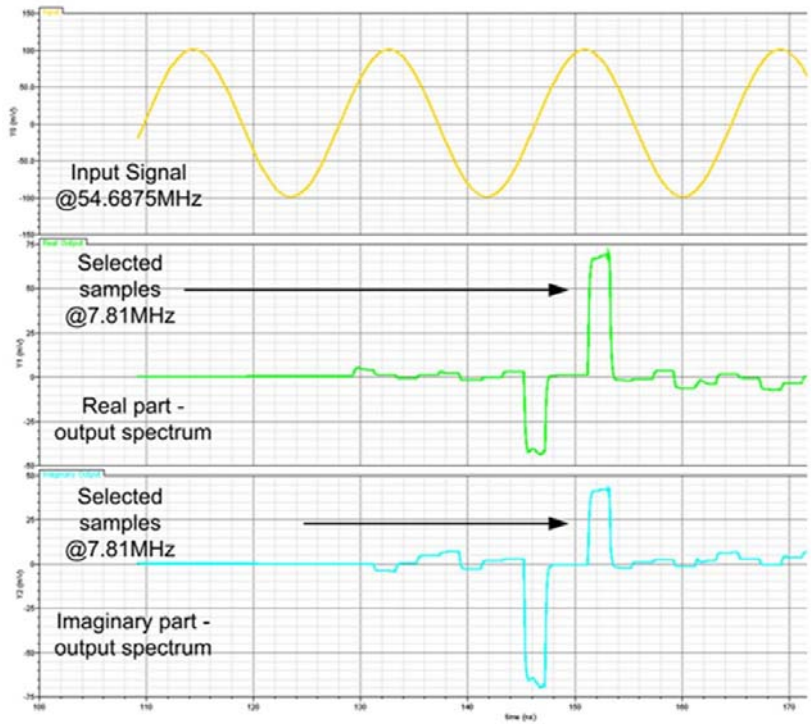
$$W_N = e^{-j(2\pi/N)}$$

- The Analog Fast Fourier Transform is performed by basic analog operations

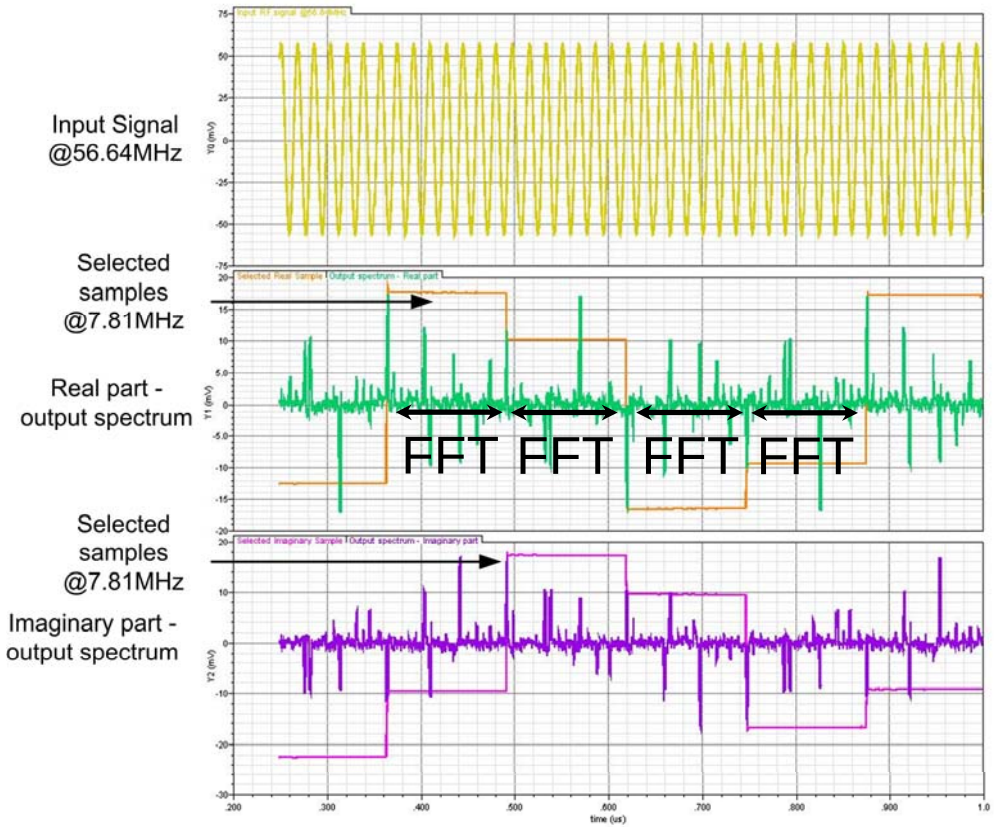
A Sampled Analog Signal Processor

- Simulation of 64-sample SASP

$F_{sampling}$ = 500MHz
F_{in} = 7*500MHz /64



$F_{sampling}$ = 500MHz
F_{in} = 7.25*500MHz /64



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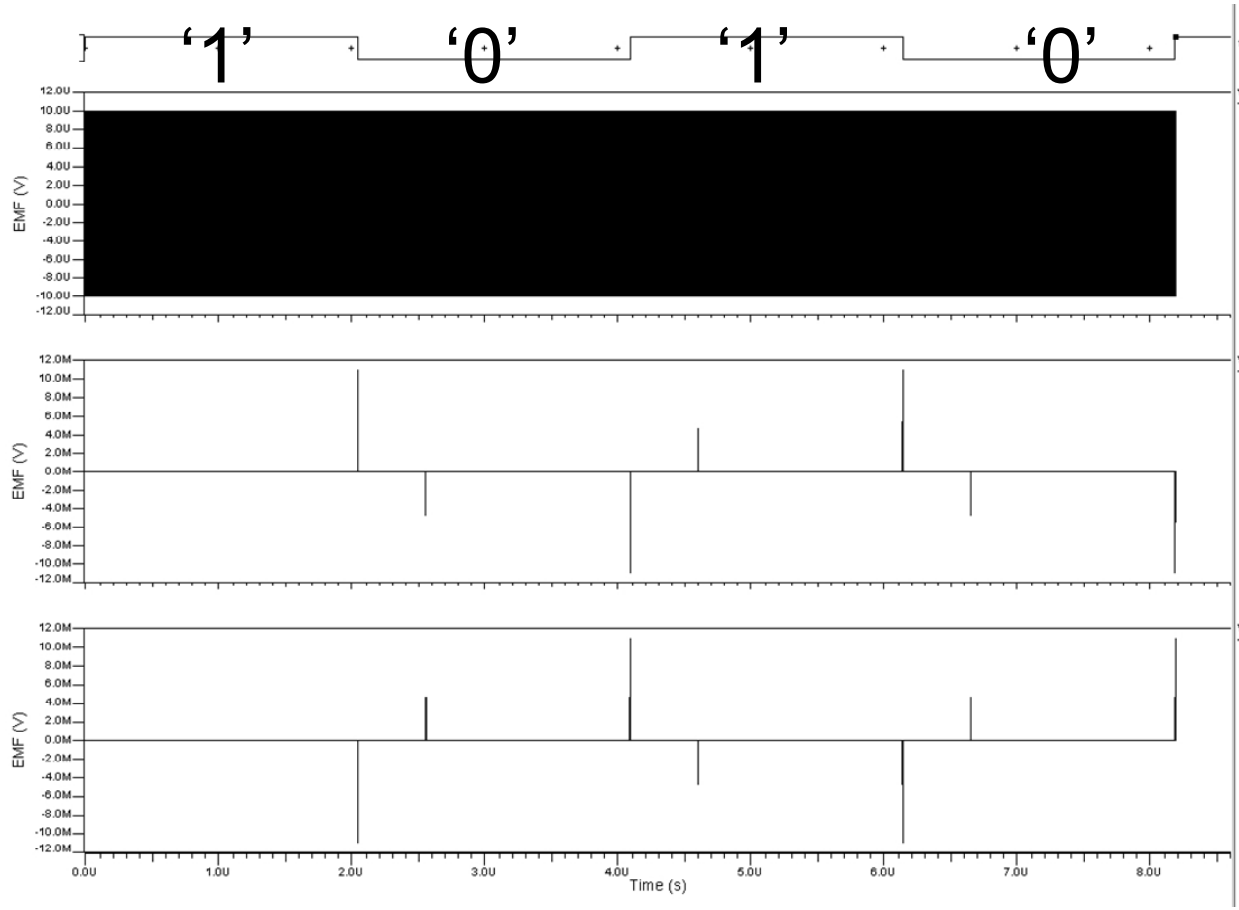
Software Radio simulations

- Frequency Demodulation: BPSK example



Input

BPSK modulation
$f_{carrier}$ = 500MHz

Output SASP:

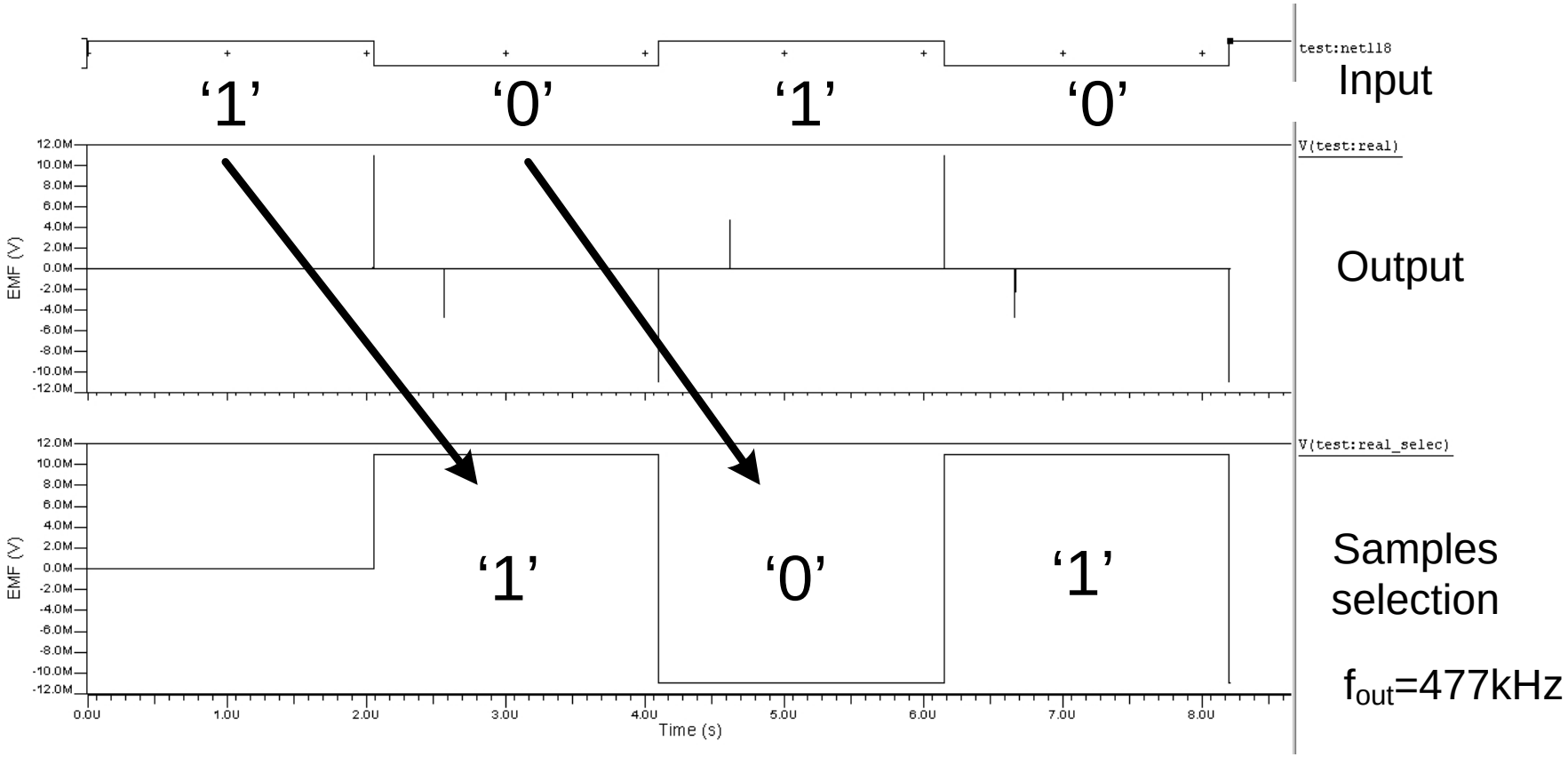
Real Signal

Imaginary Signal

- Bit signatures can be directly recognized into the spectrum

Software Radio simulations

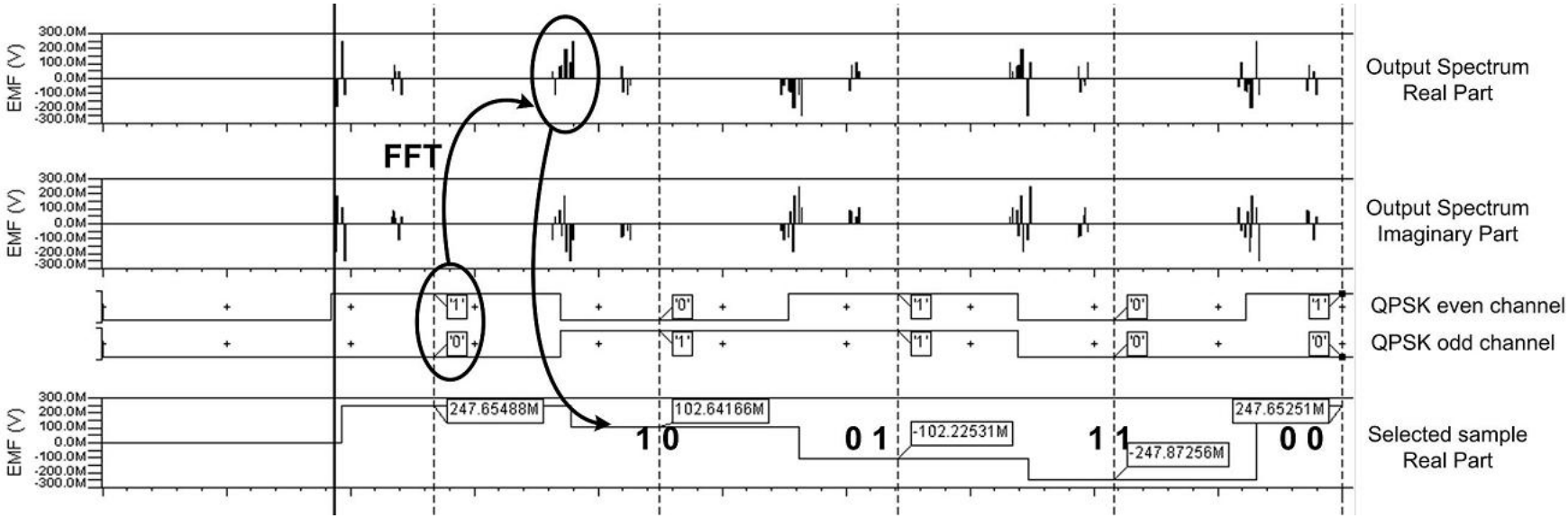
- Frequency Demodulation: BPSK example



- 500MHz → 477kHz : decimation by a ratio of 1000 – ADC and DSP work at low frequencies

Software Radio simulations

- Frequency Demodulation: QPSK example



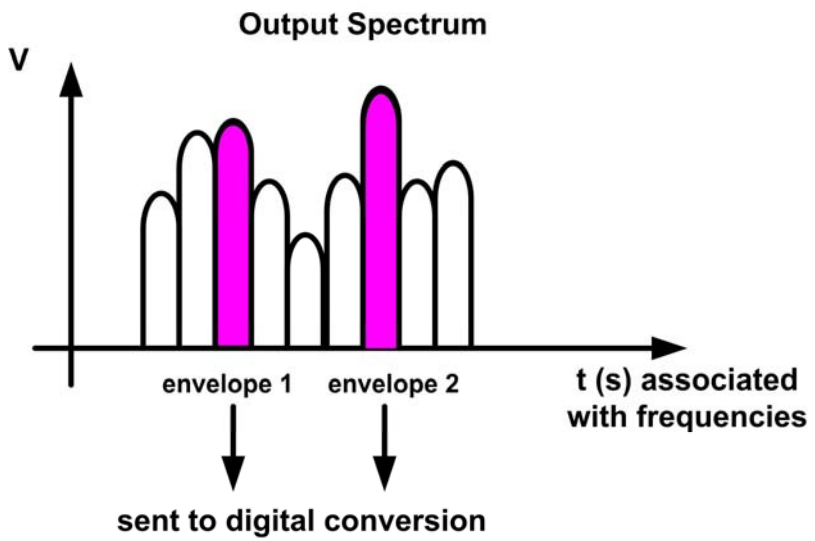
- The four-bit signature can be identified into the spectrum
- Open window to more complex modulation types: 8-QPSK, 16-QAM, 64-QAM

Conclusion

- Optimized algorithm can be developed to demodulate signal into frequency domain – ADC requirements are totally relaxed

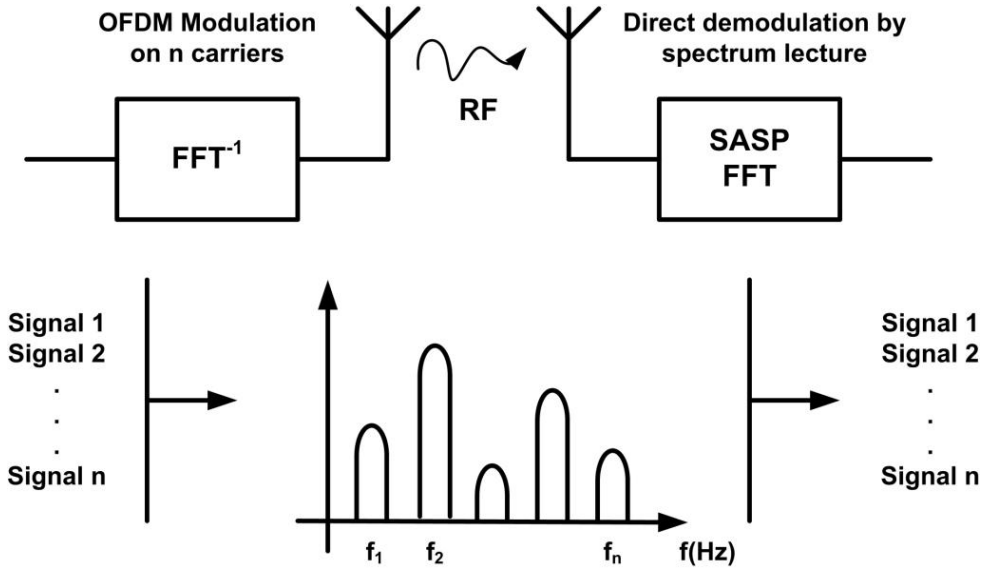
Software Radio simulations

- Concurrent Reception



- Several signal envelops can be processed at the same time
- Military and Security applications: Listen any channel at the same time
- Commercial applications: Multi-applications devices

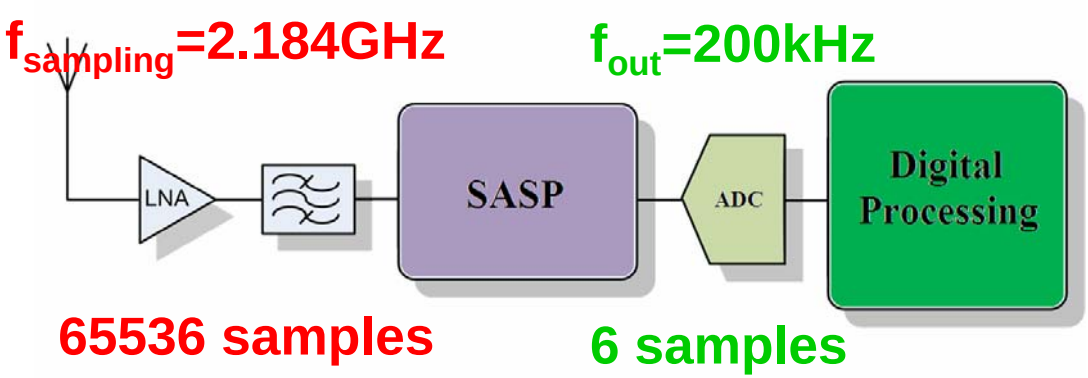
- Direct Reception



- As a FFT is processed, the SASP displays all the sub-carriers of OFDM-modulated signals. The digital part has just to handle the sub-carriers demodulations.

Perspectives:
From a prototype to a final product

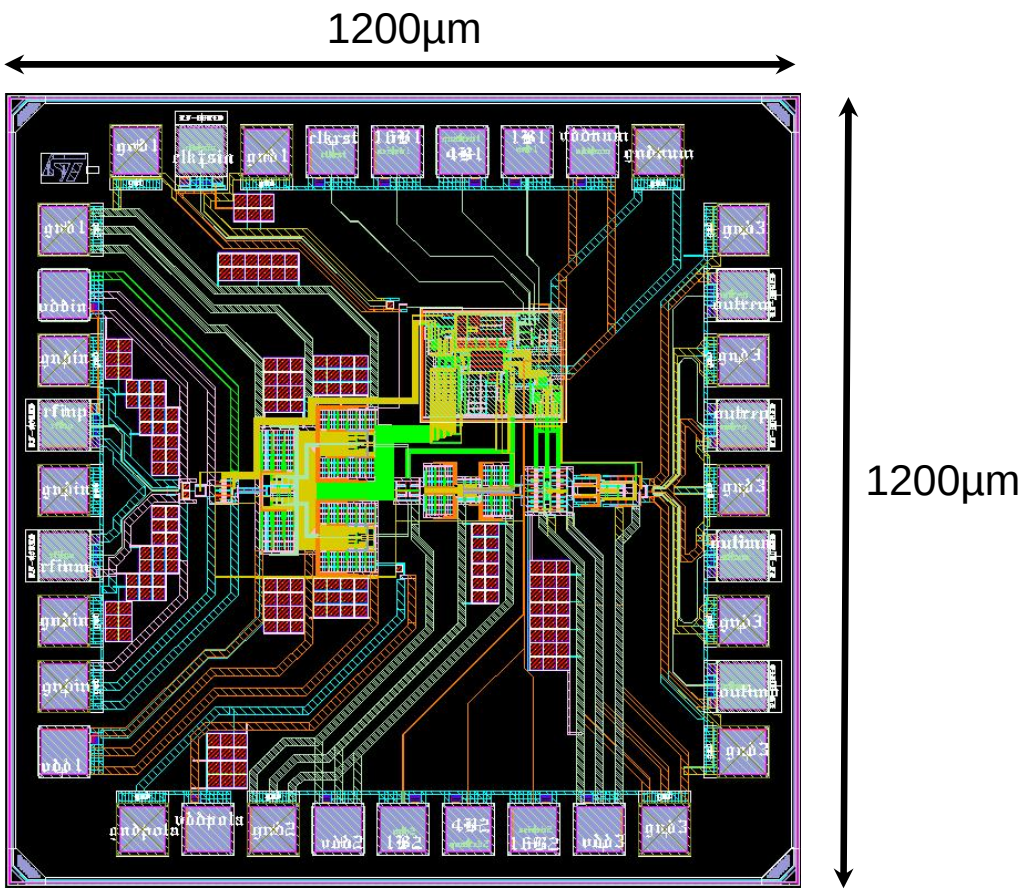
- Example of the GSM standard with a 65536-sample SASP
- T_{bit}=3.69µs, Channel Bandwitdh=200kHz, Carrier Frequency=900MHz



- With $f_{sampling}$=2.184GHz, 6 samples encoding 8 bits are displayed
- A « frequency demodulation » algorithm would support a direct demodulation from the processed spectrum

A Sampled Analog Signal Processor

- Design of a 64-sample SASP



Technology: 65nm CMOS STMicrolectronics

Die Area: 1.44mm²

Maximal Frequency: 1GHz

RF spectrum range covered: 0-500MHz

Power consumption: 360mW

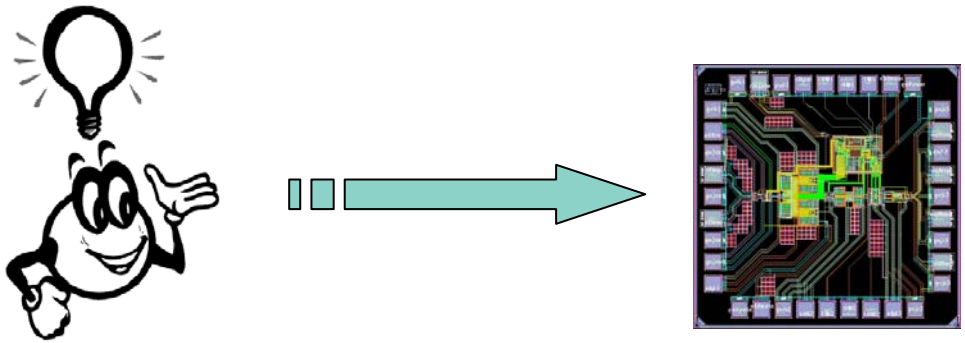
- 64-sample SASP prototype → finalized in a 65536-sample SASP

Conclusion

- The SASP is an Analog Processor in Software Radio receiving chain. It is technically:
  - Low Power (P<500mW)
  - Low Cost (CMOS technology)
  - Small Die Area (IC<5mm²)
  - Relaxes ADC and DSP constraints
- The SASP re-invents RF signal processing:
  - Frequency Demodulation (Optimized demodulation)
  - Concurrent Reception (Resources shared)
- The SASP
  - can be a solution for a true Software Radio architecture dedicated to mobile terminals
  - but … many technological challenges remain to be overcome to achieve an industrial product

Conclusion

- A 65536-sample SASP working at 10GHz is the goal to reach a complete Software Radio Processor



Thank you for your attention,

Any questions ?

Contact Information

Feel free to contact me for more information

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  - Mail: IMS Lab / 351 Cours de la Libération / 33405 Talence Cedex / France
  - PhD. Student – IC Design Team – Software Radio RFIC

- **Main References**
  - « **A Disruptive Receiver Architecture Dedicated to Software-Defined Radio** », *IEEE transactions on Circuits and Systems II 55, 4 (2008) 344-348*
  - « **A Universal Radio Frequency Receiver Architecture Based on Sampled Analog Signal Processing** », *IEEE MWSCAS'07, Montreal, Canada*
  - « **A Disruptive Software-Defined Radio Receiver Architecture Based on Sampled Analog Signal Processing** », *IEEE Radio Frequency Integrated Circuits Symposium, Honolulu, United States, June 2007*