A RECONFIGURABLE SDR RECEIVER FOR MULTI-MODE GNSS APPLICATIONS

Alper Ucar, Ediz Cetin and Izzet Kale

Applied DSP and VLSI Research Group, Department of Electronic, Communication and Software Engineering, University of Westminster, London, United Kingdom
{ucara, e.cetin, kalei}@wmin.ac.uk

ABSTRACT

This paper describes a novel reconfigurable Software Defined Radio (SDR) receiver for the next-generation GPS and Galileo Global Navigation Satellite Systems (GNSS). The proposed receiver utilizes variable–rate BandPass Sampling (BPS) to downconvert the signal of interest to an Intermediate Frequency (IF) thereby simplifying the Analog Front-End (AFE) as well as rendering the simplified AFE mostly free of the perennial RF-impairments. A Continuous-Time (CT) quadrature bandpass sigma-delta ($\Sigma\Delta$) modulator is used for data conversion which circumvents the need for an anti–alias filter and relaxes the RF band select filter specifications by attenuating adjacent band interference through its loop filter. System level simulations demonstrate that the BPS receiver with a CT $\Sigma\Delta$–ADC is a feasible option that leads to reduced power consumption and high levels of integration making single chip radio receivers realistically viable.

1. INTRODUCTION

Third-generation (3G) mobile systems have introduced new standards and services, and it is anticipated that 4G will focus on integrating existing wireless standards on a single universal radio platform. With the development of the European navigation system Galileo and the modernization plan for GPS, integration of wireless communication systems with GNSS will become a practical reality thereby providing an important platform for the provision of a number of Location Based Services (LBS) as well as navigation information. It is evident that a flexible radio platform is needed that can be configured to tune into the bands of interest complying with the modulation standard and adapt to a dynamic communication environment to achieve acceptable performance.

The Software Radio (SR), envisioned in [1], is a wishful solution to this demand in which all RF and baseband processing is done in the digital domain. However, this puts extreme requirements on the Analog-to-Digital Converter (ADC) in terms of sampling rate, dynamic range, and power dissipation such that a feasibly conceivable solution will not be available in the near future.

An alternative solution is to utilize BPS to relax the requirements of the ADC since the sampling rate reduces to twice that of the information bandwidth. A practical version of SR is the SDR in which the RF signal is sampled after a suitable band selection filter and a Low–Noise Amplifier (LNA) [2]. In order to support the idea of SDR, the ADC should be placed as near to the antenna as possible thereby minimizing the number of analog components required. An SDR platform utilizing a BPS ADC with variable sampling rate seems to be a viable option today to achieve wideband reception. The goal of this paper is to derive the requirements of the BPS receiver front-end by providing a signal chain noise analysis for the next-generation GNSS applications.

The paper is organized as follows. Section 2 introduces BPS for the open service GNSS signals. Section 3 analyzes the design considerations for the receiver and Section 4 presents the experimental results. Finally the concluding remarks are given in Section 5.

2. BANDPASS SAMPLING FOR GNSS SIGNALS

Open service radionavigation signals will be in multiple bands within the next decade, as depicted in Figure 1, offering improved position accuracy and robustness against multipath and interference effects. Therefore, the next generation radionavigation terminal has to be a flexible wideband receiver able to tune into different bands as and when desired and to dynamically sense and adapt to the environmental conditions (i.e. the presence of interferers). However, realization of such a receiver is not feasible today mainly due to the requirements on the AFE and the ADC. The current ADC technology is not mature enough to provide direct RF sampling at Nyquist. On the other hand, utilizing LowPass Sampling (LPS) at IF to process multi-frequency signals is still a challenging task due to the need for off-chip analog filters and high-frequency local oscillators which makes it difficult to integrate the receiver monolithically.

Wideband reception in the receiver may be achieved by employing BPS which is a subsampling technique by intentional aliasing of the signal band of to realize

frequency downconversion. One of the challenges in BPS is determination of the sampling rate.
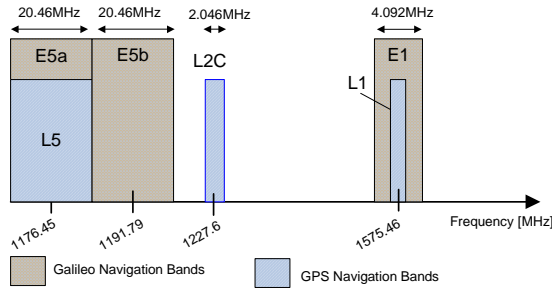

Figure 1. Open Service GNSS Bands

The sampling rate needs to be chosen carefully in order to minimize signal aliasing from adjacent spectral replicas. The conditions for the acceptable uniform bandpass sampling rates can be written as [3]:

$$\frac{2f_u}{m} \le f_S \le \frac{2f_l}{m-1} \qquad (2.1)$$

where f_u is the upper and f_l is the lower frequency of the bandpass signal, B is the signal bandwidth, f_S is the uniform BPS rate and m is the subsampling factor given by:

$$1 \le m \le \frac{f_u}{B}. \qquad (2.2)$$

When a fixed sampling rate is to be chosen for multi-band signals, the spectral replicas of the signals at different bands must be placed in a particular order in the frequency spectrum to minimize aliasing as before. The Ladder diagram concept reported in [4] has been used for the open service E1–L1, L2C, E5a–L5, and E5b GNSS bands and is illustrated in Figure 2. As can be observed from the figure, the minimum feasible sampling frequency is approximately 165 MHz since going below that will result in two or more bands overlapping. Moreover, if it is desired to incorporate commercial service radionavigation bands, the sampling rate might be significantly increased up to 331 MHz [5]. Compared to LPS, high sampling rates will result in significant overhead that leads to large power dissipation in the ADC as well as the DSP. One solution that can avoid high sampling rates is to subsample and therefore downconvert one navigation band at a time and adjust the sampling frequency with respect to the desired signal and environment conditions. A slight drawback of this approach is the need to accurately generate more than one clock frequency which may be favorable as opposed to working at much higher data rates.
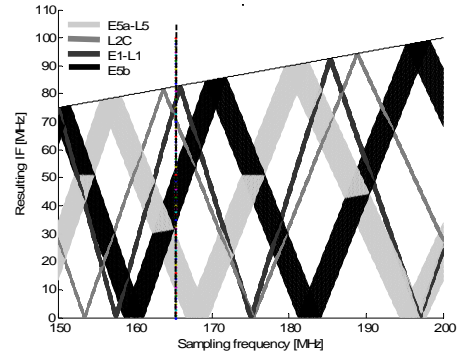

Figure 2. Ladder Diagram for Open Service GNSS Bands

3. DESIGN CONSIDERATIONS

GNSS applications require very strict Noise Figures (NFs) since the received signal power at the antenna is well below the thermal noise floor and it will remain so until a digital correlator at the digital backend successfully tracks the signal. As an example, the signal power level of the Galileo E1 band (32.73 MHz), depicted in Figure 3, has a Signal-to-Noise Ratio (SNR) of –26 dB at the receiver antenna. This will improve when an appropriate PseudoRandom Noise (PRN) code is successfully correlated with the signal. The improvement is called the processing gain, G_p, which is given by [6]:

$$Gp = 10\log\left(\frac{f_{PRN}}{f_d}\right) \qquad (3.1)$$

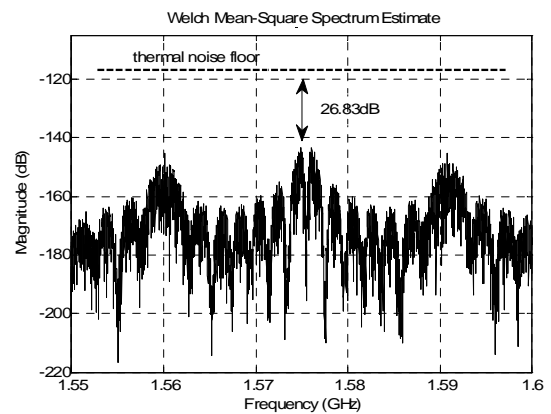where f_{PRN} is the code rate and f_d is the data rate.

Figure 3. Galileo E1 Signal at the Antenna

Table I. Signal Levels for Open Service GNSS Bands

	GPS			Galileo					
	L1 C/A	L2C	L5	E1		E5a		E5b	
Carrier Frequency [MHz]	1575.46	1227.6	1176.45	1575.46		1176.45		1207.14	
Min Received Power [dBW]	-127.66	-130.0	-124.0	-125.69		-125.0			
				B	C	I	Q	I	Q
Code Rate [Mchips/s]	1.023	1.023	10.23	1.023	1.023	10.23	10.23	10.23	10.23
Gp [dB]	43.1	43.1	53.1	43.1		53.1		53.1	
Input SNR	-16.7	-19.1	-23.1	-17.8		-24.1		-27.9	
Post-correlation SNR [dB]	26.3	24.0	30.0	25.2		29.0		25.1	
Required NF$_{AFE+ADC}$ [dB]	16.3	14.0	20.0	15.2		19.0		20.11	

The required NF of the AFE and the ADC can be written as:

$$NF_{AFE+ADC} = P_{IN} + N_0 + G_p - SNR_{min} \qquad (3.2)$$

where P_{IN} is the received signal power, $N_0 = -174$dBm/Hz is the thermal noise power density, and SNR_{min} is the minimum required SNR to be able to successfully track the navigation signal. Table I presents the signal levels of the open service GNSS bands (using 3.2) when the minimum required SNR at the output of a digital correlator is assumed to be 10 dB. As can be seen, the most stringent NF requirement on the AFE and the ADC is for the GPS L2C signal which is approximately 14dB.

3.1. Analog-to-Digital Converter

Although the ADC comes after the AFE in the signal chain, it needs to be analyzed first in order to derive the requirements of the AFE. Traditionally $\Sigma\Delta$ modulation techniques have been applied to narrowband signals. Switched–Capacitor (SC) $\Sigma\Delta$ modulators reported in the literature so far have bandwidths not much greater than 10MHz [7], [8], with the exception of [9] having a bandwidth of 40MHz. Since the output of each SC integrator must settle between two clock pulses and the maximum clock frequency is limited by the required precision, the task of deriving wideband SC $\Sigma\Delta$ modulator is difficult [10]. On the other hand, recent published CT $\Sigma\Delta$ modulators operate up to a few GHz [11], [12]. CT $\Sigma\Delta$–ADCs having programmable bandwidth and dynamic range have also been reported in the literature [13], [14]. Apart from the wideband E5 signal, current IC technologies are able to facilitate bandpass $\Sigma\Delta$–ADCs for the open service GNSS bands. The composite E5 band has 2 subbands, E5a and E5b each with a bandwidth of 20.46MHz which are convenient to process individually.

The prominent benefit of utilizing a CT $\Sigma\Delta$ modulator, shown in Figure 4, is that the anti–alias filter requirement may be circumvented since it provides inherent anti–alias filtering on the input signal path [15], [16]. This feature can also be exploited to relax the Q–factor of the RF filter by letting the CT $\Sigma\Delta$ modulator filter out some of the adjacent band interferers.
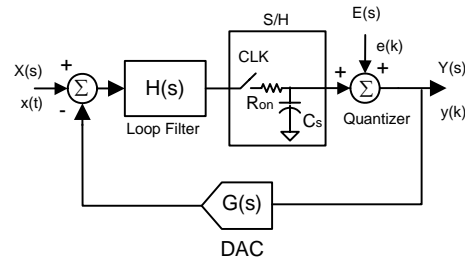

Figure 4. Block diagram of the linearized CT $\Sigma\Delta$–ADC

The output of the modulator in Figure 4 can be written as:

$$Y(s) = \frac{H(s)X(s)}{1 + H(s)G(s)} + \frac{1}{1 + H(s)G(s)}E(s) \qquad (3.3)$$

where $H(s)$ is the CT filter transfer function and $G(s)$ is transfer function of the Digital–to–Analog Converter (DAC). Equation 3.3 can be written in the z–domain as:

$$Y(z) = \frac{H(z)}{1 + K(z)}X(z) + \frac{1}{1 + K(z)}E(z) \qquad (3.4)$$

In (3.4) $K(z)$ is the z–domain loop transfer function which is defined as:

$$K(z) = Z\left\{ L^{-1}\left[H(s)G(s) \right]\big|_{t=nT_s} \right\} \qquad (3.5)$$

where T_s is the sampling time and $n = 0,1,2,...$ is the sampling index. Using (3.4) and (3.5), the Signal Transfer Function (STF) can be defined as:

$$STF(z) = \frac{H(z)}{1+K(z)} \qquad (3.6)$$

The transfer function for the CT filter can be express as:

$$H(s) = \frac{As}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2} \qquad (3.7)$$

where A is the gain, ω_c is the angular carrier frequency, and Q is the filter quality factor. The transfer function of the DAC for ease of analysis will be approximated as a zero–order hold:

$$G(s) = \frac{1 - e^{-sp}}{s} \qquad (3.8)$$

where p is the opening aperture. For a Return–to–Zero (RZ) DAC $p=T/2$, and for a Non–Return–to–Zero (NRZ) DAC $p=T$, where T is the sampling period. Substituting 3.7 and 3.8 into 3.6 gives the STF in the z–domain [15]:

$$STF(z) = H(z)\frac{1 + e^{-p\frac{\omega_c}{Q}}z^{-2}}{1 + ge^{-0.5p\frac{\omega_c}{Q}}z^{-2} + \left(e^{-p\frac{\omega_c}{Q}} - ge^{-0.5p\frac{\omega_c}{Q}}\right)z^{-2}} \qquad (3.9)$$

To see the effect of the Q–factor on the STF of the E1–L1 band, the magnitude spectrum is plotted in Figure 5 for different values of Q.
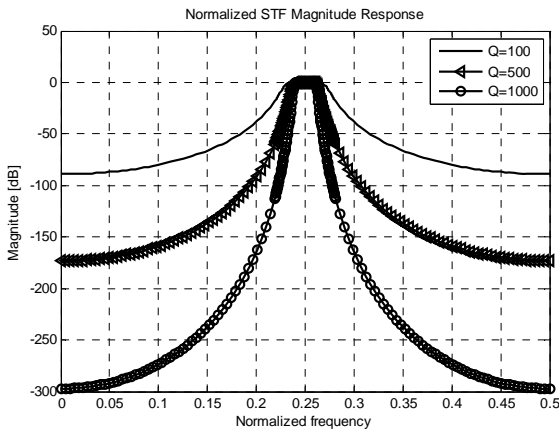
Figure 5. Difference in normalized STF for Q values of 100,500, and 1000

The attenuation of the anti–alias filter at an image frequency can be approximated as [16]:

$$\text{Attenuation} \approx \frac{1}{\sqrt{\left(\frac{2Q}{m}\right)^2 k^2 + 1}} \qquad (3.10)$$

where k is the index for the image. The graph in Figure 6 illustrates the relation between Q/m ratio and image attenuation. Notice that 20dB attenuation of the first image requires a Q factor that is 5 times the subsampling ratio, m.
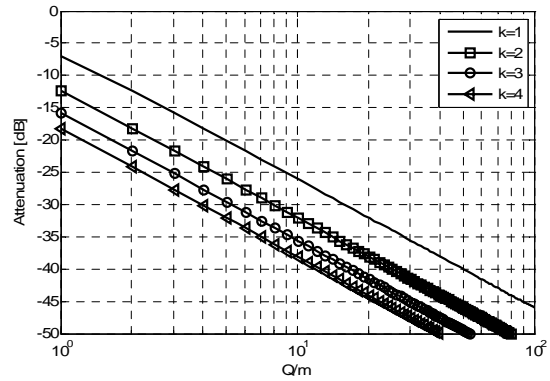
Figure 6. Image attenuation as a function of Q/m for k=1,2,3, and 4

The resulting SNR of the ADC is the key design parameter in the BPS receivers since the effects of non-idealities will be amplified due to subsampling. The dominant noise sources in an ADC that utilizes BPS are quantization noise, wideband thermal noise, and the S/H clock jitter noise. Assuming that the quantization noise is distributed over the Nyquist band, the quantization noise can be defined as [17]:

$$P_q = \frac{\Delta^2}{12} = \frac{V_{p-p}^2}{6N^2} \qquad (3.11)$$

where Δ is the quantization step, V_{p-p}^2 is the peak–to–peak voltage swing of the ADC, and N is the number of quantization levels. The S/H circuit can be modeled as a Switched–Capacitor (SC) in which the input voltage charges the capacitor, C_s, through the switch. At the end of the sampling time, the switch turns off and the capacitor holds the input voltage as well as the noise introduced by the on-resistance, R_{on}, of the switch. The noise introduced by the sampling switch can be estimated by assuming that the total noise power kT/C_s is sampled by the subsampling rate given as [18]:

$$P_{th} = \frac{kT}{C_s} \times \frac{2B}{F_s} \qquad (3.12)$$

where k is the Boltzmann constant and T is the absolute temperature.

The aperture jitter on the S/H clock, defined as the uncertainty in time between the effective sampling intervals, will result in phase noise. The jitter noise power for a given sinusoidal input signal, $Asin(2\pi f_c)$, can be written as:

$$P_j = P_s \left(m2\pi f_c \sigma_j \right)^2 \qquad (3.13)$$

where P_s is the sampled signal power and σ_j^2 is the variance of the jitter error. Notice that the SNR degradation on thermal noise is proportional to the subsampling ratio while the SNR degradation on sampling jitter is proportional to the subsampling ratio squared since $\sigma_j^2 << 1/f_s$.

In CT $\Sigma\Delta$−ADCs since both the Sample–and–Hold (S/H) and the quantizer circuits are inside the feedback loop, noise generated by their non-ideal operation can be shaped out. Figure 7 illustrates the output spectrum of the forth order CT and SC $\Sigma\Delta$ modulators when a sinusoidal input signal (used for convenience to evaluate the SNR) is applied.
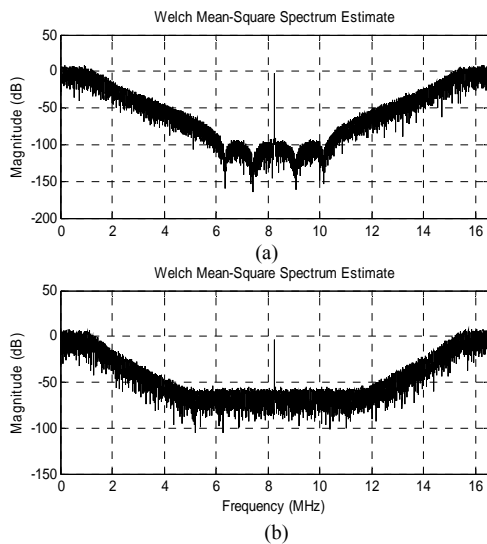

(a)

(b)

Figure 7. Illustration of the noise shaping in a forth order (a) CT $\Sigma\Delta$–ADC (b) SC $\Sigma\Delta$–ADC for the E1–L1 band with a subsampling rate of 32.99 MHz.

3.2. AFE

A block diagram of the proposed GNSS receiver is presented in Figure 8. To the author's best knowledge, the AFE of the receiver is the simplest architecture among the GNSS receiver front-ends. It consists of adjustable LNA and limiting amplifier (LA) to be able to achieve the required NF and a tunable RF bandpass filter for blocking out–of–band interferers. Realization of the fully integrated tunable RF filters has been reported recently in [19], however, achieving high Q on a mixed signal integrated

solution is still a challenging task. For this reason, we propose a relaxed Q−factor topology in which adjacent out−of−band interference is attenuated by the CT $\Sigma\Delta$–ADC. The RF filter with a bandwidth of 50 MHz will have a Q factor of approximately 30 for E1–L1 band. This eliminates the need for a SAW filter and makes the RF filter viable with the current IC technology. The simplified AFE also minimizes the signal distortion caused by the RF impairments [20], [21] since quadrature mixer and parallel I/Q paths are eliminated.
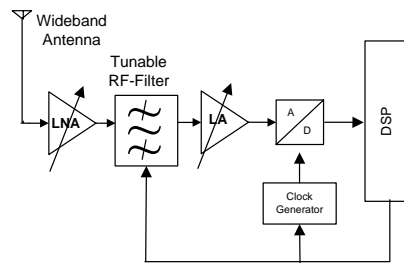

Figure 8. Proposed Bandpass Sampling GNSS Receiver Architecture

5. EXPERIMENTAL RESULTS

In order to study, analyze and evaluate the performance of the receiver, a behavioral model of the RF transmitter and the BPS receiver has been developed in Simulink™ as illustrated in Figure 8. A GPS/Galileo signal generator block [22] generates the desired signal as well as MPSK interference. Sampling clock jitter and thermal noise associated with the S/H circuit is introduced in the CT $\Sigma\Delta$ modulator.
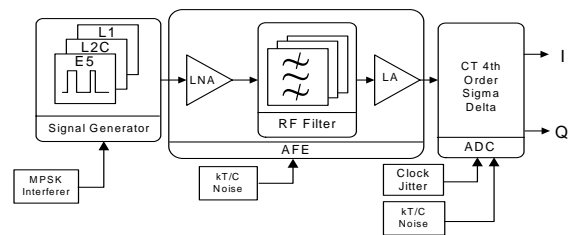

Figure 9. Behavioral Model of the RF Transmitter and the BPS Receiver

Subsampling rates and the resulting SNR of the 4th order CT $\Sigma\Delta$-ADC is determined experimentally and given in Table II in which P_N denotes the noise power. The required gain and noise budget for the AFE is derived from the requirements of the $\Sigma\Delta$ modulator. Since the noise floor in the $\Sigma\Delta$ modulator is around -73dBm, the signal power should be raised above this level in order to get sufficient signal power at the output of the ADC. Table III presents the gain and noise budget for the L2C band which is the worst–case scenario.

Table II. Sampling Rates and Resulting SNR for the GNSS Bands

Band	f_c [MHz]	B [MHz]	Fs [MHz]	P_N [dBm]	SNR$_{CT\Sigma\Delta}$ [dB]
E1–L1	1575.4	4.092	32.99	-74.07	71.06
L2C	1227.6	2.046	16.53	-73.25	70.24
E5a–L5	1176.45	20.46	162.41	-73.74	70.73
E5b	1191.79	20.46	164.53	-74.30	71.29

Table III. Gain and Noise Budget for the AFE (L2C Band)

	Input	LNA	BPF	LA
Gain [dB]		18	-2	50
NF [dB]		2	2	10
Carrier Power [dBm]	-130	-112	-114	-64
Noise Power [dBm]	-110	-90	-90	-30
SNR [dB]	-19	-21	-21	-34
Cascaded NF [dB]		2	2	2.2

6. CONCLUSIONS

The proposed receiver provides a low-complexity and flexible platform which can handle multi-band GPS and Galileo signal acquisition with minimal RF component thereby eliminating and circumventing the cost and impairments associated with them. Exploiting the characteristics of the CT $\Sigma\Delta$ modulator ADC to perform BPS can simplify the AFE by shifting the IF processing into the digital domain. Reconfiguration in the digital domain can be done in order to achieve dynamic adaptation to the signal environment. System level simulations indicate that the proposed receiver is viable with acceptable performance.

REFERENCES

[1] J. Mitola, "The software radio architecture," IEEE Communications Magazine, Vol. 33, No. 5, pp. 26-38, May 1995.

[2] F.K. Jondral, "Software-Defined Radio - Basics and Evolution to Cognitive Radio," EURASIP Journal on Wireless Communications and Networking, pp. 275–283, March 2005.

[3] R.G. Vaughan, N.L. Scott, and D.R. White, "The Theory of Bandpass Sampling," IEEE Transactions on Signal Processing , Vol. 39, No .9, pp. 1973-1984, Sep 1991.

[4] D.M. Akos, M. Stockmaster, J.B.Y Tsui, and J. Caschera, "Direct Bandpass Sampling of Multiple Distinct RF Signals,2 IEEE Transactions on Communications, Vol.47, No.7, pp.983-988, Jul 1999.

[5] D.M. Akos, A. Ene, and J. Thor, "A Prototyping Platform for Multi-Frequency GNSS Receivers," Proceedings of the 16th International Technical Meeting of the Satellite Division of The Institute of Navigation ION GPS/GNSS 2003, Portland, Oregon, Sep 2003.

[6] R. Pickholtz, D. Schilling, and L. Milstein, "Theory of Spread-Spectrum Communications–A Tutorial," IEEE Transactions on Communications, Vol.30, No.5, pp. 855-884, May 1982.

[7] I. Galdi, E. Bonizzoni, P. Malcovati, G. Manganaro, and F. Maloberti, "40 MHz IF 1 MHz Bandwidth Two-Path Bandpass $\Sigma\Delta$ Modulator With 72 dB DR Consuming 16 mW," IEEE Journal of Solid-State Circuits, Vol.43, No.7, pp.1648-1656, Jul 2008.

[8] T. Christen, T. Burger, and H. Qiuting, "A 0.13/spl mu/m CMOS EDGE/UMTS/WLAN Tri-Mode $\Sigma\Delta$ ADC with -92dB THD," IEEE International Solid-State Circuits Conference, 2007. ISSCC 2007. pp.240-599, 11-15 Feb 2007.

[9] A. Tabatabaei, K. Onodera, M. Zargari, H. Samavati, and D.K. Su, "A dual channel $\Sigma\Delta$ ADC with 40MHz aggregate signal bandwidth," IEEE International Solid-State Circuits Conference, 2003. Digest of Technical Papers, Vol.1, pp. 66-478, 2003.

[10] P. Bénabès, M. Keramat, and R. Kielbasa, "Synthesis and Analysis of Sigma-Delta Modulators Employing Continuous-Time Filters," Analog Integrated Circuits Signal Processing, Vol.23, No.2, pp. 141-152, May 2000.

[11] K.P.J. Thomas, R.S. Rana, Yong Lian, "A 1GHz CMOS fourth-order continuous-time bandpass sigma delta modulator for RF receiver front end A/D conversion," Proceedings of the ASP-DAC Design Automation Conference 2005, Vol.2, pp. 665-670 18-21 Jan 2005.

[12] S. Benabid, E. Najafi Aghdam, P. Benabes, S. Guessab, R. Kielbasa, "CMOS design of a multibit bandpass continuous-time sigma delta modulator running at 1.2 GHz," Proceedings of the Fifth IEEE International Caracas Conference on Devices, Circuits and Systems, 2004., Vol.1, pp. 51-55, 3-5 Nov 2004.

[13] R. van Veldhoven, "A Tri–mode Continuous–Time $\Sigma\Delta$ Modulator with Switched–Capacitor Feedback DAC for a GSM-EDGE/CDMA2000/UMTS Receiver," proc. IEEE International Solid-State Circuits Conference, pp. 60-61, 2003.

[14] G. Gielen and E. Goris, "Reconfigurable Front-end Architectures and A/D Converters for Flexible Wireless Transceivers for 4G radios," IEEE 7th CAS Symposium on Emerging Technologies: Circuits and Systems for 4G Mobile Wireless Communications, pp. 13-18, Jun 2005.

[15] J. Candy, "A Use of Double Integration in Sigma Delta Modulation," IEEE Transactions on Communications, Vol.33, No.3, pp. 249-258, Mar 1985.

[16] O. Shoaei, W.M. Snelgrove, "Design and implementation of a tunable 40 MHz-70 MHz Gm-C bandpass $\Delta\Sigma$ modulator," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol.44, No.7, pp.521-530, Jul 1997.

[17] A.I. Hussein, N.M. Ibrahim, W.B. Kuhn, "Accurate formulation of the signal-to-noise ratio in continuous-time bandpass noise shaping A/D converters," IEE Proceedings on Circuits, Devices and Systems, Vol.153, No.2, pp. 173-178, Apr 2006.

[18] C.A. DeVries, R.D. Mason, "Subsampling Architecture for Low Power Receivers," IEEE Transactions on Circuits and Systems II: Express Briefs, Vol.55, No.4, pp.304-308, April 2008

[19] W. Bennett, "Spectra of quantized signals," Bell Sys. Tech. Journal, Vol27, pp. 446-472, Jul 1948.

[20] D.H. Shen, Chien-Meen Hwang, B.B. Lusignan, B.A. Wooley, "A 900-MHz RF front-end with integrated discrete-time filtering," , IEEE Journal of Solid-State Circuits, Vol.31, No.12, pp.1945-1954, Dec 1996.

[21] K.B. Kim; T.S. Yun, K. Wu, and C.S. Park, "Reconfigurable RF Active Bandpass Filter with BaxSr1-xTiO3 Varactor", Electronics Letters , Vol. 44, No. 2, pp. 135-136, January 2008.

[22] E. Cetin, I. Kale, R.C.S. Morling, "Analysis and Compensation of RF Impairments for Next Generation Multimode GNSS Receivers," IEEE International Symposium on Circuits and Systems, ISCAS 2007, pp.1729-1732, 27-30 May 2007.

[23] A. Ucar, E. Cetin, I. Kale, "A Low Complexity DSP Driven Analog Impairment Mitigation Scheme for Low-IF GNSS Receivers," IEEE/ION PLANS 2008, Monterey, CA, 5–8 May 2008.

[24] A. Ucar, R, Kazazoglu, E. Cetin, and I. Kale, "GNSScope: Overview of a Toolbox for End-to-End Modeling, Simulation and Analysis of GNSS," New Navigators Seminar, London Jun 2008.